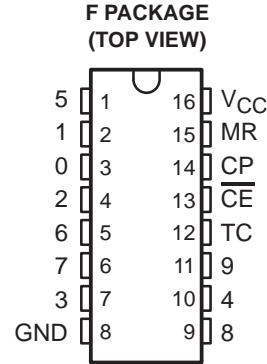


**CD54HCT4017**  
**DECADE COUNTER/DIVIDER**  
**WITH TEN DECODED OUTPUTS**  
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- 4.5-V to 5.5-V Operation
- Fully Static Operation
- Buffered Inputs
- Common Reset
- Positive-Edge Clocking
- Balanced Propagation Delay and Transition Times
- Direct LSTTL Input Logic Compatibility
  - $V_{IL} = 0.8 \text{ V}$  Maximum;  $V_{IH} = 2 \text{ V}$  Minimum
- CMOS Input Compatibility
  - $I_I \leq 1 \mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$
- Packaged in Ceramic (F) DIP Packages and Also Available in Chip Form (H)



**description**

The CD54HCT4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each decoded output normally is low and sequentially goes high on the low-to-high transition of the clock (CP) input. Each output stays high for one clock period of the ten-clock-period cycle. The terminal count (TC) output transitions low to high after output ten (9) goes low, and can be used in conjunction with the clock enable ( $\overline{\text{CE}}$ ) input to cascade several stages.  $\overline{\text{CE}}$  disables counting when in the high state. The master reset (MR) input, when taken high, sets all the decoded outputs, except 0, to low.

The CD54HCT4017 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

**FUNCTION TABLE**

INPUTS			OUTPUT STATE†
CP	$\overline{\text{CE}}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

† If  $n < 5$ , TC = H; otherwise, TC = L.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

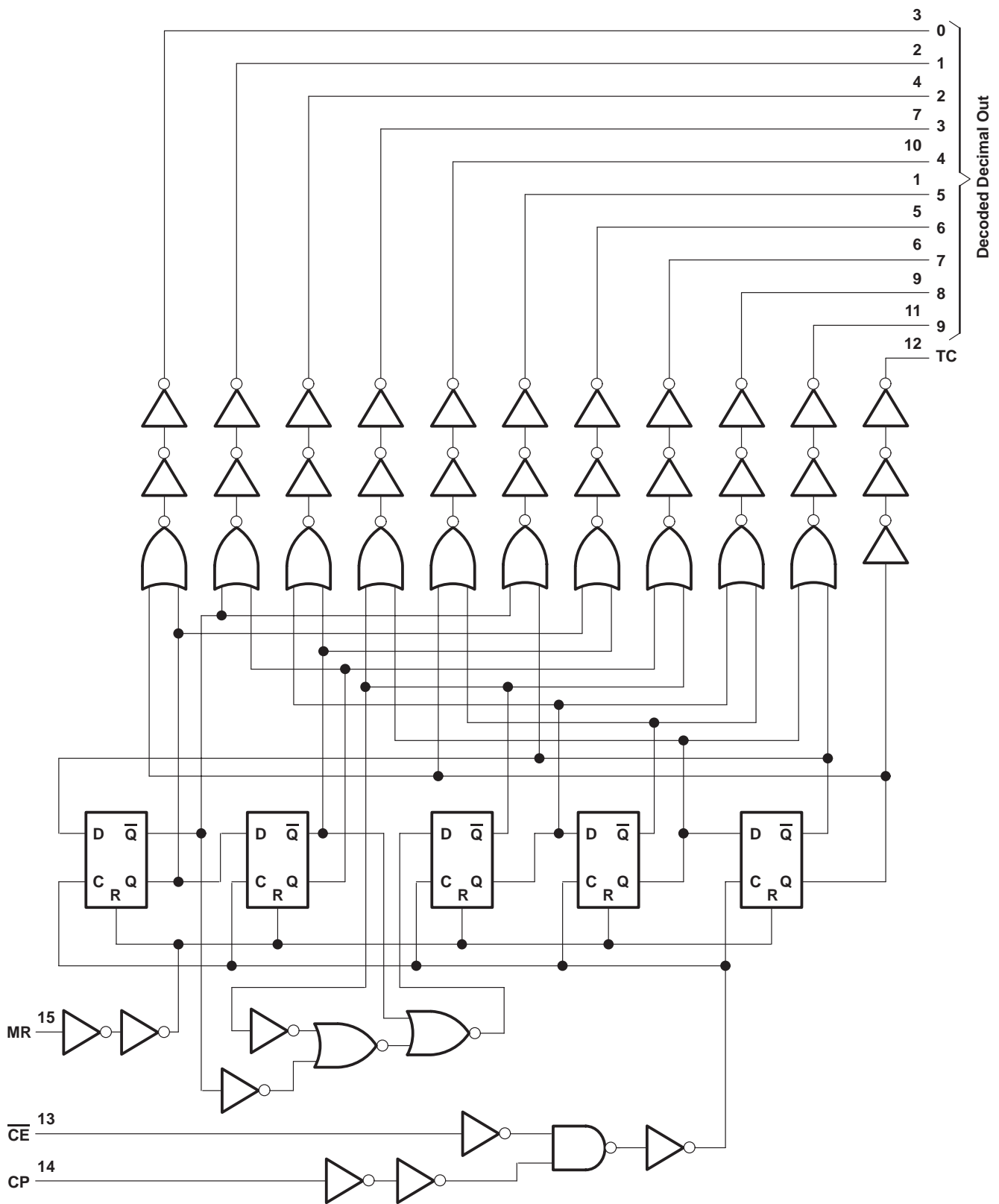


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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ V or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ V or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, each output pin, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ ) .....	±25 mA
$V_{CC}$ or ground current, $I_{CC}$ .....	±50 mA
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions (see Note 1)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
$T_A$	Operating free-air temperature		–55	125	°C

NOTE 1: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V <sub>OH</sub>	CMOS loads	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>O</sub> = -0.02 mA	4.5 V	4.4			4.4	V	
	TTL loads	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>O</sub> = -4 mA	4.5 V	3.98			3.7		
V <sub>OL</sub>	CMOS loads	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>O</sub> = 0.02 mA	4.5 V	0.1			0.1	V	
	TTL loads	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>O</sub> = 4 mA	4.5 V	0.26			0.4		
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> to 0	5.5 V	±100			±1000	nA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	8			160	μA	
ΔI <sub>CC</sub> <sup>†</sup>		V <sub>I</sub> = V <sub>CC</sub> to 2.1 V, I <sub>O</sub> = 0	4.5 to 5.5 V	100	360	490	μA		
C <sub>i</sub>				10	10	10	pF		

<sup>†</sup> For dual-supply systems, theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

**INPUT LOADING**

INPUT	UNIT LOAD
CP	0.15
$\overline{\text{CE}}$	0.25
MR	0.3

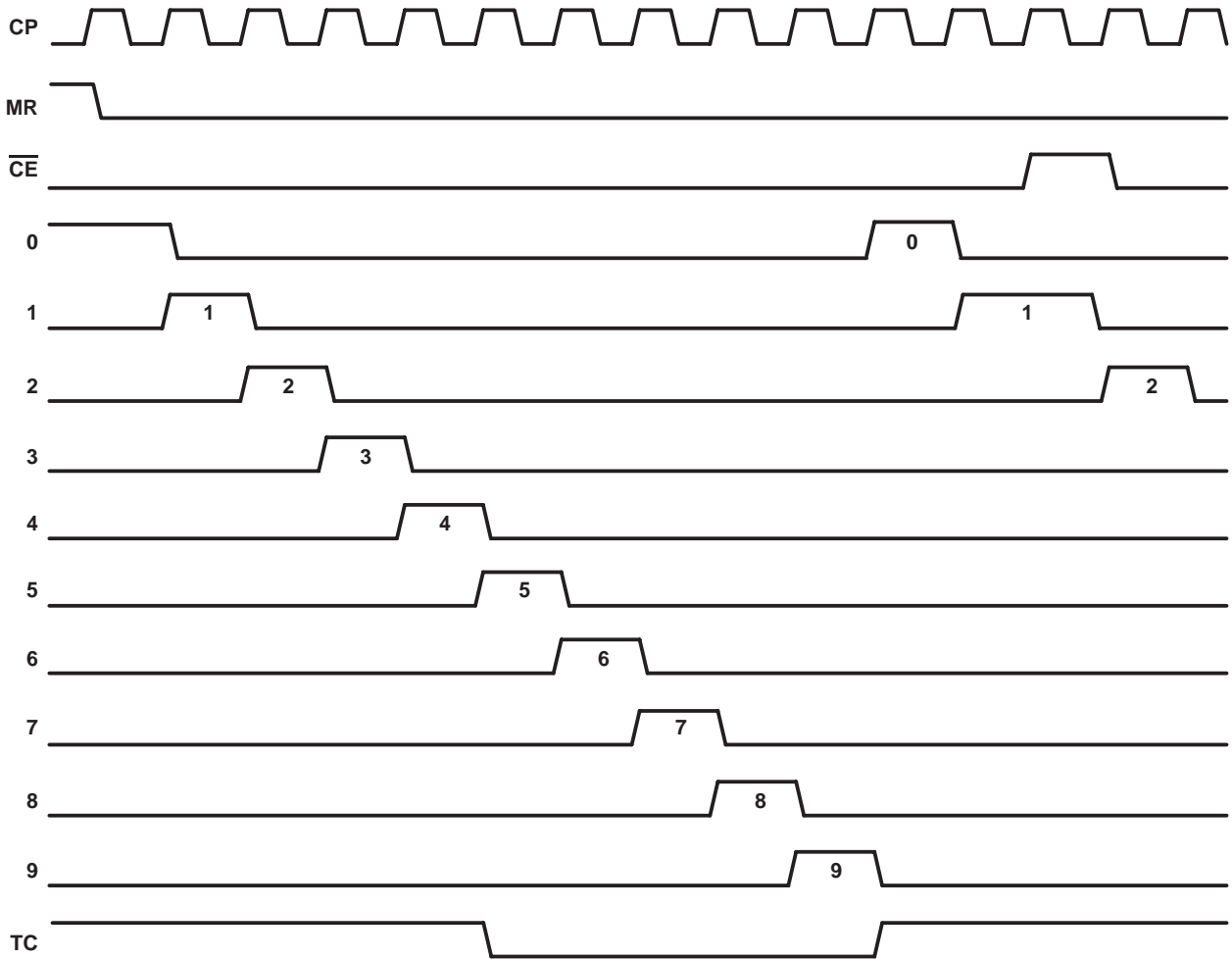
Unit load is ΔI<sub>CC</sub> limit, e.g., 360 μA MAX at T<sub>A</sub> = 25°C.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Maximum clock frequency	4.5 V	25		17		MHz
t <sub>w</sub>	Pulse duration	CP	4.5 V		16	24	ns
		MR	4.5 V		16	24	
t <sub>su</sub>	Setup time, $\overline{\text{CE}}$ to CP	4.5 V	15		22		ns
t <sub>h</sub>	Hold time, $\overline{\text{CE}}$ to CP	4.5 V	0		0		ns
t <sub>rem</sub>	Removal time, MR	4.5 V	5		5		ns



timing requirements



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switching characteristics,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Figures 1 and 2)

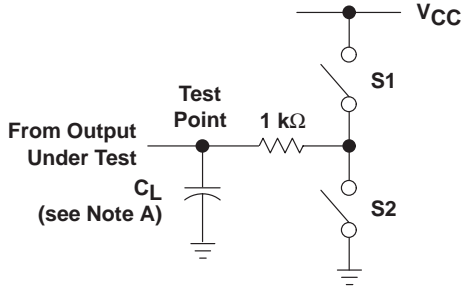
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	
f <sub>max</sub>			4.5 V	25		17		MHz
t <sub>PLH</sub>	CP	Any output	4.5 V	46		69		ns
t <sub>PHL</sub>		TC		46		69		
t <sub>PLH</sub>	$\overline{\text{CE}}$	Any output	4.5 V	50		75		ns
t <sub>PHL</sub>		TC		50		75		
t <sub>PLH</sub>	MR	Any output	4.5 V	46		69		ns
t <sub>PHL</sub>		TC		46		69		
t <sub>THL</sub>		Any output	4.5 V	15		22		ns
t <sub>TLH</sub>		TC		15		22		

**operating characteristics**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	39	pF

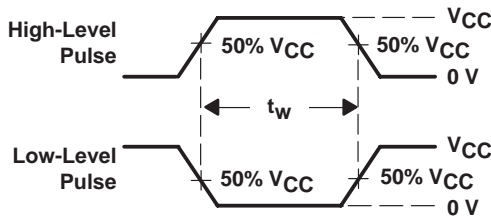


PARAMETER MEASUREMENT INFORMATION

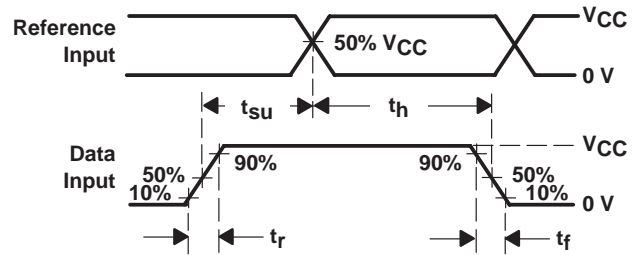


LOAD CIRCUIT

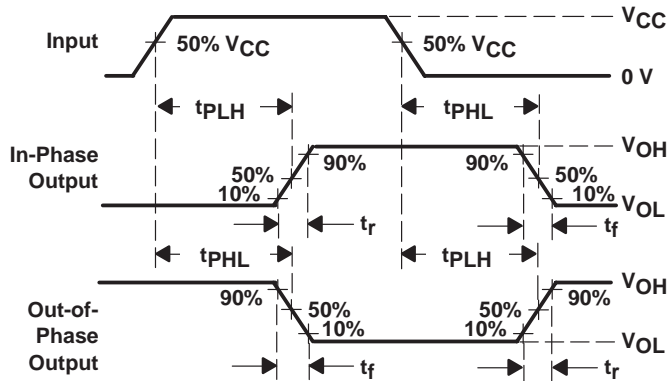
PARAMETER		S1	S2
$t_{en}$	tpZH	Open	Closed
	tpZL	Closed	Open
$t_{dis}$	tPHZ	Open	Closed
	tPLZ	Closed	Open
$t_{pd}$ or $t_t$		Open	Open



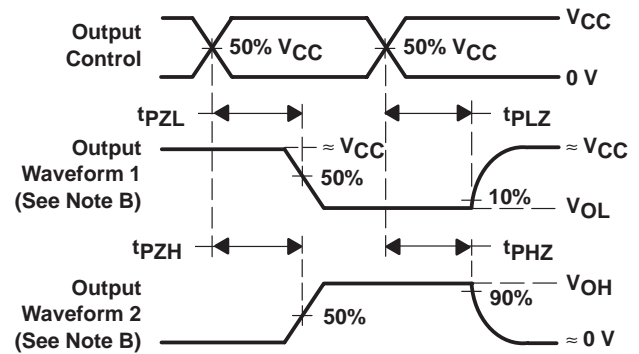
VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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**PARAMETER MEASUREMENT INFORMATION**

INPUT LEVEL	$V_{CC}$
$V_S$	$0.5 V_{CC}$

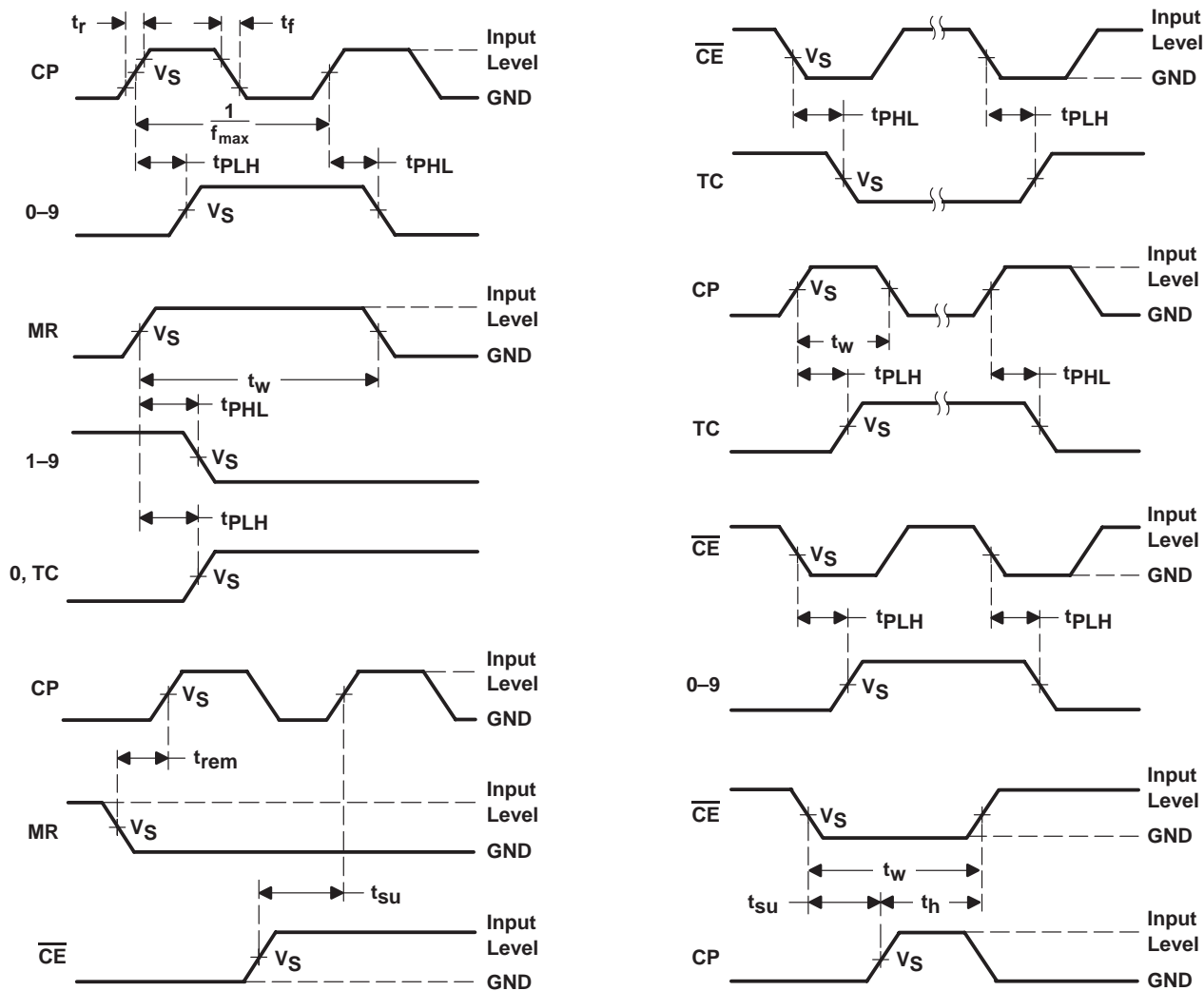


Figure 2. Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54HCT4017F3A	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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