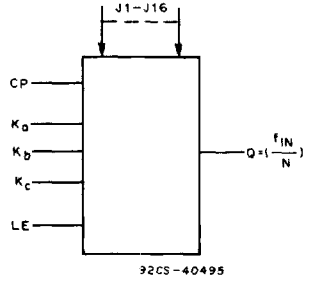
File Number **1853**

CD54/74HC4059
CD54/74HCT4059

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

CMOS Programmable Divide-by-"N" Counter

Type Features:
- *Synchronous programmable ÷ N counter: N = 3 to 9999 or 15999*
- *Presettable down-counter*
- *Fully static operation*
- *Mode-select control of initial decade counting function (÷ 10, 8, 5, 4, 2)*
- *Master preset initialization*
- *Latchable ÷ N output*

The RCA-CD54/74HC4059 and the CD54/74HCT4059 are high-speed silicon-gate devices that are pin-compatible with the CD4059B devices of the CD4000B series. These devices are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock cycle wide occurring at a rate equal to the input frequency divided by N. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set "high", Kb "high" and Kc "low". Jam inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counter can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

Applications:
- *Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.*
- *Fixed or programmable frequency division*
- *"Time out" timer for consumer-application industrial controls*
- *Companion Application Note, ICAN-6374, "Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"*

CD54/74HC4059
CD54/74HCT4059

from which counting down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table I. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷ 5 mode is selected. Whenever the master preset mode is used, control signals Kb = "low" and Kc = "low" must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig. 1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used, the counter jumps back to the "Jam" count when the output pulse appears.

A "high" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "low". If the Latch Enable is "low", the output pulse will remain high for only 1 cycle of the clock-input signal.

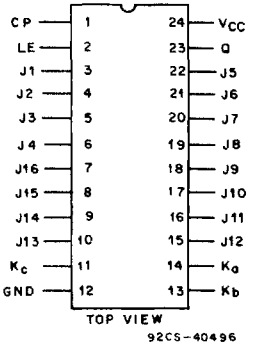
The CD54HC4059 and CD54HCT4059 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4059 and CD74HCT4059 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Table I

Mode Select Input			First Counting Section			Last Counting Section			Counter Range	
									Design	Extended
Ka	Kb	Kc	Mode Di-vides by:	Can be preset to a max. of:	Jam• inputs used:	Mode Di-vides by:	Can be preset to a max. of:	Jam• inputs used:	Max.	Max.
H	H	H	2	1	J1	8	7	J2,J3,J4	15,999	17,331
L	H	H	4	3	J1,J2	4	3	J3,J4	15,999	18,663
H	L	H	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
L	L	H	8	7	J1,J2,J3	2	1	J4	15,999	21,327
H	H	L	10	9	J1,J2,J3,J4	1	0	—	9,999	16,659
X	L	L	Master Preset			Master Preset			—	—

X = Don't Care
•J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷ 5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷ 5 mode. At power turn-on, Kc must be "low" for a period of 3 input clock pulses after V_{CC} reaches a minimum of 3 volts.



TERMINAL ASSIGNMENT

CD54/74HC4059
CD54/74HCT4059

How to Preset the CD54/74HC/HCT4059 to Desired ÷ N

The value N is determined as follows:

N = (MODE*) (1000 x Decade 5 Preset + 100 x Decade 4 Preset + 10 x Decade 3 Preset + 1 x Decade 2 Preset) + Decade 1 Preset (1)

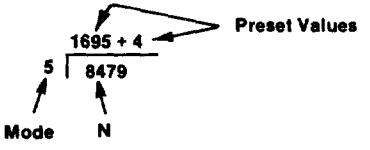
*MODE = First counting section divider (10, 8, 5, 4, or 2)

To calculate preset values for any N count, divide the N count by the Mode. The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Example:

N = 8479, Mode = 5



Mode Select = 5

Ka	Kb	Kc
H	L	H

Program Jam Inputs (BCD)

4			1	5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

To verify the results, use Equation 1:

N = 5 (1000 x 1 + 100 x 6 + 10 x 9 + 1 x 5) + 4

N = 8479

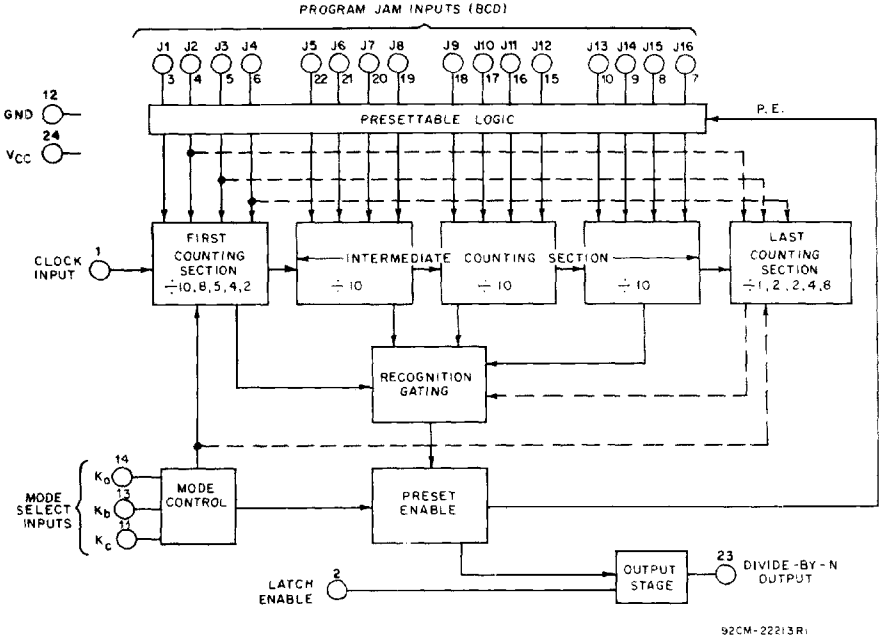


Fig. 1 - Functional block diagram.

CD54/74HC4059
CD54/74HCT4059

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... **-0.5 to +7 V**
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... **±20 mA**
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... **±20 mA**
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... **±25 mA**
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... **±50 mA**
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... **500 mW**
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... **Derate Linearly at 8 mW/°C to 300 mW**
For T_A = -55 to +100°C (PACKAGE TYPE F,H) ..... **500 mW**
For T_A = +100 to +125°C (PACKAGE TYPE F,H) ..... **Derate Linearly at 8 mW/°C to 300 mW**
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... **400 mW**
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... **Derate Linearly at 6 mW/°C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H ..... **-55 to +125°C**
PACKAGE TYPE E,M ..... **-40 to +85°C**
STORAGE TEMPERATURE (T_{stg}) ..... **-65 to +150°C**
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... **+265°C**
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... **+300°C**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4059
CD54/74HCT4059

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4059/CD54HC4059										CD74HCT4059/CD54HCT4059									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All J Inputs	0.5
CP	0.65
LE	1.65
Ka	1
Kb	1.5
Kc	0.85

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4059
CD54/74HCT4059

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay: CP to Q	t_{PLH} t_{PHL}	15	17	19	ns
LE to Q			14	19	
CP Frequency	f_{MAX}	15	54	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	36	36	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

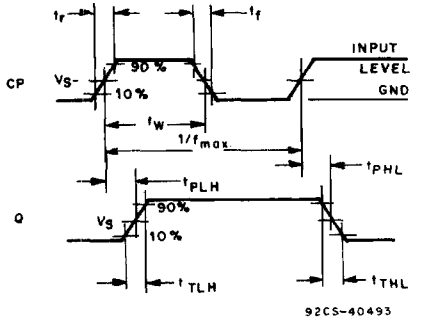
PRE-REQUISITE FOR SWITCHING FUNCTION

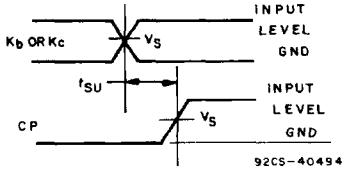
CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS 25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Pulse Width CP	t_W	2	90	—	—	—	115	—	—	—	135	—	—	—	ns
		4.5	18	—	20	—	23	—	25	—	27	—	30	—	
		6	15	—	—	—	20	—	—	—	23	—	—	—	
Setup Time Kb, Kc to CP	t_{SU}	2	75	—	—	—	95	—	—	—	110	—	—	—	
		4.5	15	—	15	—	19	—	19	—	22	—	22	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
CP Frequency	f_{MAX}	2	5	—	—	—	4	—	—	—	4	—	—	—	MHz
		4.5	27	—	25	—	22	—	20	—	18	—	17	—	
		6	32	—	—	—	26	—	—	—	21	—	—	—	

CD54/74HC4059
CD54/74HCT4059

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{CC} (V)	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	
	t_{PHL}	4.5	—	40	—	46	—	50	—	58	—	60	—	69	
CP to Q		6	—	34	—	—	—	43	—	—	—	51	—	—	
		2	—	175	—	—	—	220	—	—	—	265	—	—	
LE to Q		4.5	—	35	—	46	—	44	—	58	—	53	—	69	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times, and setup times.