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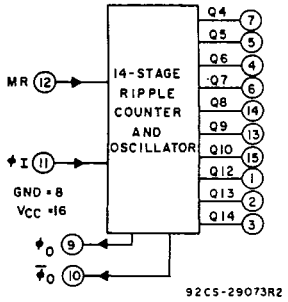
CD54/74HC4060, CD54/74HCT4060



FUNCTIONAL DIAGRAM

14-Stage Binary Counter with Oscillator

Type Features:

- *Onboard oscillator*
- *Common reset*
- *Negative edge clocking*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF*

The RCA-CD54/74HC4060 and CD54/74HCT4060 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_O). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switchpoints are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

The CD54HC4060 and CD54HCT4060 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4060 and CD74HCT4060 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD 54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL}=0.8 V Mas., V_{IH}=2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

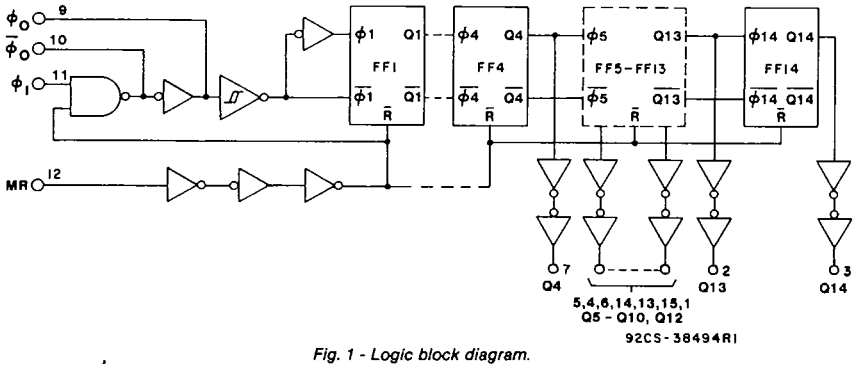


Fig. 1 - Logic block diagram.

Advance Information/
Preliminary Data

File Number **1654**

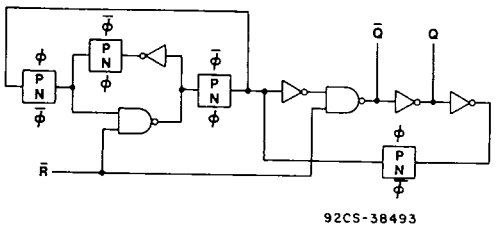


Fig. 2 - Flip-flop detail.

TRUTH TABLE T-45-23-17

ϕ_I	MR	OUTPUT STATE
⌐	L	No Change
⌐	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_o < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +60°C (PACKAGE TYPE M) ..... 300 mW
For T_A = +60 to +85°C (PACKAGE TYPE M) ..... Derate Linearly at 5 mW/°C to 175 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4060, CD54/74HCT4060

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4060, CD54HC4060										CD74HCT4060, CD54HCT4060									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			−40/ +85°C		−55/ +125°C		V_I V	V_{CC} V	+25°C			−40/ +85°C		−55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage Q Outputs CMOS Loads V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} ** or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage Q Outputs TTL Loads V_{OH}	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} ** or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage Q Outputs CMOS Loads V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} ** or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage Q Outputs TTL Loads V_{OL}	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} ** or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										

**For Pin 11 V_{IH}=3.15 V, V_{IL}=0.9 V.

CD54/74HC4060, CD54/74HCT4060

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STATIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CD74HC4060, CD54HC4060										CD74HCT4060, CD54HCT4060								UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Output Voltage V_{OH} $\bar{\Phi}_O$ Output (Pin 10) CMOS Loads	V_{CC} or Gnd	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{CC} or Gnd	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage V_{OH} $\bar{\Phi}_O$ Output (Pin 10) TTL Loads ◇	V_{CC} or Gnd	-2.6	4.5	3.98	—	—	3.84	—	3.7	—	V_{CC} or Gnd	4.5	3.98	—	—	3.84	—	3.7	—	V
		-3.3	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} $\bar{\Phi}_O$ Output (Pin 10) CMOS Loads	V_{CC} or Gnd	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{CC} or Gnd	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage V_{OL} $\bar{\Phi}_O$ Output (Pin 10) TTL Loads	V_{CC} or Gnd	2.6	4.5	—	—	0.26	—	0.33	—	0.4	V_{CC} or Gnd	4.5	—	—	0.26	—	0.33	—	0.4	V
		3.3	6	—	—	0.26	—	0.33	—	0.4										
High-Level Output Voltage V_{OH} Φ_O Output (Pin 9) TTL Loads	V_{IL} or V_{IH}	-3.2	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} ** or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} Φ_O Output (Pin 9) TTL Loads	V_{IL} or V_{IH}	3.2	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} ** or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Pin II V_{IL} = 0.9V, V_{IH} = 3.15V

◇Limits not valid when pin 12 (instead of pin 11) is used as control input.

HCT INPUT LOADING

INPUT	UNIT LOADS*
MR	0.35

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4060, CD54/74HCT4060

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L pF	Typical		UNITS
			HC	HCT	
Propagation Delay ϕ_1 to Q_4	t_{PLH} t_{PHL}	15	25	25	ns
Propagation Delay Qn to Qn+1	t_{PLH} t_{PHL}	15	6	6	ns
Propagation Delay MR to Qn Output	t_{PHL}	15	17	17	ns
Propagation Dissipation Capacitance*	C_{PD}	—	40	40	pF

C_{PD} is used to determine the dynamic power consumption, per package.
$PD = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_i/M)$ where:
M = 2^1, 2^2, 2^3,..2^{14}
C_L = output load capacitance
fi = input frequency

Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Input Pulse Width (Figure 4)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time (Figure 5)	t_{REM}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	26	—	25	—	33	—	30	—	39	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Reset Pulse Width (Figure 5)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	28	—	20	—	35	—	24	—	42	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay ϕ_1 to Q_4 Output (Figure 4)	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t_{PHL}	4.5	—	60	—	66	—	75	—	83	—	90	—	100	
	—	6	—	51	—	—	—	64	—	—	—	78	—	—	
Propagation Delay Q_n to Q_{n+1} (Figure 4)	t_{PLH}	2	—	80	—	—	—	100	—	—	—	120	—	—	ns
	t_{PHL}	4.5	—	16	—	16	—	20	—	20	—	24	—	24	
	—	6	—	14	—	—	—	17	—	—	—	20	—	—	
Propagation Delay MR to Q_n Output (Figure 5)	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	44	—	50	—	55	—	60	—	66	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition Time (Figure 4)	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	—	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I*														

*TBD

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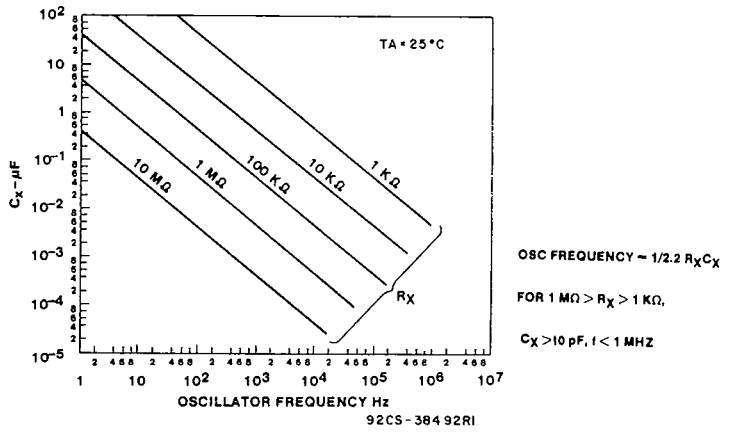
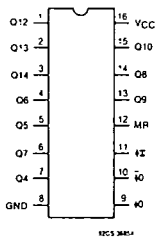
TYPICAL LIMIT VALUES FOR R_X AND C_X

CHARACTERISTIC	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R_X Min.	$C_X > 1000$ pF	2	1 KΩ
	$C_X > 10$ pF	4.5	
	$C_X > 10$ pF	6	
R_X Max.	$C_X > 10$ pF	2	20 MΩ
	$C_X > 10$ pF	4.5	
	$C_X > 10$ pF	6	
C_X Min.	$R_X > 10$ KΩ	2	10 pF
	$R_X > 10$ KΩ	4.5	
	$R_X > 10$ KΩ	6	
	$R_X = 1$ KΩ	2	1000 pF
	$R_X = 1$ KΩ	4.5	10 pF
	$R_X = 1$ KΩ	6	10 pF
Maximum Astable Oscillator Frequency	$C_X = 1000$ pF, $R_X = 1$ KΩ	2	0.5 MHz*
	$C_X = 100$ pF, $R_X = 1$ KΩ	4.5	3 MHz*
	$C_X = 100$ pF, $R_X = 1$ KΩ	6	3 MHz*

*At very high frequencies f = 1/2.2 R_XC_X no longer gives an accurate approximation.

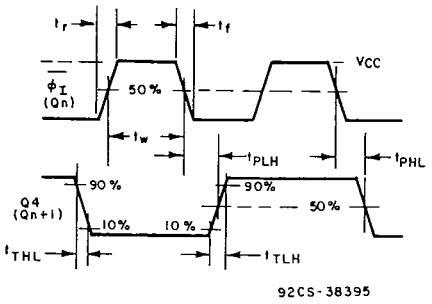


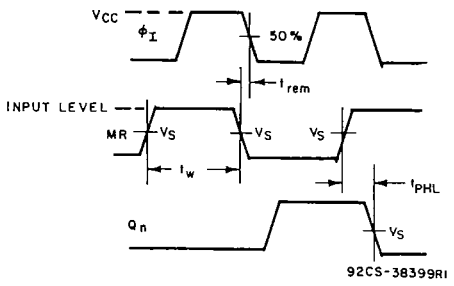


TERMINAL ASSIGNMENT

Fig. 3 - Frequency of on-board oscillator as a function of C_X and R_X.

CD54/74HC4060, CD54/74HCT4060





	54/74HC	54/74HCT
MR Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times for both HC and HCT types.

Fig. 5 - Master Reset pre-requisite and propagation delays.