



HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT54/74FCT821AT/BT/CT

FEATURES:

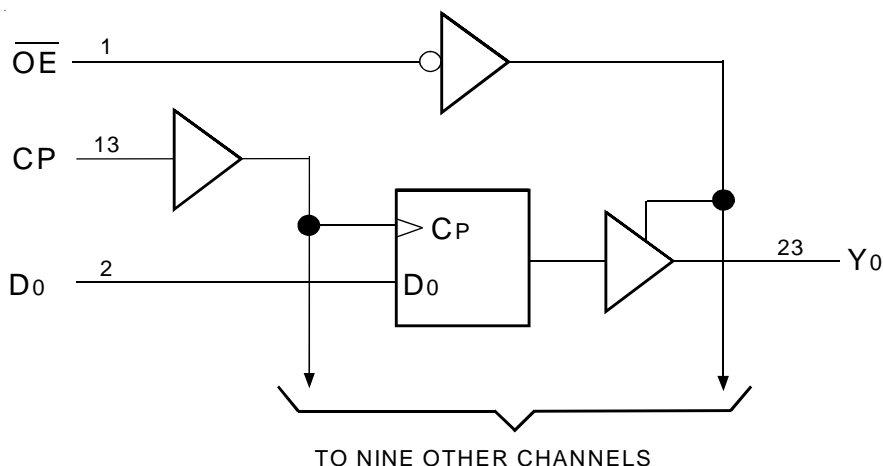
- A, B, and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Power off disable outputs permit "live insertion"
- Available in the following packages:
 - Industrial: SOIC, SSOP, QSOP
 - Military: CERDIP, LCC

DESCRIPTION:

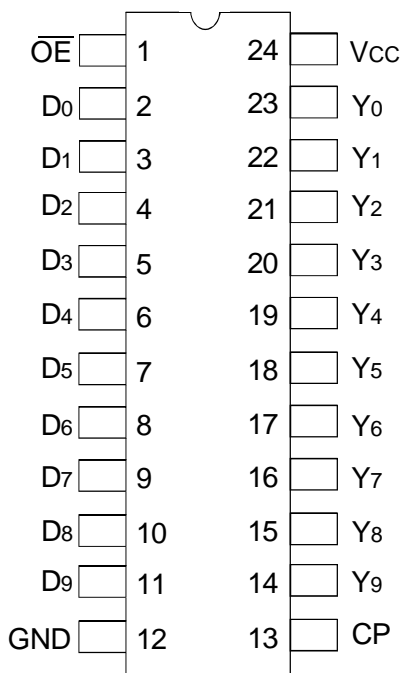
The FCT821T series is built using an advanced dual metal CMOS technology. The FCT821T series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T is a buffered, 10-bit wide version of the popular FCT374T function.

The FCT821T high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

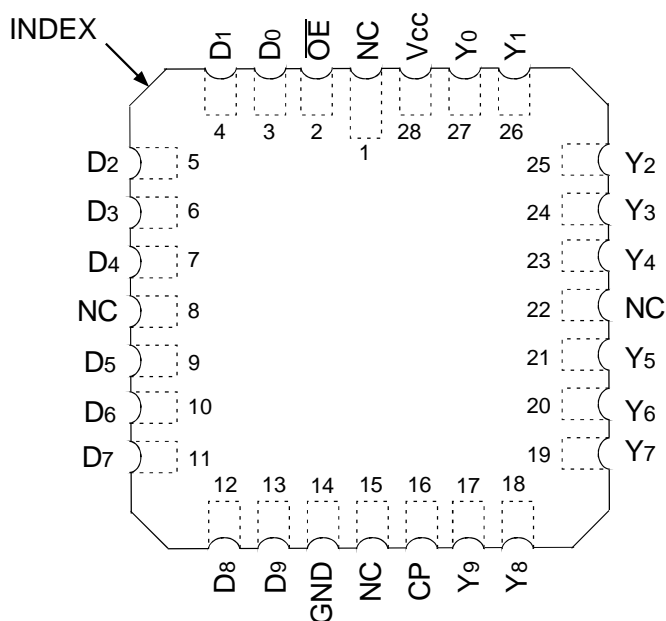
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC/ SSOP/ QSOP
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
D _x	I	D Flip-Flop Data Inputs
$\overline{\text{CLR}}$	I	When the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q _x outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register. Enters data into the register on the LOW-to-HIGH transition
Y _x	O	Register 3-State Outputs
$\overline{\text{EN}}$	I	Clock Enable. When the clock enable is LOW, data on the D _x input is transferred to the Q _x input on the LOW-to-HIGH transition. When the clock enable is HIGH, the Q _x inputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y _x outputs are in the high impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y _x outputs.

FUNCTION TABLE⁽¹⁾

Inputs					Outputs		Function
\overline{OE}	\overline{CLR}	\overline{EN}	Dx	CP	Qx	Yx	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40°C to +85°C, VCC = 5.0V ±5%; Military: TA = -55°C to +125°C, VCC = 5.0V ±10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max.	V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾	V _{CC} = Max.	V _I = 0.5V	—	—	±1	μA
I _{OZH}	High Impedance Output Current (3-State output pins) ⁽⁴⁾	V _{CC} = Max	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL I _{OH} = -8mA IND	2.4	3.3	—	V
			I _{OH} = -12mA MIL I _{OH} = -15mA IND	2	3	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL I _{OL} = 48mA IND	—	0.3	0.5	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-60	-120	-225	mA
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is ±5μA at TA = -55°C.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \overline{EN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6	16.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Output Frequency
 N_i = Number of Outputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

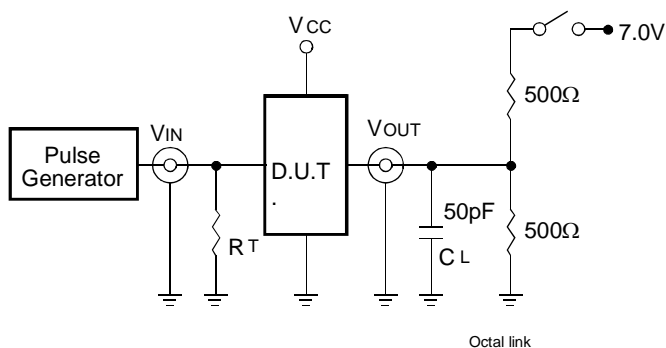
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT821AT				54FCT821BT		54/74FCT821CT				Unit
			Ind.		Mil.		Mil.		Ind.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Yx (\overline{OE} = LOW)	CL = 50pF RL = 500Ω	1.5	10	1.5	11.5	1.5	8.5	1.5	6	1.5	7	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	20	1.5	20	1.5	16	1.5	12.5	1.5	13.5	
t _{SU}	Set-up Time HIGH or LOW Dx or \overline{EN} to CP	CL = 50pF RL = 500Ω	4	—	4	—	3	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW, Dx to CP		2	—	2	—	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time HIGH or LOW, \overline{EN} to CP		2	—	2	—	0	—	0	—	0	—	ns
t _{PHL}	Propagation Delay, \overline{CLR} to Yx		1.5	14	1.5	15	1.5	9.5	1.5	8	1.5	8.5	ns
t _{REM}	Recovery Time, \overline{CLR} to CP		6	—	7	—	6	—	6	—	6	—	ns
t _w	Clock Pulse Width, HIGH or LOW		7	—	7	—	6	—	6	—	6	—	ns
t _w	\overline{CLR} Pulse Width LOW		6	—	7	—	6	—	6	—	6	—	ns
t _{PZH} t _{PZL}	Output Enable Time, \overline{OE} to Yx	CL = 50pF RL = 500Ω	1.5	12	1.5	13	1.5	9	1.5	7	1.5	8	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	23	1.5	25	1.5	16	1.5	12.5	1.5	13.5	
t _{PHZ} t _{PLZ}	Output Disable Time, \overline{OE} to Yx	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	7	1.5	8	1.5	7	1.5	6	1.5	6	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	9	1.5	8	1.5	6.5	1.5	6.5	

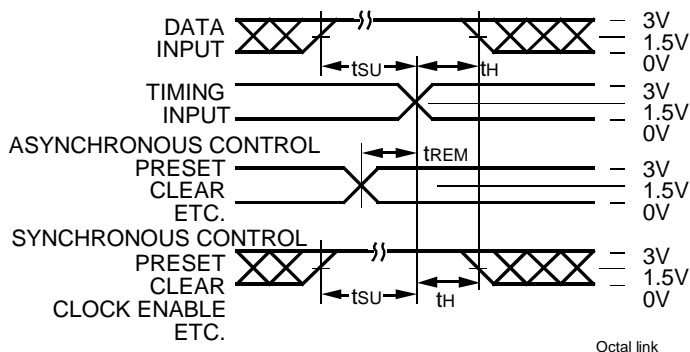
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition is guaranteed but not tested.

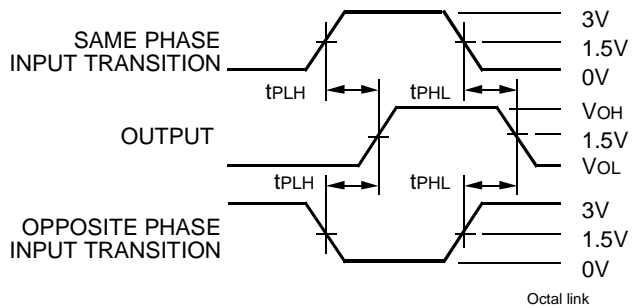
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



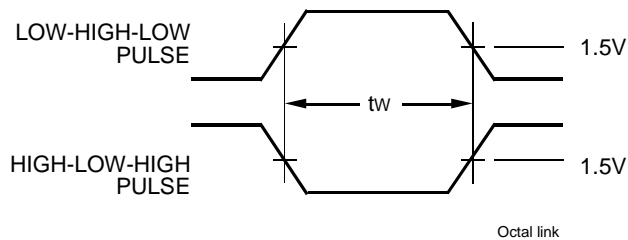
Propagation Delay

SWITCH POSITION

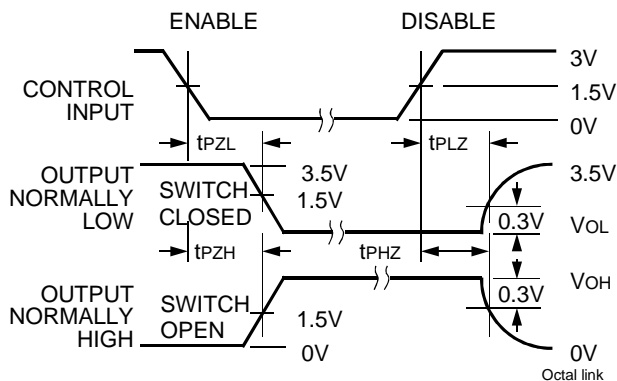
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

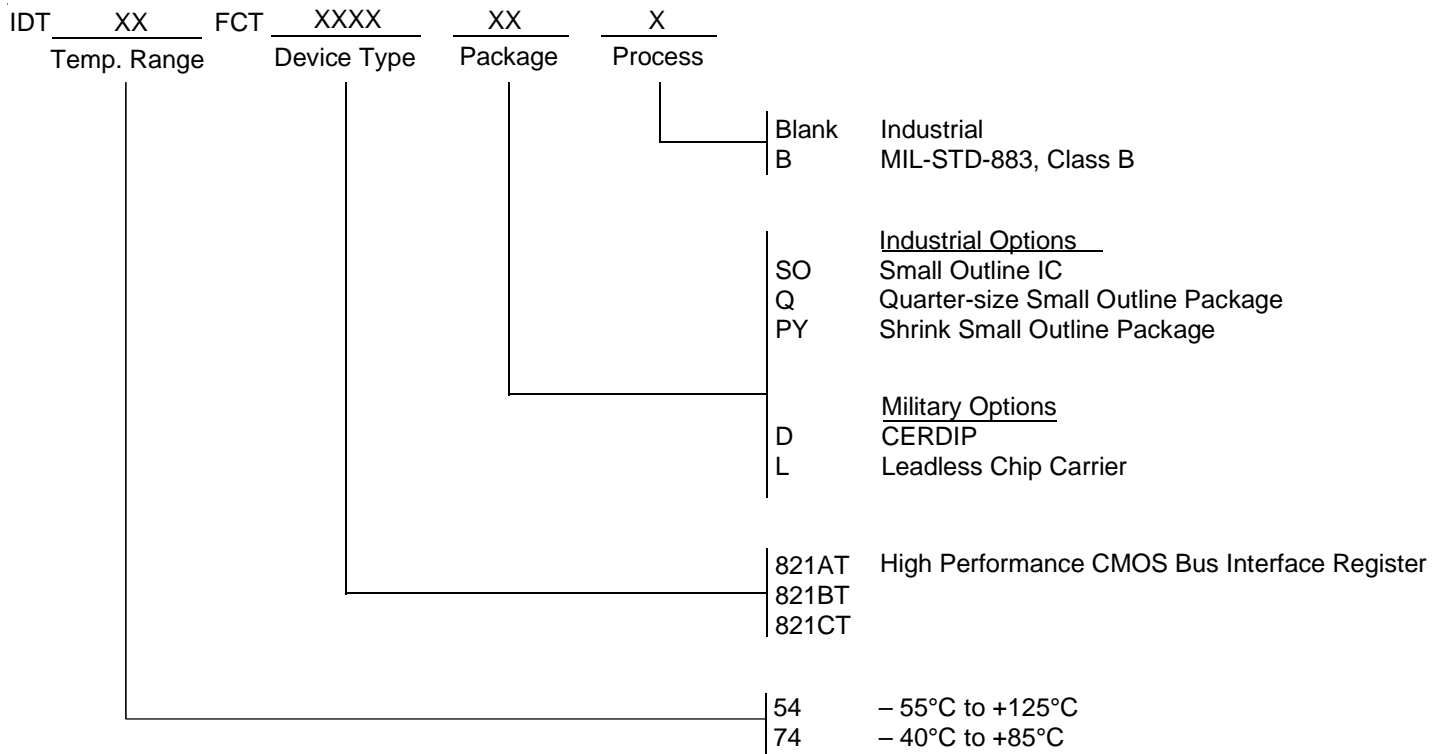


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/25/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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