Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374T/AT/CT/DT - 2374T/AT/CT
IDT54/74FCT534T/AT/CT
IDT54/74FCT574T/AT/CT/DT - 2574T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT374T/FCT534T/FCT574T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- **Features for FCT2374T/FCT2574T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION

The FCT374T/FCT2374T, FCT534T and FCT574T/FCT2574T are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

The FCT2374T and FCT2574T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

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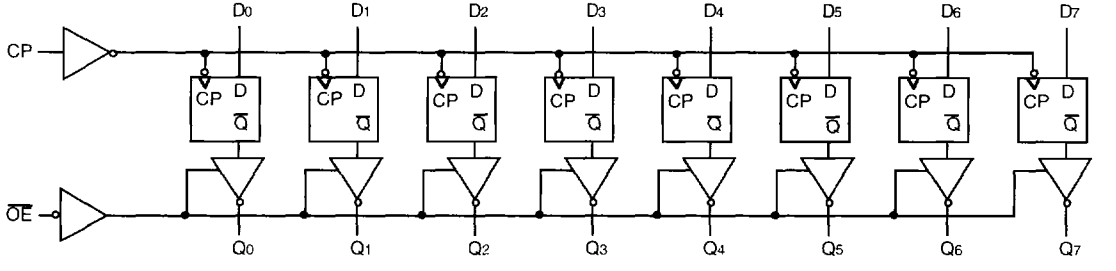
FUNCTIONAL BLOCK DIAGRAM FCT374/FCT2374T AND FCT574/FCT2574T



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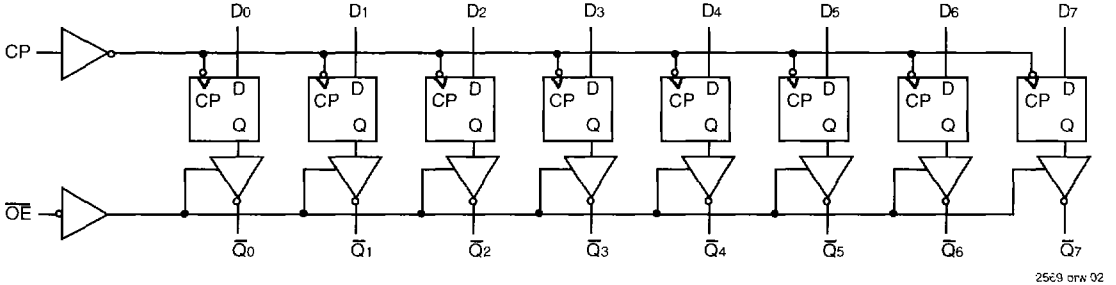
FUNCTIONAL BLOCK DIAGRAM FCT534T



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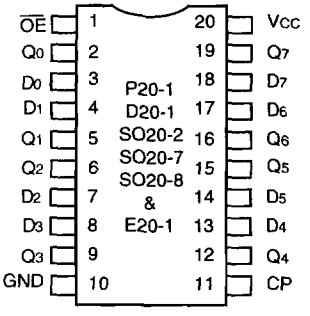
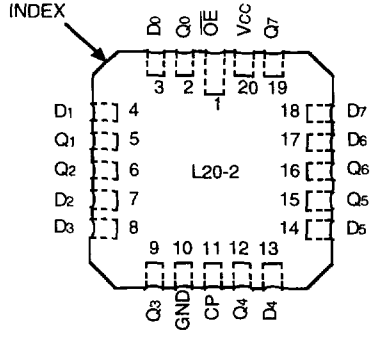
PIN CONFIGURATIONS

IDT54/74FCT374T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



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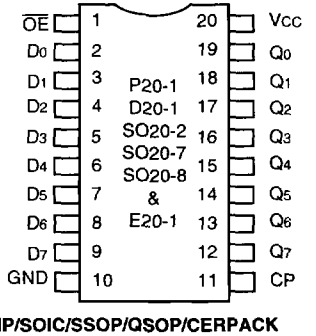
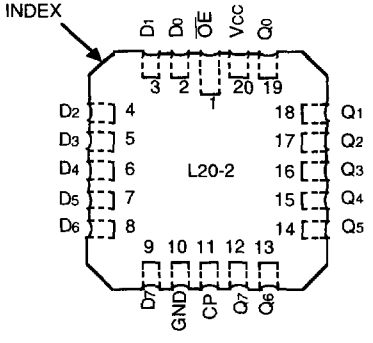
LCC
TOP VIEW

IDT54/74FCT574T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



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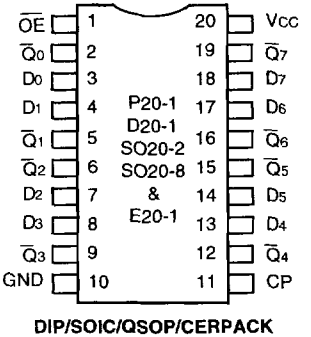
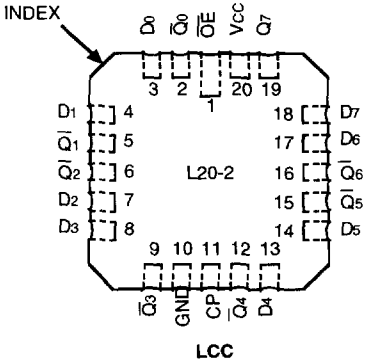
LCC
TOP VIEW

IDT54/74FCT534T



DIP/SOIC/QSOP/CERPACK
TOP VIEW



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LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
Q_N	3-state outputs, (true)
$\overline{Q}_N$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

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FUNCTION TABLE[1]

	Inputs			534		374/574	
				Outputs	Internal	Outputs	Internal
Function	$\overline{OE}$	CP	D_N	$\overline{Q}_N$	Q_N	Q_N	$\overline{Q}_N$
HI-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
LOAD REGISTER	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE:

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1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:

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1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

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1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT374T/534T/574T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max.., V_O = GND[3]		–60	–120	–225	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT2374T/2574T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT374T/534T/574T FCT2374T/2574T				FCT374AT/534AT/574AT FCT2374AT/2574AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns

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Symbol	Parameter	Conditions[1]	FCT374CT/534CT/574CT FCT2374CT/2574CT				FCT374DT/574DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	6.2	2.0	4.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.7	1.5	4.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW[4]		5.0	—	6.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. O_N for FCT374/2374T and FCT574/2574T, $\overline{O}_N$ for FCT534T.
4. This parameter is guaranteed but not tested.

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Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377T/AT/CT/DT

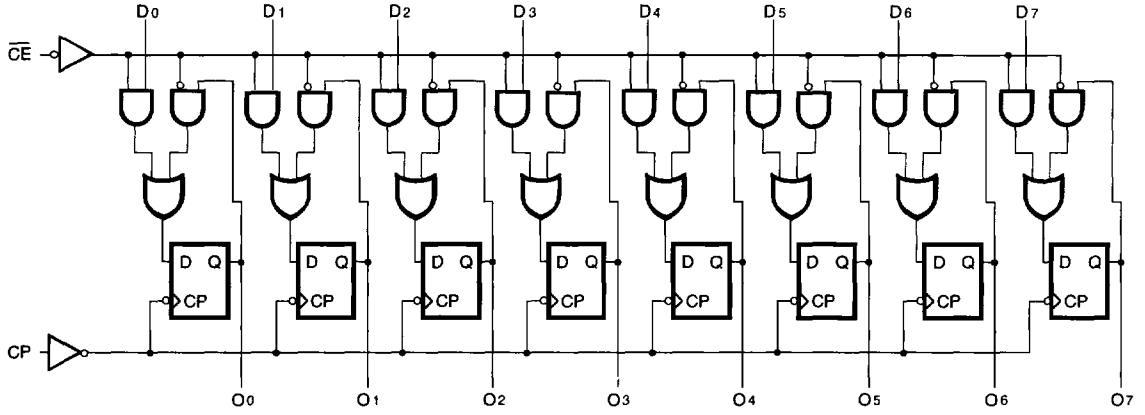
FEATURES:

- Std., A, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT377T/AT/CT/DT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT377T/AT/CT/DT have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM



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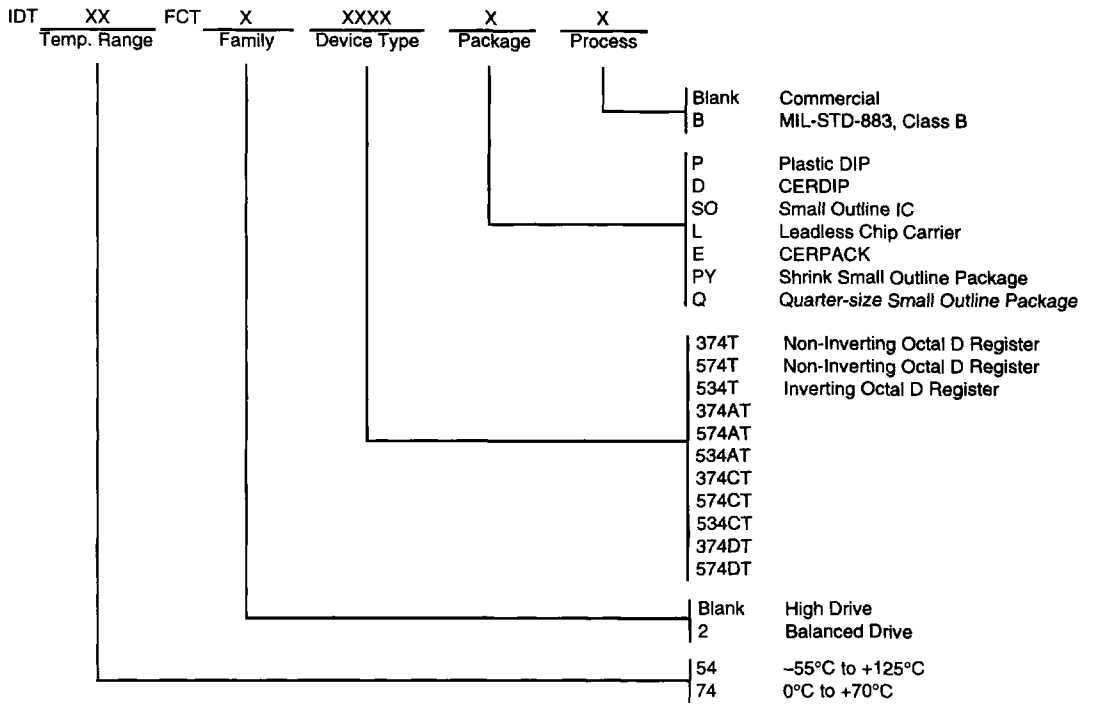
ORDERING INFORMATION



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