

December 1996

Fast CMOS Octal D Flip-Flops with Master Reset

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor On All Outputs (FCT2273T Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT273TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273CTQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT273T and CD74FCT2273T are 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) load and resets (clear) all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input.

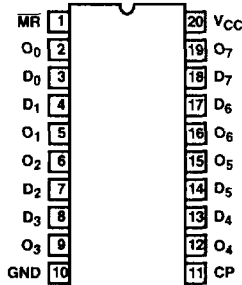
The CD74FCT2273T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

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OCTAL 5V FCT
5V FCT 25Ω

Pinouts

CD74FCT273T, CD74FCT2273T
(QSOP, SOIC)
TOP VIEW



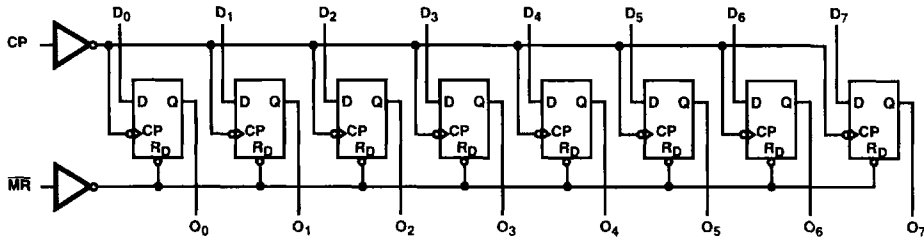
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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CD74FCT273T, CD74FCT2273T

Functional Block Diagram



TRUTH TABLE (NOTE 1)

MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

NOTE:

- H = High Voltage Level
 - h = HIGH Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
 - L = Low Voltage Level
 - l = LOW Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
 - X = Don't Care
 - ↑ = LOW-to-HIGH Clock Transition

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
D_0 - D_7	Data Inputs
O_0 - O_7	Data Outputs
GND	Ground
V_{CC}	Power

CD74FCT273T, CD74FCT2273T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
 SOIC Package 87
 QSOP Package 110
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±5%						
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0	- V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.3	0.50 V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA (25Ω Series)	-	0.3	0.50 V
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	- V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8 V
Input HIGH Current	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	1 μA
Input LOW Current	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	-1 μA
High Impedance Output Current	I _{OZH}	V _{CC} = Max	V _{OUT} = 2.7V	-	-	1 μA
	I _{OZL}		V _{OUT} = 0.5V	-	-	-1 μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2 V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 5), V _{OUT} = GND		-60	-120	- mA
Power Down Disable	I _{OFF}	V _{CC} = GND, V _{OUT} = 4.5V		-	-	100 μA
Input Hysteresis	V _H			-	200	- mV
CAPACITANCE T _A = 25°C, f = 1MHz						
Input Capacitance (Note 6)	C _{IN}	V _{IN} = 0V		-	6	10 pF
Output Capacitance (Note 6)	C _{OUT}	V _{OUT} = 0V		-	8	12 pF
POWER SUPPLY SPECIFICATIONS						
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500 μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 7)	-	0.5	2.0 mA
Supply Current per Input per MHz (Note 8)	I _{CCD}	V _{CC} = Max, Outputs Open MR = V _{CC} , One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	0.15	0.25 mA/ MHz

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OCTAL 5V FCT
5V FCT 25Ω

CD74FCT273T, CD74FCT2273T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4)	MAX	UNITS
					TYP		
Total Power Supply Current (Note 10)	I _C	V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle One Bit Toggling at f _i = 5MHz	V _{IN} = V _{CC} V _{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle Eight Bits Toggling at f _i = 2.5MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	6.0	16.3 (Note 9)	mA

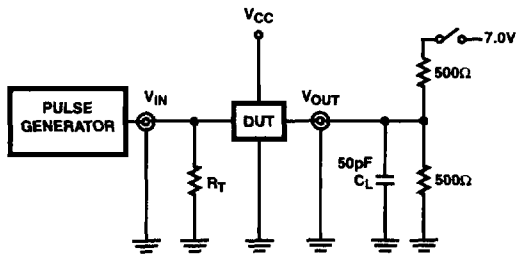
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		DT (NOTE 14)		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Propagation Delay CP to On	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.8	2.0	4.4	ns
Propagation Delay MR to On	t _{PHL} , t _{PLH}	C _L = 50pF R _L = 500Ω	2.0	13.0	2.0	7.2	2.0	6.1	2.0	5.0	ns
Setup Time, HIGH or LOW D _N to CP	t _{SU}	C _L = 50pF R _L = 500Ω	3.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time, HIGH or LOW D _N to CP	t _H	C _L = 50pF R _L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
CP Pulse Width HIGH or LOW (Note 13)	t _W	C _L = 50pF R _L = 500Ω	7.0	-	6.0	-	6.0	-	3.0	-	ns
MR Pulse Width LOW (Note 13)	t _W	C _L = 50pF R _L = 500Ω	7.0	-	6.0	-	6.0	-	3.0	-	ns
Recovery Time MR to CP (Note 13)	t _{REM}	C _L = 50pF R _L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter guaranteed but not production tested.
14. Suffix DT applies to CD74FCT273T type only.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$. $Z_{OUT} \leq 50\Omega$;
 $t_i, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

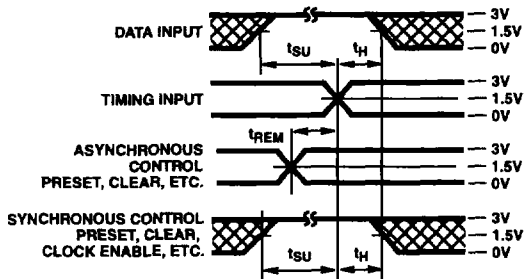


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

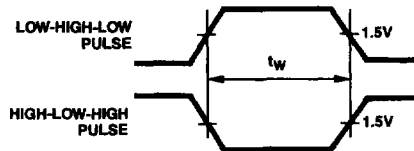


FIGURE 3. PULSE WIDTH

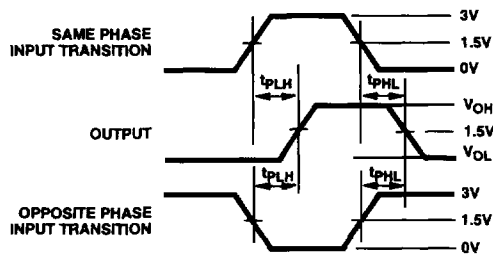


FIGURE 4. PROPAGATION DELAY

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 OCTAL 5V FCT
 5V FCT 25Ω