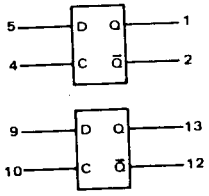
DUAL R-S FLIP-FLOPS WITH SINGLE RAIL INPUT AND POSITIVE CLOCK

MC1033
MC1233

Two dc storage flip-flops with a negative clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state. It may be teamed with the MC1016/MC1216 for shift register functions with a minimum number of packages.

POSITIVE LOGIC

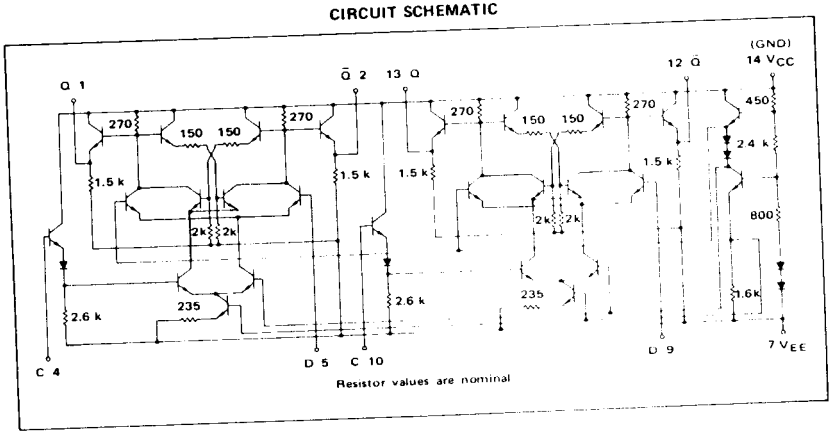


TRUTH TABLE

D	C	Q^{n+1}
0	1	Q^n
1	1	Q^n
0	0	0
1	0	1

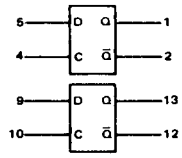
DC Input Loading Factor: C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typ

CIRCUIT SCHEMATIC



Resistor values are nominal

226



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1233 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1033 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		5	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		5	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs																
Propagation Delay	t_{4-1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	7.0	9.5	ns
	t_{4-1-}	1	5.0	10	5.0	10	7.0	12		5.0	10	5.0	10	6.0	11	
	t_{4-2+}	2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{4-2-}	2	6.0	10	6.0	10	8.0	12		6.0	10	6.0	10	7.0	11	
Rise Time	t_{1+}	1	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
	t_{2+}	2	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set Inputs																
Propagation Delay	t_{5+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
	t_{5-1-}	1	↓	↓	↓	↓	7.0	10.5		↓	↓	↓	↓	↓	↓	
	t_{5+2-}	2	↓	↓	↓	↓	7.0	10.5		↓	↓	↓	↓	↓	↓	
	t_{5-2+}	2	↓	↓	↓	↓	6.0	9.5		↓	↓	↓	↓	↓	↓	
Rise Time	t_{1+}	1	↓	7.5	↓	7.5	↓	9.0		↓	7.5	↓	7.5	↓	8.0	
	t_{2+}	2	↓	7.5	↓	7.5	↓	9.0		↓	7.5	↓	7.5	↓	8.0	
Fall Time	t_{1-}	1	↓	8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	
	t_{2-}	2	↓	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	10	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

227

@Test Temperature		TEST VOLTAGE/CURRENT VALUES					
		Vdc ±1.0%				mAdc	
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	
MC1233	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
MC1033	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ max}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 7, 9	-	14
Input Current	I_{in}	4	-	-	4	5, 7, 9, 10	-	14
		5	-	-	5	4, 7, 9, 10	-	14
Input Leakage Current	I_R	4	-	-	-	4, 5, 7, 9, 10	-	14
		5	-	-	-	4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	4	5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	V_{OL}	1	4, 5	-	-	7, 9, 10	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	4, 5	-	-	7, 9, 10	2	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	4	5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3)			$V_{IL\ max}$ +1.2 Vdc	Pulse In	Pulse Out	V_{EE} = −4.0 Vdc		(+1.2V)
Clock Inputs								
Propagation Delay	t_{4-1+}	1	4	-	1	7, 9, 10	-	14
	t_{4-1-}	1	↓	-	1	↓	-	↓
	t_{4-2+}	2		-	2		-	
	t_{4-2-}	2		-	2		-	
Rise Time	t_{1+}	1		-	1		-	
	t_{2+}	2		-	2		-	
Fall Time	t_{1-}	1		-	1		-	
	t_{2-}	2	↓	-	2	↓	-	↓
Set Inputs								
Propagation Delay	t_{5+1+}	1	5	4	1	7, 9, 10	-	14
	t_{5-1-}	1	↓	↓	1	↓	-	↓
	t_{5+2-}	2			2		-	
	t_{5-2+}	2			2		-	
Rise Time	t_{1+}	1			1		-	
	t_{2+}	2			2		-	
Fall Time	t_{1-}	1			1		-	
	t_{2-}	2	↓	↓	2	↓	-	↓

228

APPLICATIONS INFORMATION

The MC1033/MC1233 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.

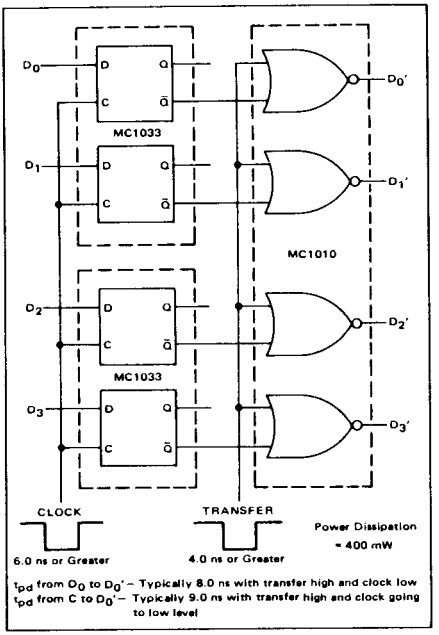


FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

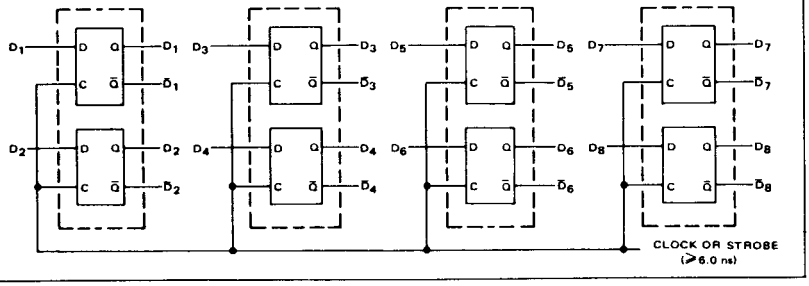
FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)

TRUTH TABLE

D	C	Q^{n+1}	$\bar{Q}^{n+1}$
ϕ	1	Q^n	$\bar{Q}^n$
0	0	0	1
1	0	1	0

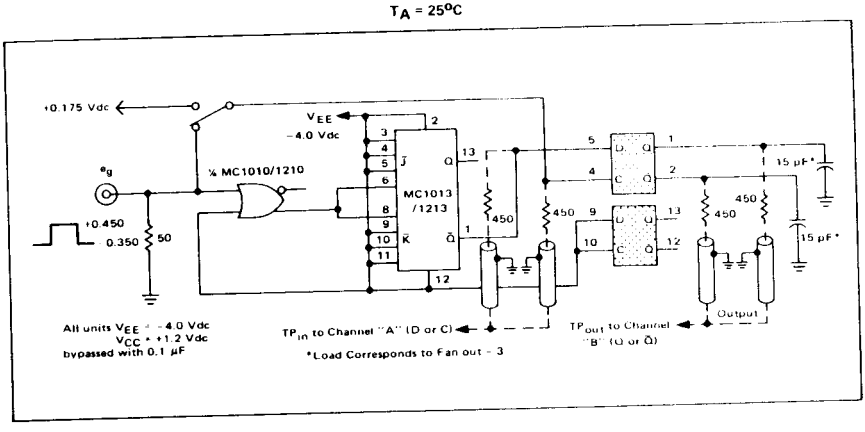
ϕ = Either state may be present

t_{pd} from D_{in} to Q or $\bar{Q} \approx 4.0$ ns
t_{pd} from C_{in} to Q or $\bar{Q} \approx 6.0$ ns

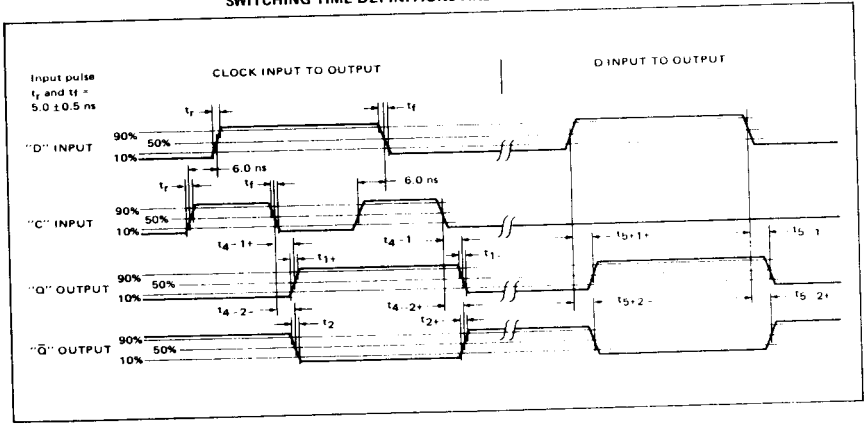


229

SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



230