HARRIS SEMICONDUCTOR

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T

January 1998

Fast CMOS 18-Bit Registers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16823T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162823T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162H823T
  - Bus Hold Retains Last Active Bus State During Three-State
  - Eliminates the Need for External Pull-Up Resistors

Description

These devices are 18-bit wide registers with clock enable ($_X\overline{CLKEN}$) and clear ($_X\overline{CLR}$) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16823T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162823T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H823T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H823ETSM	-40 to 85	56 Ld SSOP	M56.300-P

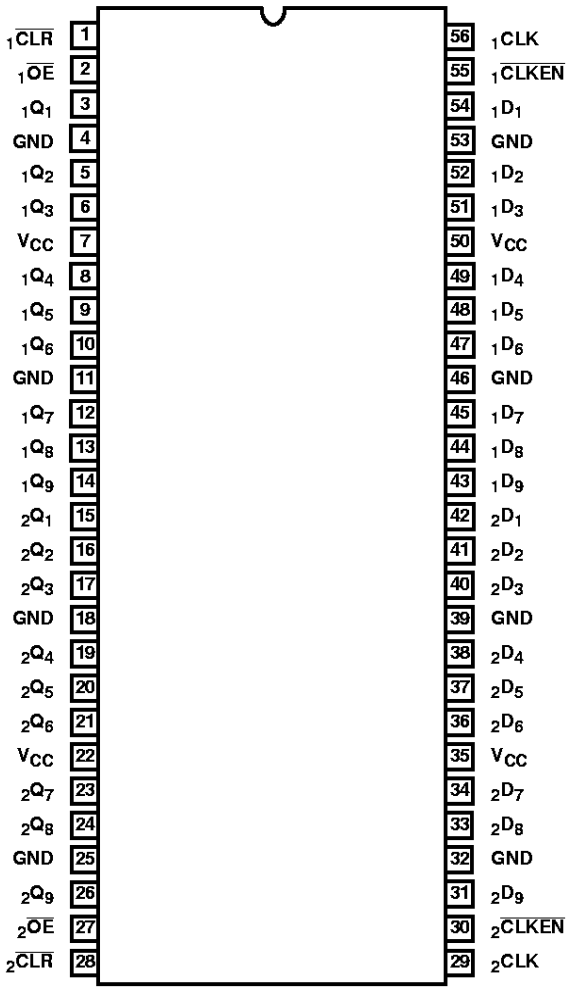
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

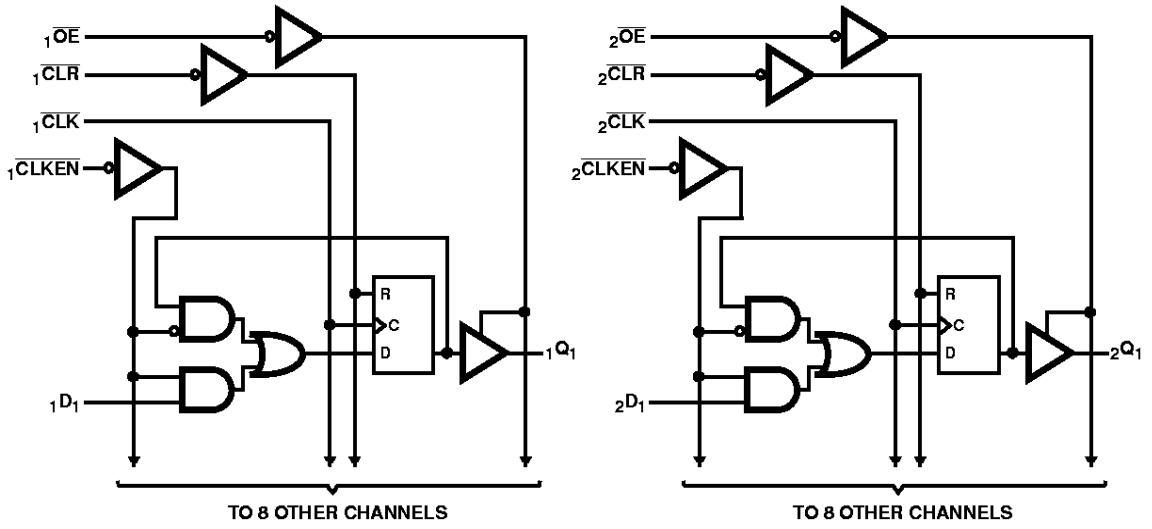
File Number 4189.3

Pinout

CD74FCT16823T, CD74FCT162823T, CD74FCT162H823T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS
	$_X\overline{OE}$	$_X\overline{CLR}$	$_X\overline{CLKEN}$	$_X$CLK	$_XD_X$	$_XQ_X$
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q (Note 2)
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before indicated steady-state input conditions were established.

Pin Descriptions

PIN NAME	DESCRIPTION
$_XD_X$	Data Inputs (Note 3)
$_X$CLK	Clock Inputs
$_X\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$_X\overline{CLR}$	Asynchronous Clear Inputs (Active LOW)
$_X\overline{OE}$	Output Enable Inputs (Active LOW)
$_XQ_X$	Three-State Outputs

NOTE:

3. For the CD74FCT162H823T, these pins have “Bus Hold”. All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}, I_{BHL}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
CD74FCT162823T, CD74FCT162H823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $_X\overline{OE}$ = $_X\overline{CLKEN}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $_X\overline{OE}$ = $_X\overline{CLKEN}$ = GND f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $_X\overline{OE}$ = $_X\overline{CLKEN}$ = GND 18 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	4.2	7.1 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	9.2	22.1 (Note 13)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT (NOTE 16) MIN	AT MAX	BT (NOTE 16) MIN	BT MAX	CT (NOTE 16) MIN	CT MAX	DT (NOTE 16) MIN	DT MAX	ET (NOTE 16) MIN	ET MAX	UNITS
Propagation Delay $_X$CLK to $_XQ_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		C_L = 300 pF (Note 17) R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
Propagation Delay $_X\overline{CLR}$ to $_XQ_X$	t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
Output Enable Time $_X\overline{OE}$ to $_XQ_X$	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		C_L = 300pF (Note 17) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns

Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
Output Disable Time (Note 17) $_XOE$ to $_XQ_X$	t_{PHZ}, t_{PLZ}	C_L = 5pF (Note 17) R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
Setup Time HIGH or LOW, $_XD_X$ to $_X$CLK	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	3.0	-	1.5	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_X$CLK	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	0	-	ns
Setup Time HIGH or LOW, $_X\overline{CLKEN}$ to $_X$CLK	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	3.0	-	2.5	-	ns
Hold Time HIGH or LOW, $_X\overline{CLKEN}$ to $_X$CLK	t_H	C_L = 50pF R_L = 500Ω	2.0	-	0	-	0	-	0	-	0	-	ns
$_X$CLK Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
$_X\overline{CLR}$ Pulse Width LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Recovery Time (Note 17) $_X\overline{CLR}$ to $_X$CLK	t_{REM}	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Output Skew (Note 18)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. Pins with Bus Hold are identified in the pin description.
9. This specification does not apply to bidirectional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.