Am25S09

Quad Two-Input, High-Speed Register

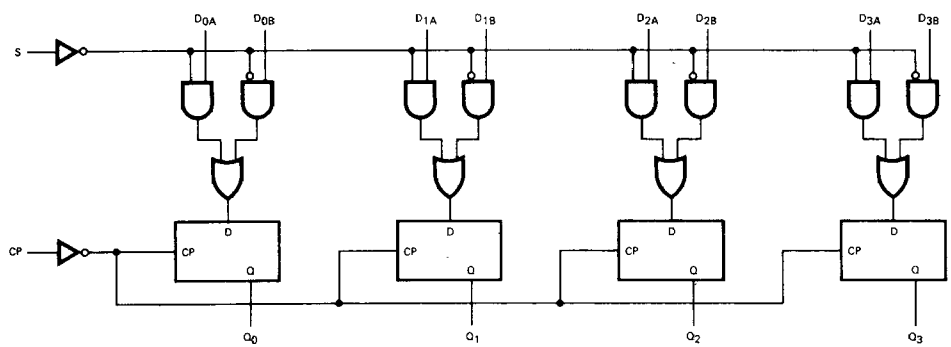
DISTINCTIVE CHARACTERISTICS

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge-triggered clock action
- High-speed Schottky technology.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

GENERAL DESCRIPTION

The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

BLOCK DIAGRAM



BD001500

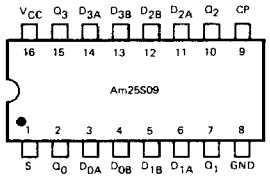
RELATED PRODUCTS

Part No.	Description
Am25LS09	Low Power Version
Am25S07/08	6/4-Bit Register
Am25LS07/08	6/4-Bit Low Power Register

03700B

Refer to Page 13-1 for Essential Information on Military Devices

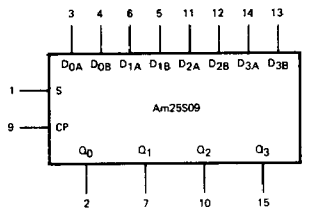
CONNECTION DIAGRAM
Top View



CD001700

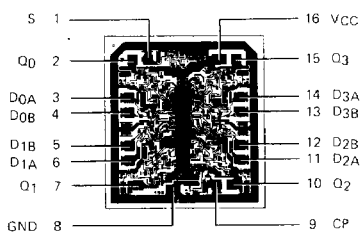
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000610

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.067" x 0.073"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S09 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S09** — Device type
  - Quad Two-Input, High-Speed Register

Valid Combinations	
Am25S09	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

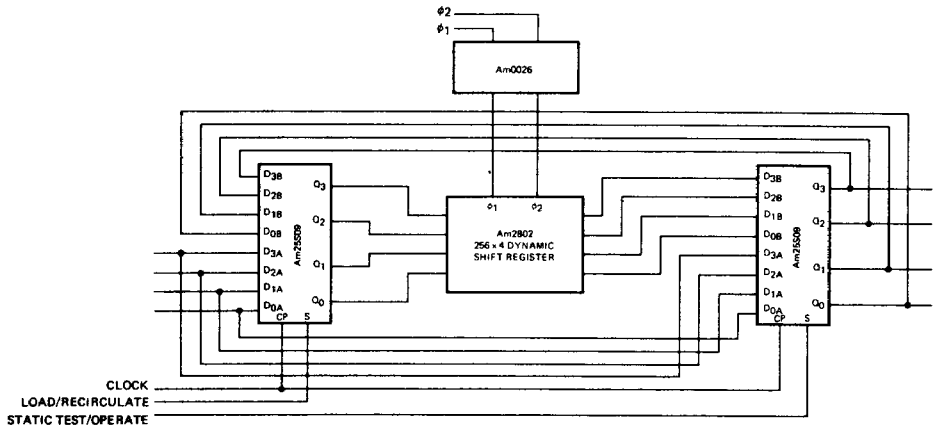
Pin No.	Name	I/O	Description
3 6 11 14	D_{0A}, D_{1A}, D_{2A}, D_{3A}	I	The "A" word into the two-input multiplexer of the D flip-flops.
4 5 12 13	D_{0B}, D_{1B}, D_{2B}, D_{3B}	I	The "B" word into the two-input multiplexer of the D flip-flops.
2,7 10,15	Q_0, Q_1, Q_2, Q_3	O	The outputs of the four D-type flip-flops of the register.
1	S	I	Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH, the B word is applied to the D inputs of the flip-flops.
9	CP	I	Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{IA}	INPUTS D_{IB}	OUTPUT Q_I
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

APPLICATIONS



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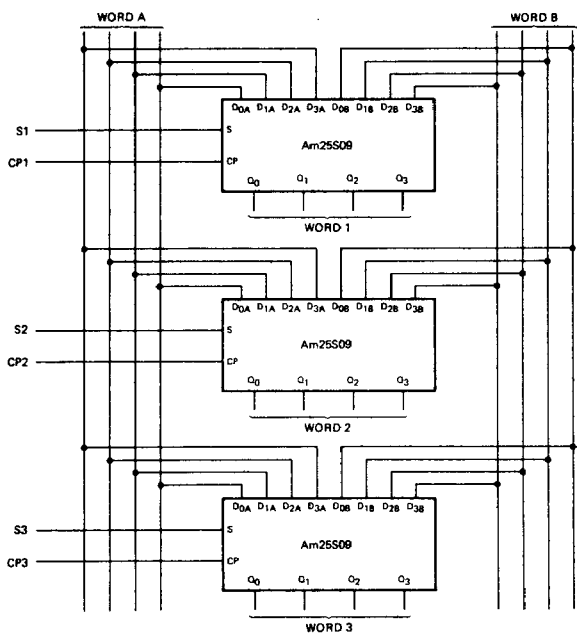
Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



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Am25S09 used to store a word from either data bus A or data bus B.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH Voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input Load Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 5)			75	120	mA

Notes:
1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C)

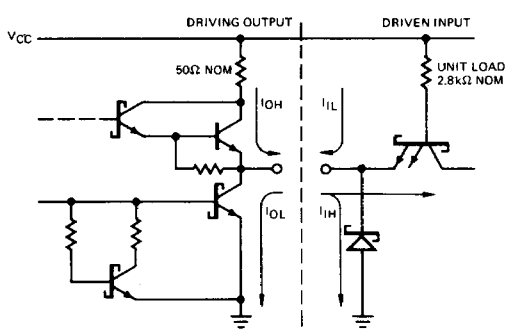
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q HIGH	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		8	12	ns
t_{PHL}	Clock to Q LOW			11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data Set-up Time		5.5			ns
t_s	Select Input Set-up Time		10			ns
t_h	Data Hold Time		3			ns
t_h	Select Input Hold Time		3			ns

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
S	1	1	–	–
Q_0	2	–	20	10
D_{0A}	3	1	–	–
D_{0B}	4	1	–	–
D_{1B}	5	1	–	–
D_{1A}	6	1	–	–
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
D_{2A}	11	1	–	–
Q_{2B}	1	1	–	–
D_{3B}	13	1	–	–
D_{3A}	14	1	–	–
Q_3	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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Note: Actual current flow direction shown