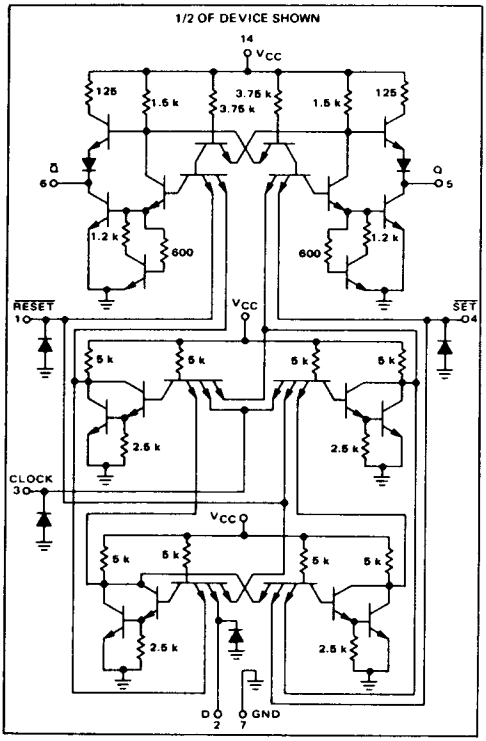
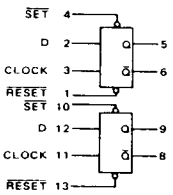
DUAL TYPE D FLIP-FLOP

MTTL MC7400P series
MTTL MC5400L/7400L series

MC5479L*
MC7479P,L*



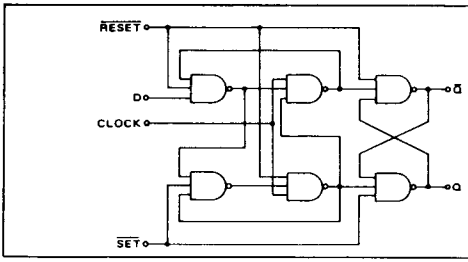
This dual type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.



t_n	t_{n+1}	
D	Q	Q̄
0	0	1
1	1	0

Input Loading Factor:
D = 1
$\overline{SET}$, CLOCK = 2
$\overline{RESET}$ = 3
Output Loading Factor = 10
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 16 ns typ
Operating Frequency = 30 MHz typ

*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 606)
See General Information section for package outline dimensions.



LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

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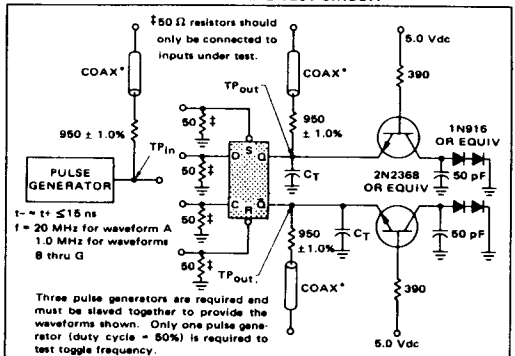
OPERATING CHARACTERISTICS

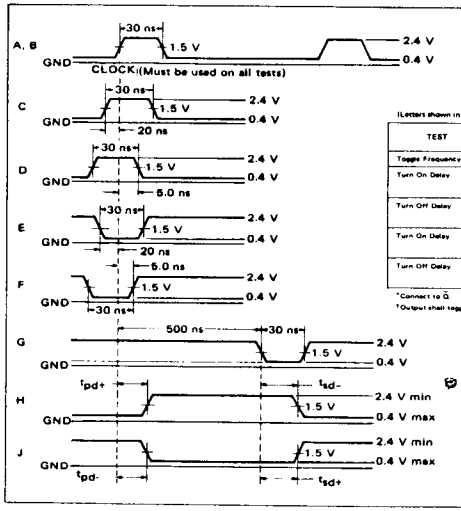
Data may be applied to the D input any time following 5.0 ns after the leading edge of a clock pulse and 20 ns before the leading edge of the following clock pulse. The state of the D input when the clock changes from the positive logic "0" state to the positive logic "1" state is transferred to the Q output of the flip-flop. The data input cannot be changed between the setup time (20 ns) and the hold time (5.0 ns) without adversely affecting the operation of the flip-flop.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs override the clock, and may be applied any time during the operating cycle.

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

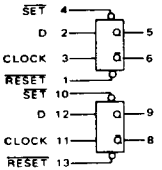
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT C	INPUT D	INPUT $\overline{R}$	INPUT $\overline{S}$	Q	Q̄	LIMITS Min	LIMITS Max	LIMITS Unit
Toggle Frequency	f_{Tog}	A	*	2.4 V	2.4 V	†	†	20	–	MHz
Turn On Delay Q̄	t_{pd-}	B	C	G	2.4 V	H	J	–	30	ns
Turn On Delay Q		B	E	2.4 V	G	J	H	–	30	ns
Turn Off Delay Q̄	t_{pd+}	B	E	2.4 V	G	J	H	–	30	ns
Turn Off Delay Q		B	C	G	2.4 V	H	J	–	30	ns
Turn On Delay Q̄	t_{sd-}	B	F	2.4 V	G	J	H	–	25	ns
Turn On Delay Q		B	D	G	2.4 V	H	J	–	25	ns
Turn Off Delay Q̄	t_{sd+}	B	D	G	2.4 V	H	J	–	25	ns
Turn Off Delay Q		B	F	2.4 V	G	J	H	–	25	ns

*Connect to Q̄.
†Output shall toggle with each input pulse.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA		Volts								
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
MC5479	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.5	5.5
MC7479	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5479 Test Limits −55 to +125°C Min	Max	Unit	MC7479 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current D	I_F	2	-	-1.6	mAdc	-	-1.6	mAdc	-	-	2	-	-	1,4	-	-	-	-	14	3,7,11
$\overline{\text{Set}}$		4	-	-3.2		-	-3.2		-	-	4	-	-	1	-	-	-	-		2,3,7,11
$\overline{\text{Reset}}$		1	-	-4.8		-	-4.8		-	-	1	-	-	2,4	-	-	-	-		3,7,11
Clock		3	-	-3.2		-	-3.2		-	-	3	-	-	1	-	-	-	-		2,4,7,11
Leakage Current D	I_{R1}	2	-	40	μAdc	-	40	μAdc	-	-	-	2	-	3,4	-	-	-	-	14	1,7,11
$\overline{\text{Set}}$		4	-	80		-	80		-	-	-	4	-	1,2,3*	-	-	-	-		7,11
$\overline{\text{Reset}}$		1	-	120		-	120		-	-	-	1	-	3*,4	-	-	-	-		2,7,11
Clock		3	-	80		-	80		-	-	-	3	-	4	-	-	-	-		1,2,7,11
D	I_{R2}	2	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	2	3,4	-	-	-	-	14	1,7,11
$\overline{\text{Set}}$		4	-			-			-	-	-	-	4	1,2,3*	-	-	-	-		7,11
$\overline{\text{Reset}}$		1	-			-			-	-	-	-	1	3*,4	-	-	-	-		2,7,11
Clock		3	-			-			-	-	-	-	3	4	-	-	-	-		1,2,7,11
Output																				
Output Voltage	V_{OL}	5	-	0.4	Vdc	-	0.4	Vdc	5	-	-	-	-	-	4	1	-	14	-	2,3,7,11
		6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	1	4	-	14	-	2,3,7,11
	V_{OH}	5	2.4	-	Vdc	2.4	-	Vdc	-	5	-	-	-	-	1	4	-	14	-	2,3,7,11
		6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	4	1	-	14	-	2,3,7,11
Short-Circuit Current	I_{SC}	5	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	14	4,5,7,11
		6	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,6,7,11
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	14	-	28.8	mAdc	-	28.8	mAdc	-	-	-	-	-	-	-	-	14	-	-	2,3,4,7,10,11,12
		14	-	28.8	mAdc	-	28.8	mAdc	-	-	-	-	-	-	-	-	14	-	-	1,2,3,7,11,12,13

*Momentarily ground pin prior to taking measurement, then set to state indicated.