

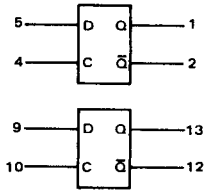
DUAL R-S FLIP-FLOPS
WITH SINGLE RAIL INPUT
AND NEGATIVE CLOCK

MECL II MC1000/1200 series

MC1016
MC1216

Two dc storage flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state.

POSITIVE LOGIC

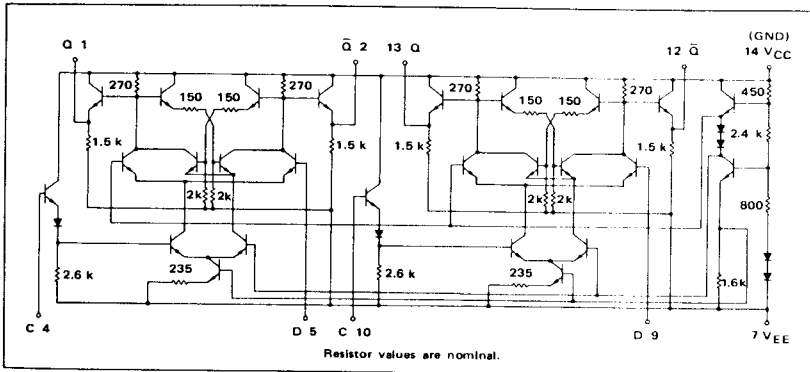


DC Input Loading Factor : C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

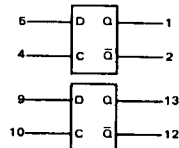
TRUTH TABLE

D	C	Q ⁿ⁺¹
0	0	Q ⁿ
1	0	Q ⁿ
0	1	0
1	1	1

CIRCUIT SCHEMATIC



MC1016, MC1216 (continued)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1216 Test Limits								Unit	MC1016 Test Limits						Unit
			-55°C		+25°C		+125°C		0°C			+25°C		+75°C				
			Min	Max	Min	Max	Min	Max	Min	Max		Min	Max	Min	Max			
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	-	mAdc	-	-	-	36	-	-	mAdc	
Input Current	I_{in}	4	-	-	-	100	-	-	-	μ Adc	-	-	-	100	-	-	μ Adc	
		5	-	-	-	150	-	-	-	μ Adc	-	-	-	150	-	-	μ Adc	
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	-	μ Adc	-	-	-	0.2	-	1.0	μ Adc	
		5	-	-	-	0.2	-	1.0	-	μ Adc	-	-	-	0.2	-	1.0	μ Adc	
"Q" Logical "1" Output Voltage ¹	V_{OH}	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	-	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	-	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
"Q-bar" Logical "1" Output Voltage ¹	V_{OH}	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	-	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"Q-bar" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	-	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max			Typ	Max	Typ	Max	Typ	Max		
Clock Inputs	Propagation Delay	t_{4+1-}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	ns	
		t_{4+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5		5.0	8.0	5.0	8.0	5.0	8.5		
		t_{4+2-}	2	5.0	8.0	5.0	8.0	6.0	9.5		5.0	8.0	5.0	8.0	5.0	8.5		
		t_{4+2+}	2	6.0	9.0	6.0	9.0	7.0	10.5		6.0	9.0	6.0	9.0	6.0	9.5		
Rise Time	t_{1-}	1	5.0	7.5	5.0	7.5	6.0	8.5		5.0	7.5	5.0	7.5	5.0	8.0			
		2	5.0	7.5	5.0	7.5	6.0	8.5		5.0	7.5	5.0	7.5	5.0	8.0			
Fall Time	t_{1-}	1	6.0	8.5	6.0	8.5	7.0	10.5		6.0	8.5	6.0	8.5	6.0	9.5			
		2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5			
Set Inputs	Propagation Delay	t_{5+1-}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns	
		t_{5-1-}	1					7.0	10.5									
		t_{5+2-}	2					7.0	10.5									
		t_{5-2+}	2					6.0	9.5									
Rise Time	t_{1+}	1		7.5		7.5		9.0			7.5		7.5		8.0			
		2		7.5		7.5		9.0			7.5		7.5		8.0			
Fall Time	t_{1-}	1		8.5	6.0	8.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10			
		2		8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10			

¹ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

@Test Temperature
 MC1216 { -55°C
 +25°C
 +125°C
 MC1016 { 0°C
 +25°C
 +75°C

TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					
V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	mAdc
-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-	-2.5
-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-	-2.5
-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-	-2.5
-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	V _{CC} (Gnd)
Power Supply Drain Current	-	4, 10	-	5, 7, 9	-	14
Input Current	-	-	4, 5	5, 7, 9, 10, 7, 9, 10	-	14
Input Leakage Current	-	-	-	4, 5, 7, 9, 10, 4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage†	-	4, 5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	5	4	-	7, 9, 10	-	14
"Q" Logical "1" Output Voltage†	5	4	-	7, 9, 10	2	14
"Q" Logical "0" Output Voltage	-	4, 5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3) Clock Inputs Propagation Delay	Pulse In	V _{IH min} +1.2 Vdc	Pulse Out	V _{EE} = -4.0 Vdc		(+1.2V)
Rise Time	4	-	1	7, 9, 10	-	14
	↓	-	1	↓	-	↓
	-	-	2	-	-	-
	-	-	2	-	-	-
	-	-	2	-	-	-
Fall Time	↓	-	1	↓	-	↓
	-	-	2	-	-	-
Set Inputs Propagation Delay	5	4	1	7, 9, 10	-	14
Rise Time	↓	↓	1	↓	-	↓
	-	-	1	-	-	-
	-	-	2	-	-	-
	-	-	2	-	-	-
	-	-	2	-	-	-
Fall Time	↓	↓	1	↓	-	↓
	-	-	2	-	-	-

APPLICATIONS INFORMATION

The MC1016/MC1216 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.

FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

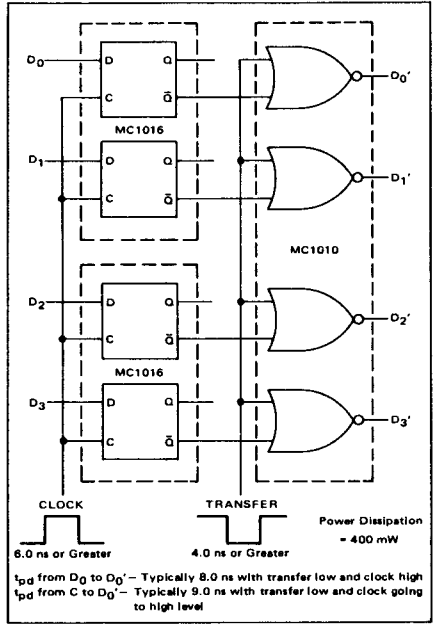
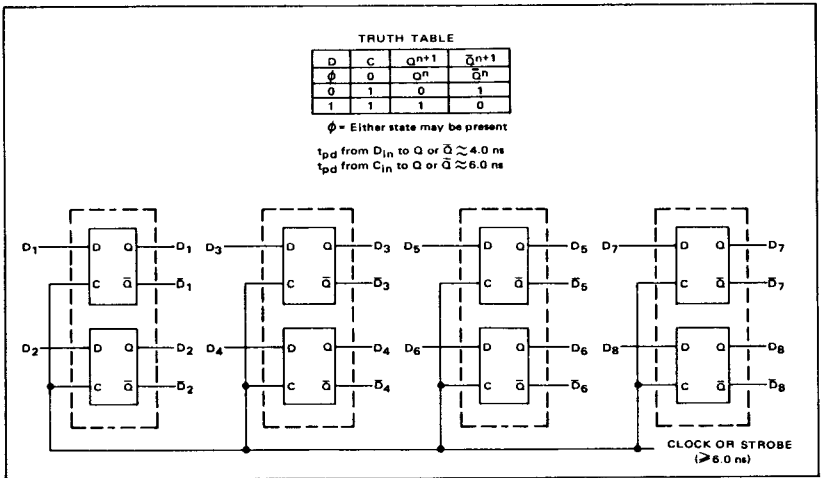
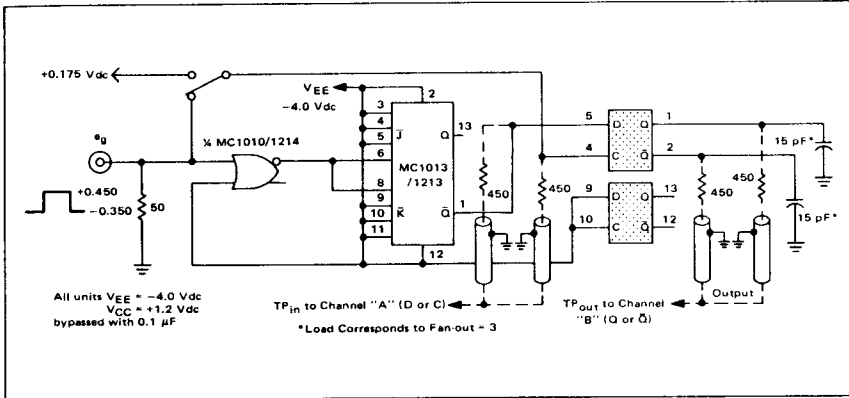


FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)



MC1016, MC1216 (continued)

SWITCHING TIME TEST CIRCUIT
 $T_A = 25^\circ\text{C}$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

