

January 1998

Fast CMOS 20-Bit Buffers
Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16827T
 - High Output Drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
 - Power Off Disable Outputs Permit "Live Insertion"
 - Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$
- CD74FCT162827T
 - Balanced Output Drivers: $\pm 24mA$
 - Reduced System Switching Noise
 - Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$
- CD74FCT162H827T
 - Bus Hold Retains Last Active Bus State During Three-State
 - Eliminates the Need for External Pull-Up Resistors

Description

These devices are 20-bit wide bus drivers designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the devices to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16827T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162827T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H827T has "Bus Hold" which retains the input's last state whenever the input goes to high impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

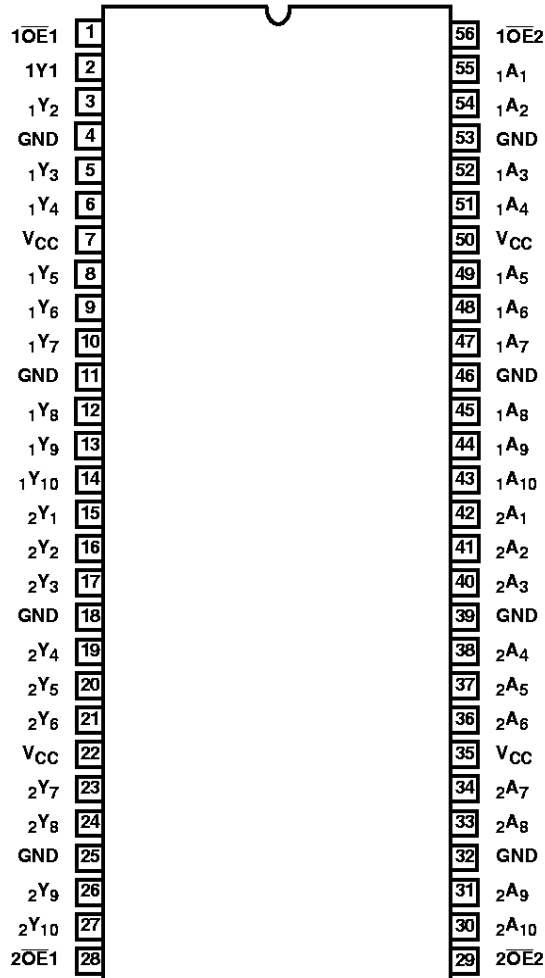
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
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CD74FCT162827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H827ETSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

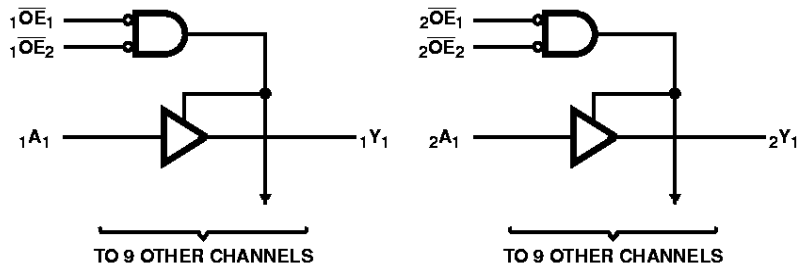
CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T

Pinout

CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$\overline{xOE_1}$	$\overline{xOE_2}$	xAX	xYX
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{xOE_x}$	Output Enable Inputs (Active LOW)
xAX	Data Inputs (Note 2)
xYX	Three-State Outputs

NOTE:

2. For the CD74FCT162H827T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
 TSSOP Package 85
 SSOP Package 70
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%						
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level	2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level	-	-	0.8	V
Input HIGH Current	I _{IH}	Standard Input, V _{CC} = Max V _{IN} = V _{CC}	-	-	1	μA
Input HIGH Current	I _{IH}	Standard I/O, V _{CC} = Max V _{IN} = V _{CC}	-	-	1	μA
Input HIGH Current	I _{IH}	Bus Hold Input (Note 7) V _{CC} = Max V _{IN} = V _{CC}	-	-	±100	μA
Input HIGH Current	I _{IH}	Bus Hold I/O (Note 7) V _{CC} = Max V _{IN} = V _{CC}	-	-	±100	μA
Input LOW Current	I _{IL}	Standard Input, V _{CC} = Min V _{IN} = GND	-	-	-1	μA
Input LOW Current	I _{IL}	Standard I/O, V _{CC} = Min V _{IN} = GND	-	-	-1	μA
Input LOW Current	I _{IL}	Bus Hold Input (Note 7) V _{CC} = Min V _{IN} = GND	-	-	±100	μA
Input LOW Current	I _{IL}	Bus Hold I/O (Note 7) V _{CC} = Min V _{IN} = GND	-	-	±100	μA
Bus Hold Sustain Current	I _{BHH}	Bus Hold Input (Note 7) V _{CC} = Min	V _{IN} = 2.0V	-50	-	μA
	I _{BHL}		V _{IN} = 0.8V	50	-	μA
High Impedance Output Current (Three-State) (Note 8)	I _{OZH}	V _{CC} = Max V _{OUT} = 2.7V	-	-	1	μA
	I _{OZL}	V _{CC} = Max V _{OUT} = 0.5V	-	-	-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA	-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 6), V _{OUT} = GND	-80	-140	-200	mA
Output Drive Current	I _O	V _{CC} = Max (Note 6), V _{OUT} = 2.5V	-50	-	-180	mA
Input Hysteresis	V _H		-	100	-	mV

CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
CD74FCT16827T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0mA	2.5	3.5	-	V
			I _{OH} = -15.0mA	2.4	3.5	-	V
			I _{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I _{OFF}	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		-	-	±100	μA
CD74FCT162827T, CD74FCT162H240T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I _{ODL}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I _{ODH}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C _{IN}	V _{IN} = 0V	-	4.5	6		pF
Output Capacitance (Note 9)	C _{OUT}	V _{OUT} = 0V	-	5.5	8		pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 10)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 12)	I _{CCD}	V _{CC} = Max, Outputs Open OE1 = OE2 = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	60	100	μA/MHz
Total Power Supply Current (Note 13)	I _C	V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle OE1 = OE2 = GND f _I = 5MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE1 = OE2 = GND 8 Bits Toggling f _I = 2.5MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	3.0	5.5 (Note 12)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	8.0	20.5 (Note 12)	mA

CD74FCT16827T, CD74FCT162827T, CD74FCT162H827T

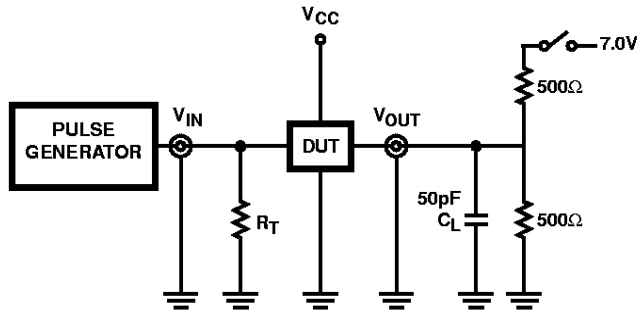
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $X_A X$ to $X Y X$	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	8.0	1.5	5.0	1.5	4.4	1.5	3.8	1.5	3.2	ns
		$C_L = 300\text{pF}$ (Note 15) $R_L = 500\Omega$	1.5	15.0	1.5	13.0	1.5	10.0	1.5	7.5	1.5	7.0	ns
Output Enable Time $X \overline{O}E_X$ to $X Y X$	$t_{PZH},$ t_{PZL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	5.0	1.5	4.8	ns
		$C_L = 300\text{pF}$ (Note 16) $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	14.0	1.5	9.0	1.5	9.0	ns
Output Disable Time (Note 16) $\overline{O}E_N$ to Y_N	$t_{PHZ},$ t_{PLZ}	$C_L = 5\text{pF}$ $R_L = 500\Omega$	1.5	9.0	1.5	6.0	1.5	5.7	1.5	4.3	1.5	4.0	ns
		$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10.0	1.5	7.0	1.5	6.0	1.5	4.3	1.5	4.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Pins with Bus Hold are identified in the pin description.
- This specification does not apply to bidirectional functionalities with Bus Hold.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamperes and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

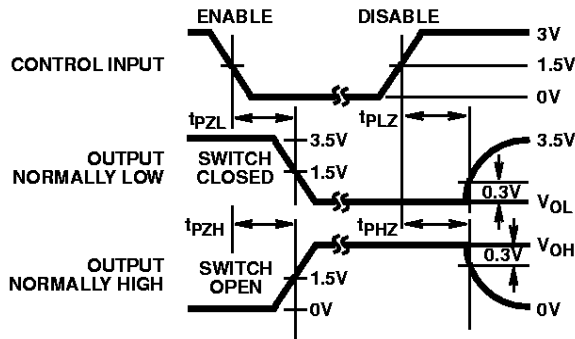


FIGURE 2. ENABLE AND DISABLE TIMING

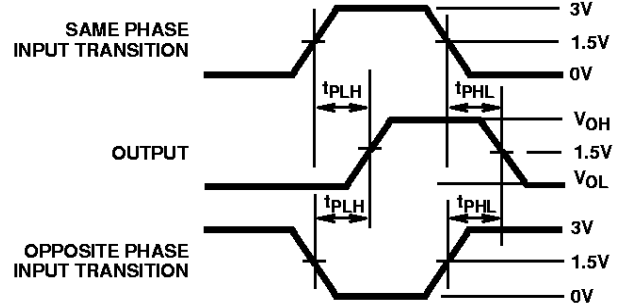


FIGURE 3. PROPAGATION DELAY

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 Singapore 1334
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