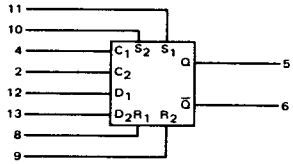
TYPE D FLIP-FLOPS

MC1022
MC1222

Designed for clocked-storage operation based on the "master-slave" principle. Operation depends only on voltage levels, therefore the shape of the clock waveform becomes unimportant in determining the state of the flip-flop. When the clock is low, the input data is stored in the "master" and is subsequently transferred to the "slave" when the clock is high, making the data available at the outputs. In this operation the "master" is disabled before the slave is enabled, due to the design of the internal threshold skew. Along with two data and two Clock inputs, the unit provides two SET and two RESET inputs that are independent of the Clock.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}	$\bar{Q}^{n+1}$
	8 or 9	10 or 11	5	6
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

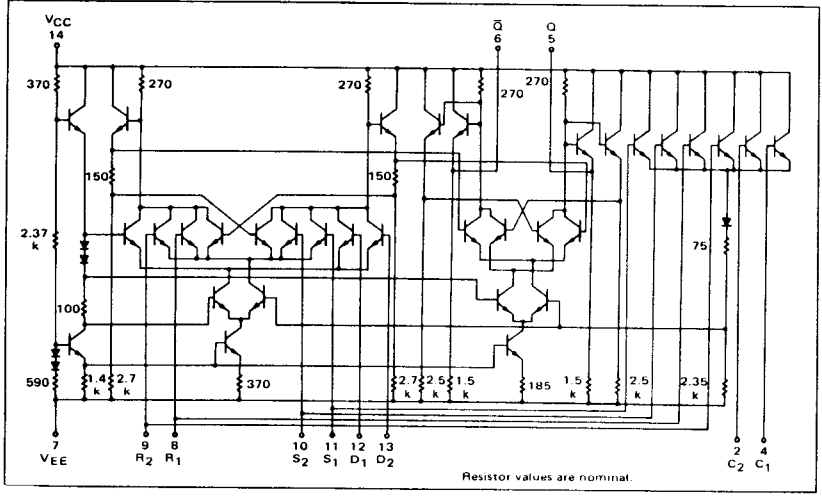
N.D. = Not Defined

CLOCKED TRUTH TABLE

Pin No	D	C	Q^{n+1}	$\bar{Q}^{n+1}$
	12 or 13	2 or 4	5	6
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

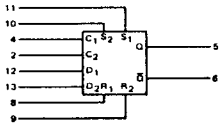
*A "1" or Clock input is defined for this flip-flop as a change in level from a low input to a high input.

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS



Characteristic	Symbol	Pin Under Test	MC1222 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1022 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	27	-	-	mAdc	-	-	-	27	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		4	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
		11	-	-	-		-	-		-	-	-		-	-	
		12	-	-	-		-	-		-	-	-		-	-	
		13	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		5†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		5†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\overline{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		6†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		6†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Input Propagation Delay	t_{2+5-}	5	8.0	12	8.0	12	11	15	ns	8.0	12	8.0	12	9.0	13	ns
	t_{2+5+}	5	7.0	11	7.0	11	12	18		7.0	11	7.0	11	9.0	13	
	t_{2+6+}	6	7.0	11	7.0	11	12	18		7.0	11	7.0	11	9.0	13	
	t_{2+6-}	6	8.0	12	8.0	12	11	15		8.0	12	8.0	12	9.0	13	
Rise Time	t_{5+}, t_{6+}	5, 6	5.0	7.5	5.0	8.5	7.0	11		5.0	8.0	5.0	8.5	6.0	9.0	
Fall Time	t_{5-}, t_{6-}	5, 6	7.0	9.5	7.0	11.5	8.0	13		7.0	10.5	7.0	11.5	8.0	12	
Set Input Propagation Delay	t_{10+5+}	5	8.0	12	8.0	13	10	22	ns	8.0	12	8.0	13	10	14	ns
	t_{10+5+}	5		12	8.0	13	10	22			12	8.0	13	10	14	
	t_{10+6-}	6		13	9.0	14	11	19			13	9.0	14	11	15	
	t_{10+6-}	6		13	9.0	14	11	19			13	9.0	14	11	15	
Reset Input Propagation Delay	t_{9+5-}	5	8.0	13	9.0	14	11	19	ns	8.0	13	9.0	14	11	15	ns
	t_{9+5-}	5		13	9.0	14	11	19			13	9.0	14	11	15	
	t_{9+6+}	6		12	8.0	13	10	22			12	8.0	13	10	14	
	t_{9+6+}	6		12	8.0	13	10	22			12	8.0	13	10	14	

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

† Output level to be measured after clock transition on pin 2 or 4 through one positive-going and one negative-going edge. (V_{IH}, V_{IL})

@Test Temperature		V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L
MC1222	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1022	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

TEST VOLTAGE/CURRENT VALUES: Vdc ± 1.0%; mAdc

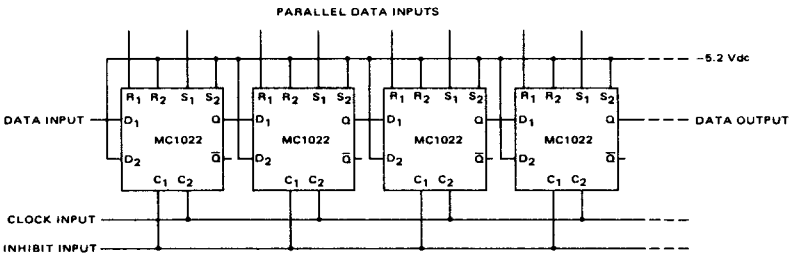
Characteristic	Symbol	Pin Under Test	V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	7	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
Input Current	I_{in}	2	-	-	2	4, 7, 8, 9, 10, 11, 12, 13	-	14
		4	-	-	4	2, 7, 8, 9, 10, 11, 12, 13	-	
		8	-	-	8	2, 4, 7, 9, 10, 11, 12, 13	-	
		9	-	-	9	2, 4, 7, 8, 10, 11, 12, 13	-	
		10	-	-	10	2, 4, 7, 8, 9, 11, 12, 13	-	
		11	-	-	11	2, 4, 7, 8, 9, 10, 12, 13	-	
		12	-	-	12	2, 4, 7, 8, 9, 10, 11, 13	-	
		13	-	-	13	2, 4, 7, 8, 9, 10, 11, 12	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-	10	-	2, 4, 7, 8, 9, 11, 12, 13	5	14
		5†	-	13	-	2, 7, 8, 9, 10, 11, 12	5	14
"Q" Logical "0" Output Voltage	V_{OL}	5	-	9	-	2, 4, 7, 8, 10, 11, 12, 13	-	14
		5†	13	-	-	4, 7, 8, 9, 10, 11, 12	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	6	-	8	-	2, 4, 7, 9, 10, 11, 12, 13	6	14
		6†	12	-	-	4, 7, 8, 9, 10, 11, 13	6	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	6	-	11	-	2, 4, 7, 8, 9, 10, 12, 13	-	14
		6†	-	12	-	2, 7, 8, 9, 10, 11, 13	-	14
Switching Times Clock Input Propagation Delay					Pulse In	V_{EE} − 4.0 Vdc	Pulse Out	(+1.2Vdc)
	t_{2+5-}	5	-	-	2	4,7,8,9,10,11,12,13	5	14
	t_{2+5+}	5	-	-			5	
	t_{2+6+}	6	-	-			6	
	t_{2+6-}	6	-	-			6	
Rise Time	t_{5+}, t_{6+}	5, 6	-	-			5,6	
Fall Time	t_{5-}, t_{6-}	5, 6	-	-			5,6	
Set Input Propagation Delay	t_{10+5+}	5	-	2	10	4,7,8,11,12,13	5	14
	t_{10+5+}	5	2	-			5	
	t_{10+6-}	6	-	2			6	
	t_{10+6-}	6	2	-			6	
Reset Input Propagation Delay	t_{9+5-}	5	-	2	9	4,7,8,11,12,13	5	14
	t_{9+5-}	5	2	-			5	
	t_{9+6+}	6	-	2			6	
	t_{9+6+}	6	2	-			6	

APPLICATIONS INFORMATION

The MC1022/MC1222 single-phase Type D flip-flop offers advantages over the J-K flip-flop in applications such as single-rail operation. Since a true master-slave design is utilized, the input data may be asynchronous. There is no chance of data "rippling through" if the clock is in the low state. The SET and RESET inputs are also completely independent of the clock and will override the clock, setting both the master and the slave portions of the flip-flop. All the logic inputs are duplicated and ORed together internally, giving additional flexibility.

A low-level clock state (logic "0") allows information to be transferred to the master portion of the flip-flop through a "D" input. The master will continuously update itself to changing data as long as the clock is at a low level. When the clock goes to the high level, the master is disabled and the data transferred to the slave, thereby becoming available at the outputs. The thresholds of the master and slave portions of the flip-flop are internally offset to give a "raceless" flip-flop (i.e., the master is disabled before the slave is enabled, and vice versa). Thus the flip-flop operation is independent of the rise and fall times of the clock waveforms.

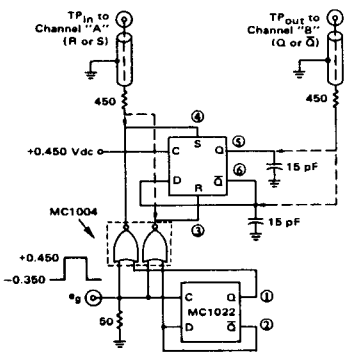
50 MHz SHIFT REGISTER



Unused inputs should be returned to V_{EE}.

A "1" level on the Inhibit input may be used to stop the shifting of data through the register. Parallel data may be brought into the register asynchronously since SET or RESET data internally inhibits the clock.

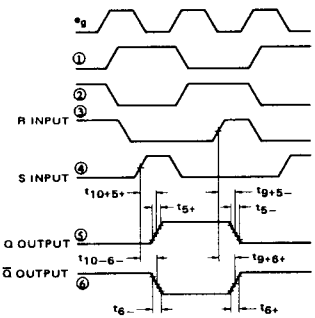
SWITCHING TIME TEST CIRCUIT (T_A = 25°C)



All Units V_{EE} = −4.0 Vdc, V_{CC} = +1.2 Vdc } bypassed with 0.1 μF

Unused inputs returned to V_{EE}.

SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



Switching time test circuit and waveforms give method of test with input pulses on pins 9 or 10 and output pulses on pins 5 and 6. Other tests specified and other combinations are tested in same manner and will meet limits specified.