HARRIS SEMICONDUCTOR

CD74FCT564, CD74FCT574

BiCMOS FCT Interface Logic, Octal D-Type Flip-Flops, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 5.6ns at V_{CC} = 5V, T_A = 25°C
- Positive Edge Triggered
- CD74FCT564
  - Inverting
- CD74FCT574
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT564 and CD74FCT574 are octal D-Type, three-state, positive edge triggered flip-flops which use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the three state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The CD74FCT564 and CD74FCT574 share the same configurations; the CD74FCT564, however, has inverted outputs and the CD74FCT574 has noninverted outputs.

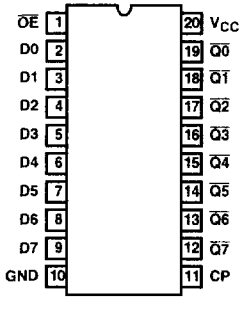
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT564E	0 to 70	20 Ld PDIP	E20.3
CD74FCT574E	0 to 70	20 Ld PDIP	E20.3
CD74FCT564M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574SM	0 to 70	20 Ld SSOP	M20.209

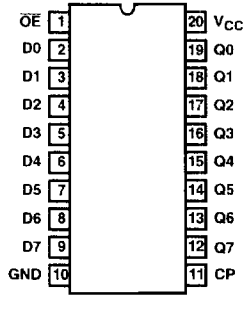
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT564
(PDIP, SOIC, SSOP)
TOP VIEW



CD74FCT574
(PDIP, SOIC, SSOP)
TOP VIEW

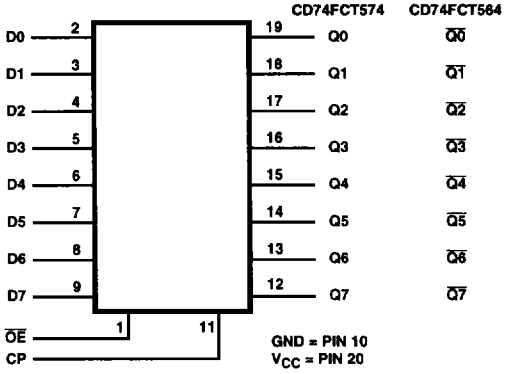


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2295.2**

Functional Diagram



TRUTH TABLE (NOTE 1)

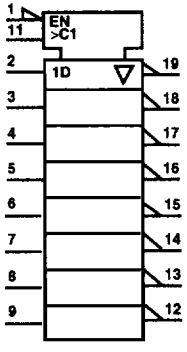
INPUTS			OUTPUTS	
			CD74FCT564	CD74FCT574
$\overline{OE}$	CP	DN	$\overline{QN}$	QN
L	↑	H	L	H
L	↑	L	H	L
L	L	X	Qo	Qo
H	X	X	Z	Z

NOTE:

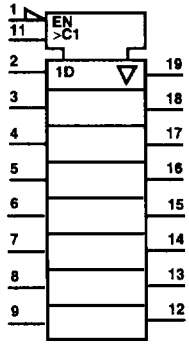
1. H = High Level (Steady State)
   L = Low Level (Steady State)
   X = Don't Care
   ↑ = Transition from low to high level
   Qo = The level of Q before the indicated steady state input conditions were established.
   Z = HIGH Impedance

IEC Logic Symbols

CD74FCT564



CD74FCT574



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Operating Conditions

Operating Temperature Range, T_A . . . . . 0°C to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	135
SOIC Package	125
SSOP Package	130

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_{CC} = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		MAX	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70°C.

Switching Specifications Over Operating Range t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 4

PARAMETER		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Clock to Q	CD74FCT574	t_{PLH}, t_{PHL}	5	6.6	2	10	ns
Clock to $\overline{Q}$	CD74FCT564	t_{PLH}, t_{PHL}	5	6.6	1.5	10	ns
Output Disable to Q	CD74FCT574	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to Q	CD74FCT574	t_{PZL}, t_{PZH}	5	9	1.5	12.5	ns
Output Disable to $\overline{Q}$	CD74FCT564	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$	CD74FCT564	t_{PZL}, t_{PZH}	5	9	1.5	12.5	ns
Power Dissipation Capacitance		C_{PD} (Note 6)	-	34 Typical			pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} (Figure 1)	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three State Output Capacitance		C_O	-	-	-	15	pF

NOTE:

6. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   PD (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_i C_{PD} + V_O^2 to C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_i = input frequency

Prerequisite For Switching

PARAMETER	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Clock Pulse Width CD74FCT574	t_W	5 (Note 7)		7	-	ns
CD74FCT564	t_W	5		7	-	ns
Setup Time Data to Clock	t_{SU}	5		2	-	ns
Data to Clock Hold Time						
CD74FCT574	t_H	5		2	-	ns
CD74FCT564	t_H	5		2	-	ns
Maximum Clock Frequency	f_{MAX}	5		70	-	MHz

NOTE:

7. 5V: minimum is at 4.5V.
   5V: minimum is at 4.75V for 0°C to 70°C.
   Typical is at 5V.