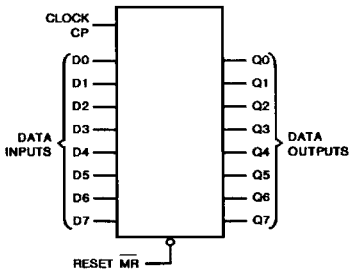
CD54/74FCT273
CD54/74FCT273AT

July 1990

Octal D Flip-Flop with Reset



FUNCTIONAL DIAGRAM

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 5.3ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT273)*

The CD54/74FCT273 and CD54/74FCT273AT octal D flip-flops with reset use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 4 milliamperes.

Information at the D Input of the CD54/74FCT273 and CD54/74FCT273AT is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

The CD54/74FCT273 and CD54/74FCT273AT are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT273 is also available in chip form (H suffix). This unpackaged device is operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX Types - Speed of bipolar FAST*/AS/S; FCTXXXAT Types - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS
RESET $\overline{MR}$	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Qo

H = High level (steady state).
L = Low level (steady state).
X = Irrelevant
⎍ = Transition from low to high level.
Qo = The level of Q before the indicated steady-state input conditions were established.

4 TECHNICAL DATA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

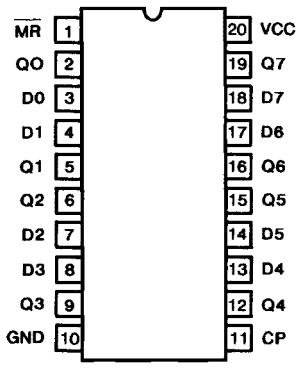
DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 400mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

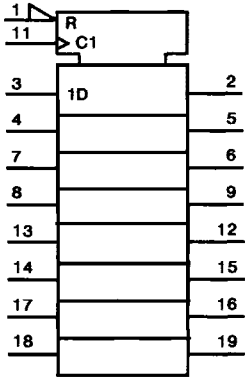
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT273 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT273AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Data to CP Setup Time	tSU	5†		3	-	3.5	-		2	-	2	-	ns
Hold Time	tH	5		2	-	2	-		1.5	-	1.5	-	ns
Removal Time, $\overline{MR}$ to CP	tREM	5		4	-	5	-		2	-	2.5	-	ns
$\overline{MR}$ Pulse Width	tW	5		7	-	7	-		6	-	6	-	ns
CP Pulse Width	tW	5		7	-	7	-		6	-	6	-	ns
CP Frequency	fMAX	5		70	-	70	-						MHz

†Min. is @ 4.5V
Min. is @ 4.75V for 0°C to +70°C
Typ is @ 5V

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5ns, C_L = 50pF, R_L = See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	CD54/74FCT273 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT273AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays:	CP to Qn	tPLH, tPHL	5†	7	2	13	2	15	5.3	2	7.2	2	8.5	ns
	$\overline{MR}$ to Qn	tPLH, tPHL	5	8	2	13	2	15	4.7	2	7.2	2.5	8.3	ns
Power Dissipation		§CDP	-	36 Typical					36 Typical					pF
Input Capacitance		CI	-	-	-	10	-	10	-	-	10	-	10	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

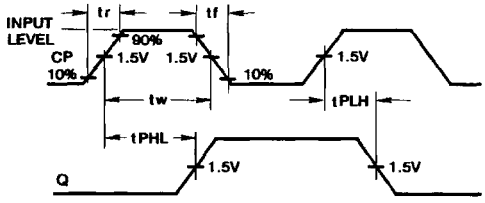


Fig. 1 - Propagation delay times and clock pulse width.

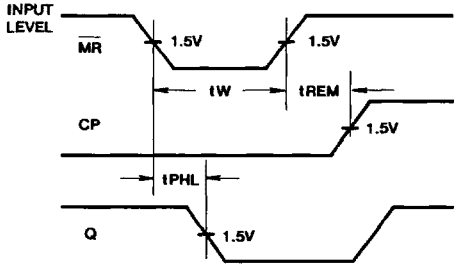


Fig. 2 - Prerequisite and propagation delay times for master reset.

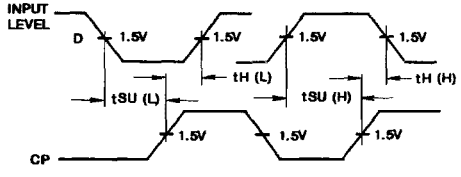


Fig. 3 - Prerequisite for clock.

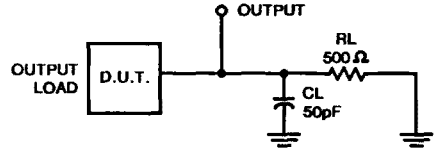


Fig. 4 - Test circuit.