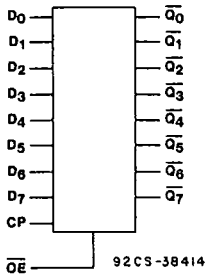
T-46-07-11

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

File Number **1640**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State, Inverting
Positive-Edge Triggered

Type Features:
- *Common 3-state output-enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capability*
- *Typical propagation delay = 13 ns @ V_{cc} = 5V, C_L = 15 pF, T_A = 25°C (clock to output)*

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

The RCA-CD54/74HC534, 564 and CD54/74HCT534, 564 are high speed OCTAL D-TYPE FLIP-FLOPS manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

The CD54/74HC534, 564 and CD54/74HCT534, 564 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the Q outputs on the positive going transition of the CLOCK input. When a high logic level is applied to the OUTPUT ENABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The CD54/74HCT logic family is speed, function, and pin compatible with the standard 54LS/74LS logic family.

The CD54HC and CD54HCT devices are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC and CD74HCT devices are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

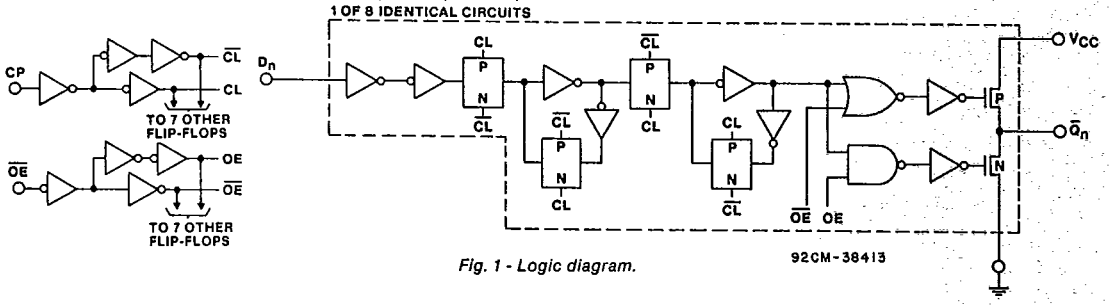


Fig. 1 - Logic diagram.

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

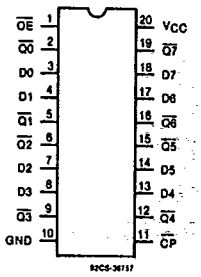
CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

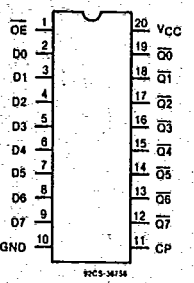
TRUTH TABLE

Inputs			Output
$\overline{OE}$	CP	Dn	$\overline{Qn}$
L	↗	H	L
L	↗	L	H
L	L	X	No Change
H	X	X	Z

Note:
X=Don't care
Z=High impedance state
↗=Low-to-High transition



Top View
CD54/74HC, HCT534 Types
TERMINAL ASSIGNMENT



Top View
CD54/74HC,HCT564 Types
TERMINAL ASSIGNMENT

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC534/CD54HC534 CD74HC564/CD54HC564										CD74HCT534/CD54HCT534 CD74HCT564/CD54HCT564									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D_0—D_7	0.15
CP	0.30
$\overline{OE}$	0.55

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Clock to Q	t_{PLH} t_{PHL}	15	13	14	ns
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	15	12	12	ns
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	15	12	14	ns
Maximum Clock Frequency	f_{max}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	32	36	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: F_i = input frequency f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25° C HC Min.	25° C HC Max.	25° C HCT Min.	25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Maximum Clock Frequency	f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse Width Fig. 2	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time Data to Clock Fig. 3	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	20	—	15	—	25	—	18	—	30	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock Fig. 3	534 t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
	564 t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	3	—	5	—	3	—	5	—	3	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	

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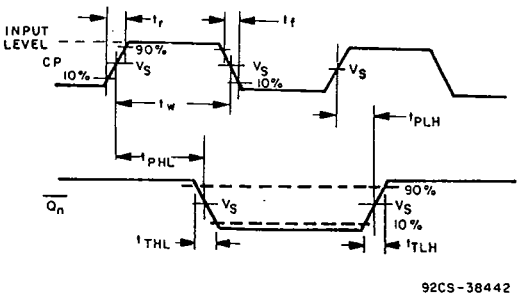
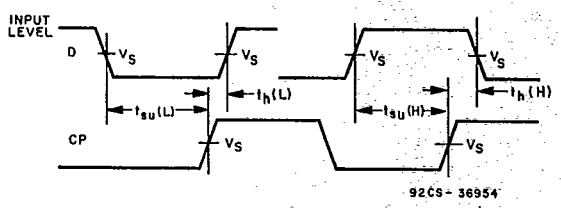
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Clock to Output Fig. 2	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
	t_{PHL}	4.5	—	33	—	35	—	41	—	44	—	50	—	53	ns
		6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay Output Disable to Q Fig. 4 534	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
		4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
	t_{PHZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay Output Disable to Q Fig. 4 564	t_{PLZ}	2	—	135	—	—	—	170	—	—	—	205	—	—	
		4.5	—	27	—	30	—	34	—	38	—	41	—	45	ns
	t_{PHZ}	6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay Output Enable to Q Fig. 4	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
	t_{PZH}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time Fig. 2	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



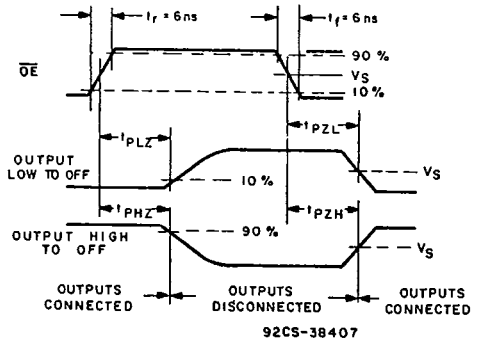
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

Fig. 2—Clock to output delays and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

Fig. 3—Data set-up and hold times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

Fig. 4—Transition times and propagation delay times.