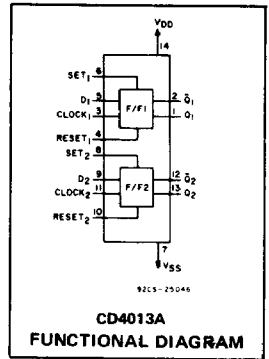


Dual 'D'-Type Flip-Flop

The RCA-CD4013A consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and Q̄ outputs. These devices can be used for shift register applications, and by connecting Q̄ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse.

Setting or resetting is independent of the clock and is accomplished by a high level on the set (with low-level on reset) or reset (with low-level on set) line, respectively. These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T _{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T _A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE (V _{DD})	
(Voltages referenced to V _{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P _D)	
FOR T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T _A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Features:

- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation — 10 MHz (typ.) clock toggle rate at 10 V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Registers, counters, control circuits

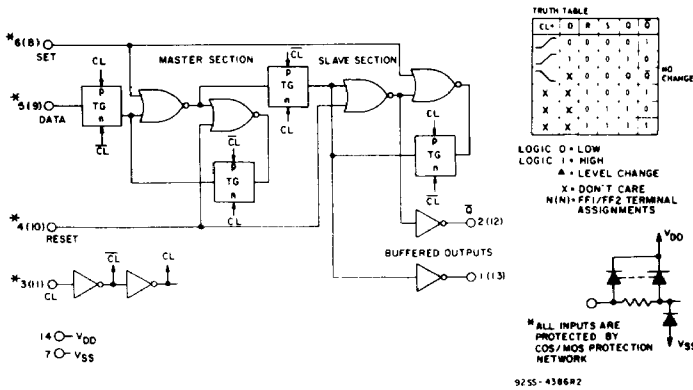


Fig. 1 — Logic diagram and truth table for CD4013A (one of two identical flip flops).

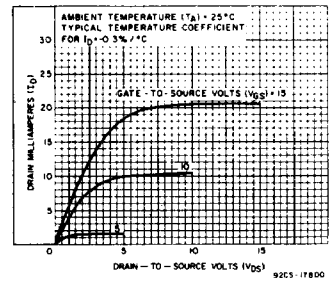


Fig.2 — Typical n-channel drain characteristics.

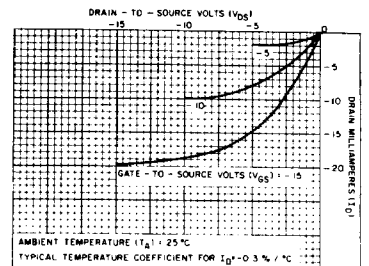


Fig.3 — Typical p-channel drain characteristics.

CD4013A Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted:
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges –

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D,F,K,H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$)	–	3	12	3	12	V
Data Setup Time t_S	5 10	40 20	–	50 25	–	ns
Clock Pulse Width t_W	5 10	200 80	–	500 100	–	ns
Clock Input Frequency f_{CL}	5 10	dc	2.5 7	dc	1 5	MHz
Clock Rise or Fall Time t_{rCL}^*, t_{fCL}	5 10	–	15 5	–	15 5	μs
Set or Reset Pulse Width	5 10	250 100	–	500 125	–	ns

* If more than one unit is cascaded in a parallel clocked operation, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

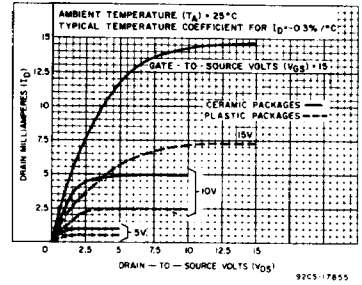


Fig. 4 – Minimum n-channel drain characteristics.

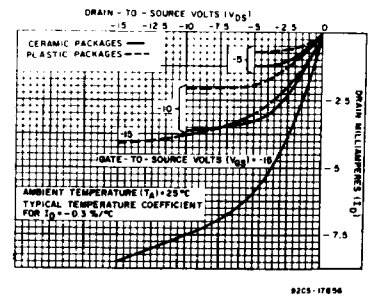


Fig. 5 – Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_f = 20 \text{ ns}$, $C_L = 15 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS						UNITS
		D,F,K,H Packages			E Package			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: Clock to Q or \bar{Q} Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	350	ns
	10	–	75	110	–	75	125	
Set to Q or Reset to \bar{Q} t_{PLH}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Set to \bar{Q} or Reset to Q t_{PHL}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Transition Time, t_{THL}, t_{TLH}	5	–	75	125	–	75	150	ns
	10	–	50	70	–	50	75	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4	–	1	4	–	MHz
	10	7	10	–	5	10	–	
Minimum Clock Pulse Width, t_W	5	–	125	200	–	125	500	ns
	10	–	50	80	–	50	100	
Minimum Set or Reset Pulse Width, t_W	5	–	125	250	–	125	500	ns
	10	–	50	100	–	50	125	
Minimum Data Setup Time, t_S	5	–	20	40	–	20	50	ns
	10	–	10	20	–	10	25	
Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_i	Any Input	–	5	–	–	5	–	pF

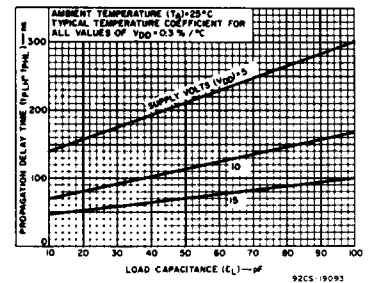


Fig. 6 – Typical propagation delay time vs. C_L .

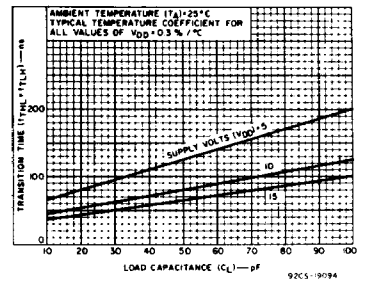


Fig. 7 – Typical transition time vs. C_L .

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)									Units
				D, F, K, H Packages						E Package			
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85		
Quiescent Device Current, I _L Max.	-	-	5	1	0.005	1	60	10	0.01	10	140	μA	
	-	-	10	2	0.005	2	120	20	0.02	20	280		
	-	-	15	25	0.5	25	1000	250	2.5	250	2500		
Output Voltage: Low-Level, V _{OL}	-	0.5	5	0 Typ.; 0.05 Max.									V
	-	0.10	10	0 Typ.; 0.05 Max.									
	-	0.5	5	5 Typ.; 4.95 Min.									
High-Level, V _{OH}	-	0.5	5	10 Typ.; 9.95 Min.									V
	-	0.10	10										
Noise Immunity: Inputs Low, V _{NL}	4.2	-	5	2.25 Typ.; 1.5 Min.									V
	9	-	10	4.5 Typ.; 3 Min.									
	0.8	-	5	2.25 Typ.; 1.5 Min.									
Inputs High, V _{NH}	1	-	10	4.5 Typ.; 3 Min.									V
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.									V
	9	-	10	1 Min.									
	0.5	-	5	1 Min.									
Inputs High, V _{NMH}	1	-	10	1 Min.									V
Output Drive Current: N-Channel (Sink) I _{DN} Min.	0.5	-	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA	
	0.5	-	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5		
P-Channel (Source) I _{DP} Min.	4.5	-	5	-0.31	-0.5	-0.25	-0.175	-0.17	-0.5	-0.14	-0.12	mA	
	9.5	-	10	-0.8	-1.3	-0.65	-0.45	-0.4	-1.3	-0.33	-0.27		
Input Leakage Current, I _{IL} , I _{IH}	Any Input		15	±10 ⁻⁵ Typ.; ±1 Max.									μA

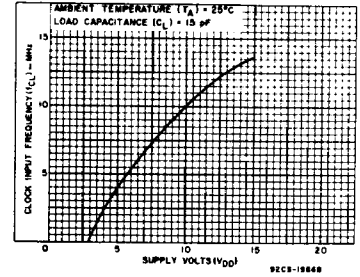


Fig. 8 — Typical maximum clock input frequency vs. V_{DD}.

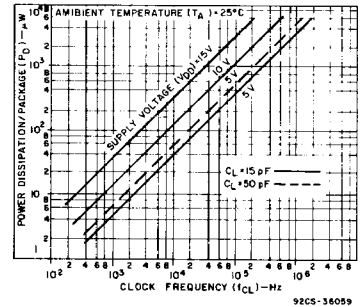


Fig. 9 — Typical dissipation characteristics.

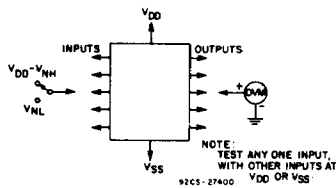


Fig. 10 — Noise immunity test circuit.

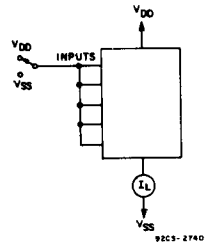


Fig. 12 — Quiescent device-current test circuit.

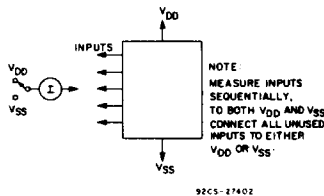


Fig. 11 — Input leakage test circuit.

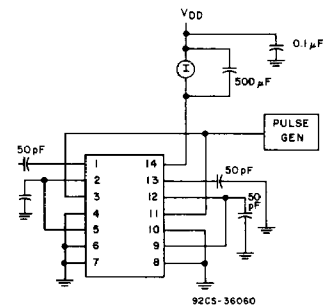


Fig. 13 — Dynamic power dissipation test circuit.