# HARRIS SEMICONDUCTOR

# HFA1109

## 450MHz, Low Power, Current Feedback Video Operational Amplifier

February 1997

### Features

- Wide -3dB Bandwidth ($A_V$ = +2) . . . . . . . . . . . . 450MHz
- Gain Flatness (To 250MHz) . . . . . . . . . . . . . . . . . . 0.8dB
- Very Fast Slew Rate ($A_V$ = +2) . . . . . . . . . . . . . 1100V/µs
- High Input Impedance . . . . . . . . . . . . . . . . . . . . . 1.7MΩ
- Differential Gain/Phase . . . . . . . . . 0.02%/0.02 Degrees
- Low Supply Current . . . . . . . . . . . . . . . . . . . . . . . 10mA

### Applications

- Professional Video Processing
- Video Switchers and Routers
- Medical Imaging
- PC Multimedia Systems
- Video Distribution Amplifiers
- Flash Converter Drivers
- Radar/IF Processing

### Description

The HFA1109 is a high speed, low power, current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process. This amplifier features a unique combination of power and performance specifically tailored for video applications.

The HFA1109 is a standard pinout op amp. It is a higher performance, drop-in replacement (no feedback resistor change required) for the CLC409.

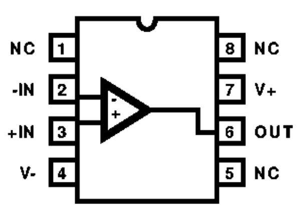
If a comparably performing op amp with an output disable function (useful for video multiplexing) is required, please refer to the HFA1149 data sheet.

### Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HFA1109IP | -40 to 85 | 8 Ld PDIP | E8.3 |
| HFA1109IB (H1109) | -40 to 85 | 8 Ld SOIC | M8.15 |
| HFA11XXEVAL | DIP Evaluation Board for High Speed Op Amps | | |

### Pinout

HFA1109
(PDIP, SOIC)
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

### Absolute Maximum Ratings

Voltage Between V+ and V- . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12V
DC Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $V_{SUPPLY}$
Differential Input Voltage. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8V
Output Current (Note 2) . . . . . . . . . . . . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle

ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 1400V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93). . . 2000V
Machine Model (Per EIAJ ED-4701Method C-111) . . . . . . . 100V

### Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| PDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . | 130 |
| SOIC Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . | 170 |

Maximum Junction Temperature (Die). . . . . . . . . . . . . . . . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . . . . 150°C
Maximum Storage Temperature Range . . . . . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300°C
(SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . -40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

### Electrical Specifications

$V_{SUPPLY}$ = ±5V, $A_V$ = +2, $R_F$ = 250Ω, $R_L$ = 100Ω, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. (°C) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Input Offset Voltage | | A | 25 | - | 1 | 5 | mV |
| | | A | Full | - | 2 | 8 | mV |
| Average Input Offset Voltage Drift | | B | Full | - | 10 | - | µV/°C |
| Input Offset Voltage Common-Mode Rejection Ratio | $\Delta V_{CM}$ = ±2V | A | 25 | 47 | 50 | - | dB |
| | $\Delta V_{CM}$ = ±2V | A | Full | 45 | 48 | - | dB |
| Input Offset Voltage Power Supply Rejection Ratio | $\Delta V_{PS}$ = ±1.25V | A | 25 | 50 | 53 | - | dB |
| | $\Delta V_{PS}$ = ±1.25V | A | Full | 47 | 51 | - | dB |
| Non-Inverting Input Bias Current | | A | 25 | - | 4 | 10 | µA |
| | | A | Full | - | 5 | 15 | µA |
| Non-Inverting Input Bias Current Drift | | B | Full | - | 30 | - | nA/°C |
| Non-Inverting Input Bias Current Power Supply Sensitivity | $\Delta V_{PS}$ = ±1.25V | A | 25 | - | 0.5 | 1 | µA/V |
| | $\Delta V_{PS}$ = ±1.25V | A | Full | - | 0.5 | 3 | µA/V |
| Inverting Input Bias Current | | A | 25 | - | 2 | 10 | µA |
| | | A | Full | - | 3 | 15 | µA |
| Inverting Input Bias Current Drift | | B | Full | - | 40 | - | nA/°C |
| Inverting Input Bias Current Common-Mode Sensitivity | $\Delta V_{CM}$ = ±2V | A | 25 | - | 3 | 6 | µA/V |
| | $\Delta V_{CM}$ = ±2V | A | Full | - | 3 | 8 | µA/V |
| Inverting Input Bias Current Power Supply Sensitivity | $\Delta V_{PS}$ = ±1.25V | A | 25 | - | 1.6 | 5 | µA/V |
| | $\Delta V_{PS}$ = ±1.25V | A | Full | - | 1.6 | 8 | µA/V |

**Electrical Specifications** $V_{SUPPLY}$ = ±5V, $A_V$ = +2, $R_F$ = 250Ω, $R_L$ = 100Ω, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. (°C) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Non-Inverting Input Resistance | $\Delta V_{CM}$ = ±2V | A | 25, 85 | 0.8 | 1.7 | - | MΩ |
| | $\Delta V_{CM}$ = ±2V | A | -40 | 0.5 | 1.4 | - | MΩ |
| Inverting Input Resistance | | C | 25 | - | 60 | - | Ω |
| Input Capacitance | | C | 25 | - | 1.6 | - | pF |
| Input Voltage Common Mode Range (Implied by $V_{IO}$ CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests) | | A | Full | ±2 | ±2.5 | - | V |
| Input Noise Voltage Density (Note 4) | f = 100kHz | B | 25 | - | 4 | - | nV/√Hz |
| Non-Inverting Input Noise Current Density (Note 4) | f = 100kHz | B | 25 | - | 2.4 | - | pA/√Hz |
| Inverting Input Noise Current Density (Note 4) | f = 100kHz | B | 25 | - | 40 | - | pA/√Hz |
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| Open Loop Transimpedance Gain (Note 4) | | B | 25 | - | 500 | - | kΩ |
| Minimum Stable Gain | | B | Full | - | 1 | - | V/V |
| **AC CHARACTERISTICS** | | | | | | | |
| -3dB Bandwidth ($V_{OUT}$ = 0.2$V_{P-P}$, Note 4) | $A_V$ = -1, $R_F$ = 200Ω | B | 25 | - | 380 | - | MHz |
| | $A_V$ = +1, $+R_S$ = 550Ω | B | 25 | - | 350 | - | MHz |
| | $A_V$ = +2 | B | 25 | - | 450 | - | MHz |
| Gain Peaking | $A_V$ = +2, $V_{OUT}$ = 0.2$V_{P-P}$ | B | 25 | - | 0 | 0.2 | dB |
| Gain Flatness ($A_V$ = +2, $V_{OUT}$ = 0.2$V_{P-P}$, Note 4) | To 125MHz | B | 25 | - | -0.45 | - | dB |
| | To 200MHz | B | 25 | - | -0.75 | - | dB |
| | To 250MHz | B | 25 | - | -0.82 | - | dB |
| Gain Flatness ($A_V$ = +1, $+R_S$ = 550Ω, $V_{OUT}$ = 0.2$V_{P-P}$, Note 4) | To 125MHz | B | 25 | - | ±0.06 | - | dB |
| | To 200MHz | B | 25 | - | ±0.26 | - | dB |
| | To 250MHz | B | 25 | - | ±0.5 | - | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage Swing, Unloaded (Note 4) | $A_V$ = -1, $R_L$ = ∞ | A | 25 | ±3 | ±3.2 | - | V |
| | | A | Full | ±2.8 | ±3 | - | V |
| Output Current (Note 4) | $A_V$ = -1, $R_L$ = 75Ω | A | 25, 85 | ±33 | ±36 | - | mA |
| | | A | -40 | ±30 | ±33 | - | mA |
| Output Short Circuit Current | $A_V$ = -1 | B | 25 | - | 120 | - | mA |
| Closed Loop Output Resistance (Note 4) | DC, $A_V$ = +1 | B | 25 | - | 0.05 | - | Ω |
| Second Harmonic Distortion ($V_{OUT}$ = 2$V_{P-P}$, Note 4) | 20MHz | B | 25 | - | -55 | - | dBc |
| | 60MHz | B | 25 | - | -57 | - | dBc |

**Electrical Specifications** $V_{SUPPLY} = \pm5V$, $A_V = +2$, $R_F = 250\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. (°C) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 4) | 20MHz | B | 25 | - | -68 | - | dBc |
| | 60MHz | B | 25 | - | -60 | - | dBc |
| Reverse Isolation ($S_{12}$) | 30MHz | B | 25 | - | -65 | - | dB |
| **TRANSIENT CHARACTERISTICS** | | | | | | | |
| Rise and Fall Times | $V_{OUT} = 0.5V_{P-P}$ | B | 25 | - | 1.1 | - | ns |
| Overshoot | $V_{OUT} = 0.5V_{P-P}$ | B | 25 | - | 0 | - | % |
| Slew Rate | $A_V = -1$, $R_F = 200\Omega$ $V_{OUT} = 5V_{P-P}$ | B | 25 | - | 2600 | - | V/µs |
| | $A_V = +1, V_{OUT} = 4V_{P-P}$, $+R_S = 550\Omega$ | B | 25 | - | 575 | - | V/µs |
| | $A_V = +2$, $V_{OUT} = 5V_{P-P}$ | B | 25 | - | 1100 | - | V/µs |
| Settling Time ($V_{OUT}$ = +2V to 0V step, Note 4) | To 0.1% | B | 25 | - | 19 | - | ns |
| | To 0.05% | B | 25 | - | 23 | - | ns |
| | To 0.01% | B | 25 | - | 36 | - | ns |
| Overdrive Recovery Time | $V_{IN} = \pm2V$ | B | 25 | - | 5 | - | ns |
| **VIDEO CHARACTERISTICS** | | | | | | | |
| Differential Gain (f = 3.58MHz) | $R_L = 150\Omega$ | B | 25 | - | 0.02 | - | % |
| | $R_L = 75\Omega$ | B | 25 | - | 0.05 | - | % |
| Differential Phase (f = 3.58MHz) | $R_L = 150\Omega$ | B | 25 | - | 0.02 | - | Degrees |
| | $R_L = 75\Omega$ | B | 25 | - | 0.05 | - | Degrees |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | | |
| Power Supply Range | | C | 25 | ±4.5 | - | ±5.5 | V |
| Power Supply Current (Note 4) | | A | 25 | - | 9.6 | 10 | mA |
| | | A | Full | - | 10 | 11 | mA |

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.

## Application Information

### Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and $R_F$. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and $R_F$, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to $R_F$. The HFA1109 design is optimized for a $250\Omega$ $R_F$ at a gain of +2. Decreasing $R_F$ decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so $R_F$ can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended $R_F$ values, and the expected bandwidth, for various closed loop gains. For a gain of +1, a resistor ($+R_S$) in series with +IN is required to reduce gain peaking and increase stability.

**TABLE 1. OPTIMUM FEEDBACK RESISTOR**

| GAIN ($A_{CL}$) | $R_F$ (Ω) | BANDWIDTH (MHz) |
|---|---|---|
| -1 | 200 | 400 |
| +1 | 250 ($+R_S$ = 550Ω) | 350 |
| +2 | 250 | 450 |
| +5 | 100 | 160 |
| +10 | 90 | 70 |

## PC Board Layout

The frequency response of this amplifier depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. Thus it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

## Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor ($R_S$) in series with the output prior to the capacitance.

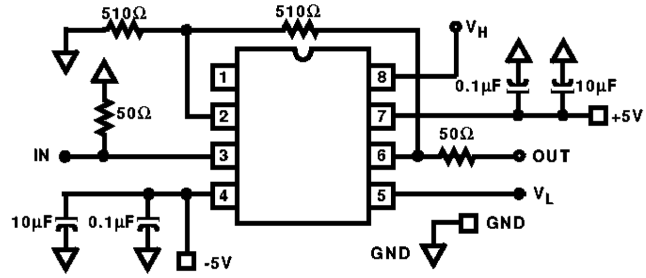
$R_S$ and $C_L$ form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth. By decreasing $R_S$ as $C_L$ increases, the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

## Evaluation Board

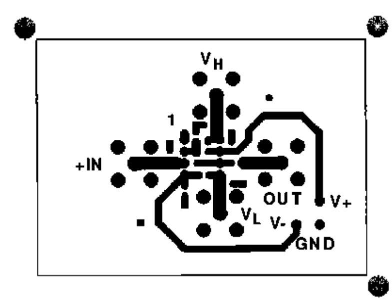
The performance of the HFA1109 may be evaluated using the HFA11XX evaluation board (part number HFA11XXEVAL). Please contact your local sales office for information. When evaluating this amplifier, the two 510Ω gain setting resistors on the evaluation board should be changed to 250Ω.

The layout and schematic of the board are shown in Figure 1.

**BOARD SCHEMATIC**




**TOP LAYOUT**




**BOTTOM LAYOUT**

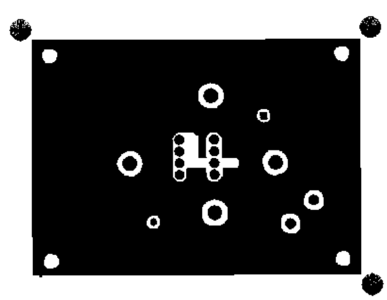


**FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT**

## Typical Performance Curves
$V_{SUPPLY}$ = ±5V, $T_A$ = 25°C, $R_F$ = Value From the Optimum Feedback Resistor Table, $R_L$ = 100Ω, Unless Otherwise Specified

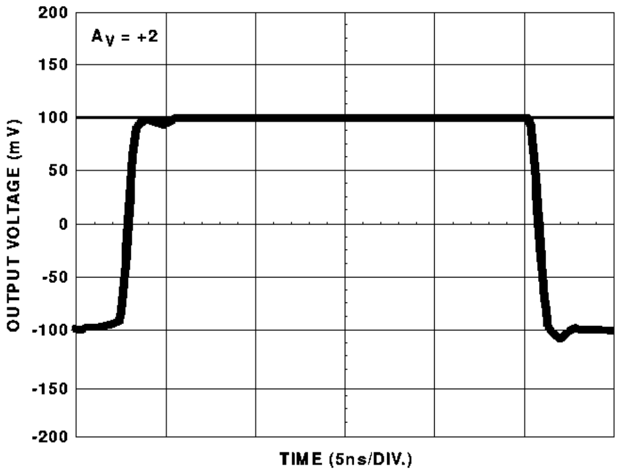



FIGURE 2. SMALL SIGNAL PULSE RESPONSE

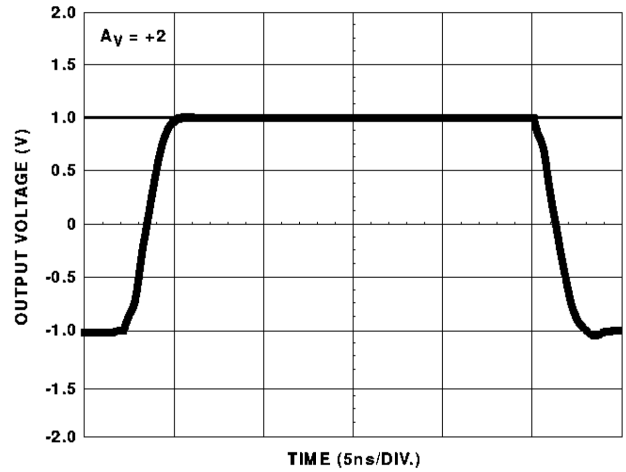



FIGURE 3. LARGE SIGNAL PULSE RESPONSE

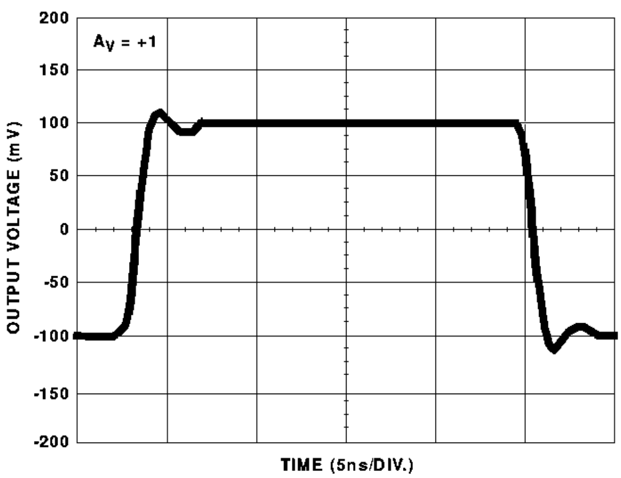



FIGURE 4. SMALL SIGNAL PULSE RESPONSE

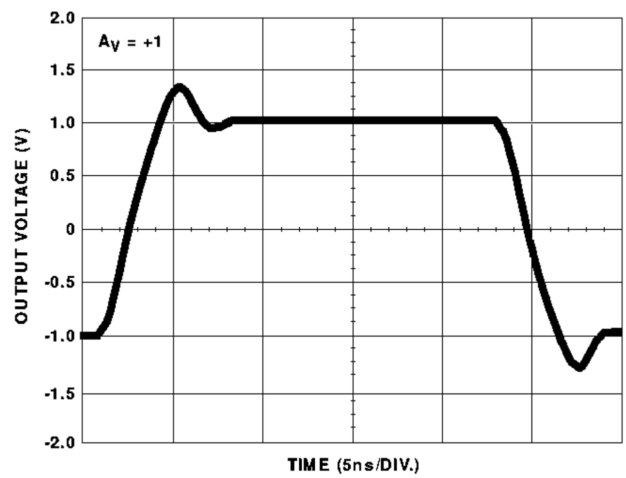



FIGURE 5. LARGE SIGNAL PULSE RESPONSE

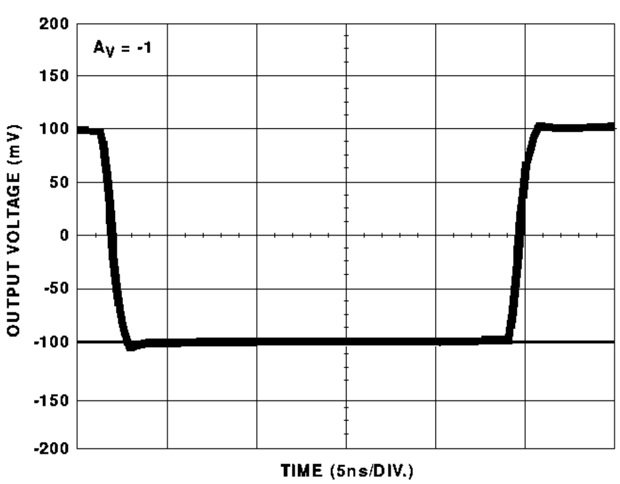



FIGURE 6. SMALL SIGNAL PULSE RESPONSE

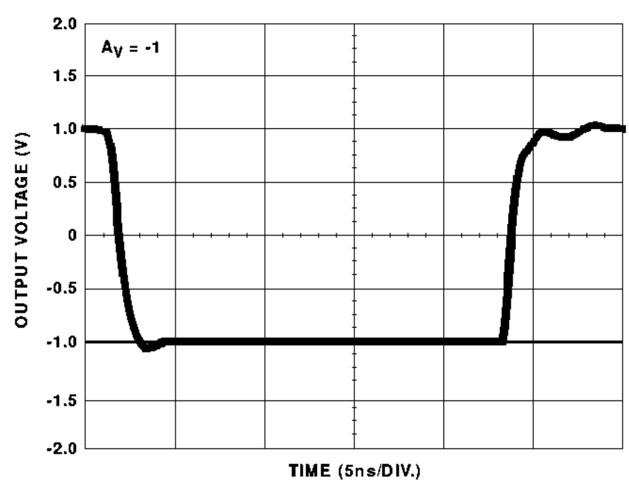



FIGURE 7. LARGE SIGNAL PULSE RESPONSE

## *Typical Performance Curves* $V_{SUPPLY}$ = ±5V, $T_A$ = 25°C, $R_F$ = Value From the Optimum Feedback Resistor Table, $R_L$ = 100Ω, Unless Otherwise Specified **(Continued)**

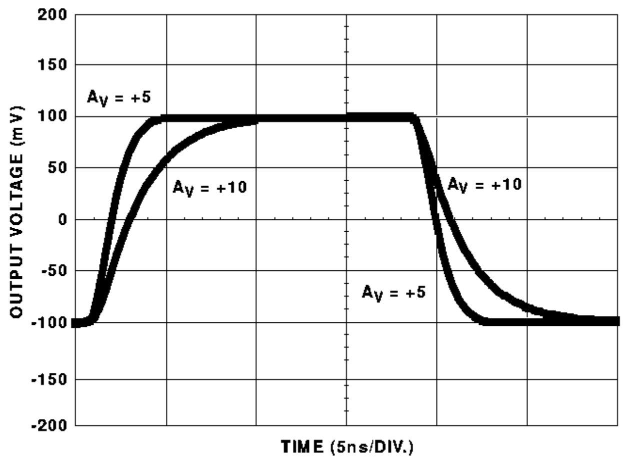



FIGURE 8. SMALL SIGNAL PULSE RESPONSE

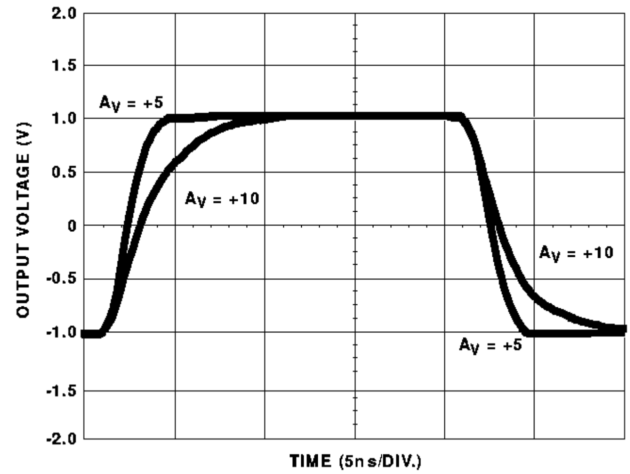



FIGURE 9. LARGE SIGNAL PULSE RESPONSE

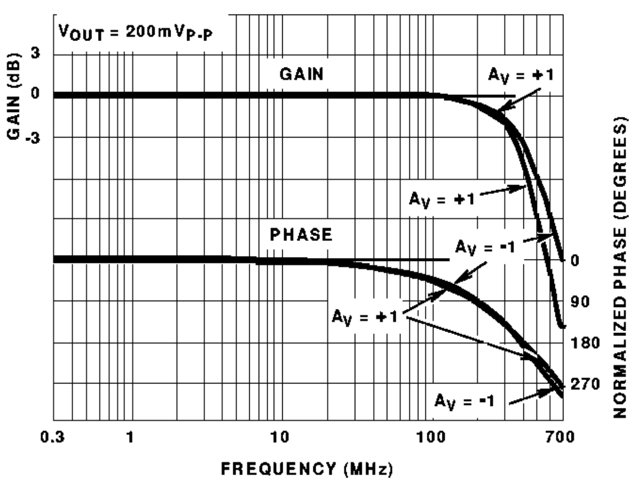



FIGURE 10. FREQUENCY RESPONSE

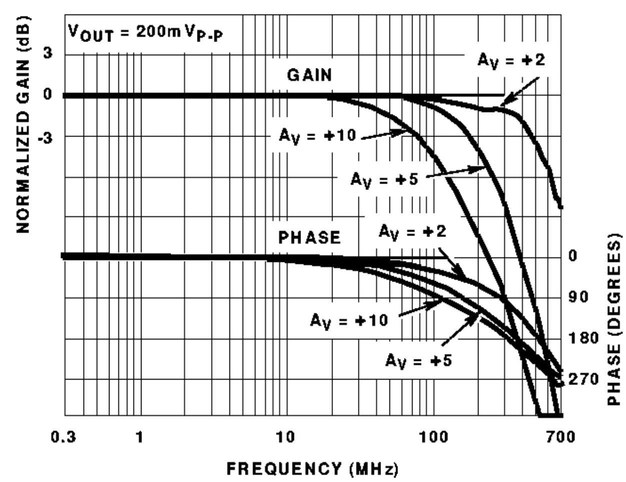



FIGURE 11. FREQUENCY RESPONSE

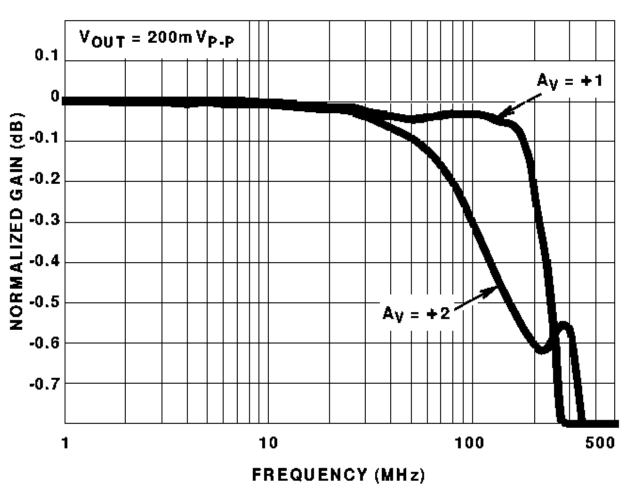



FIGURE 12. GAIN FLATNESS

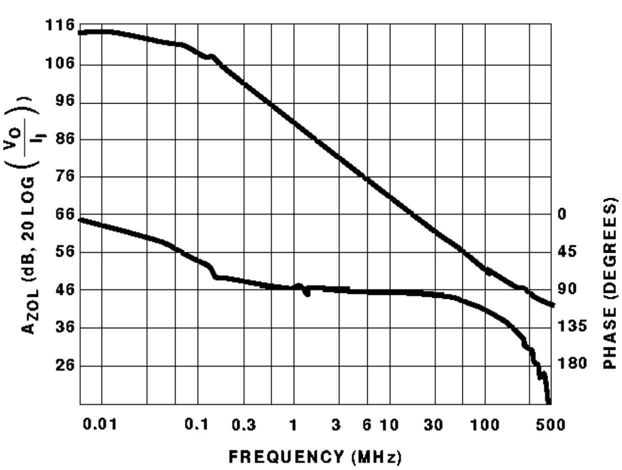



FIGURE 13. OPEN LOOP TRANSIMPEDANCE

## *Typical Performance Curves* $V_{SUPPLY}$ = ±5V, $T_A$ = 25°C, $R_F$ = Value From the Optimum Feedback Resistor Table, $R_L$ = 100Ω, Unless Otherwise Specified **(Continued)**

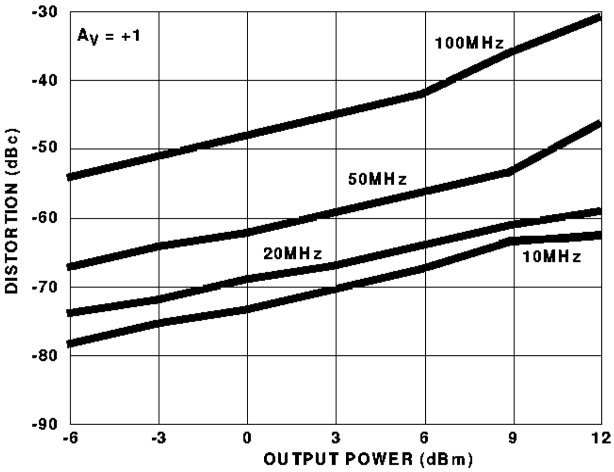



FIGURE 14. 2nd HARMONIC DISTORTION vs $P_{OUT}$

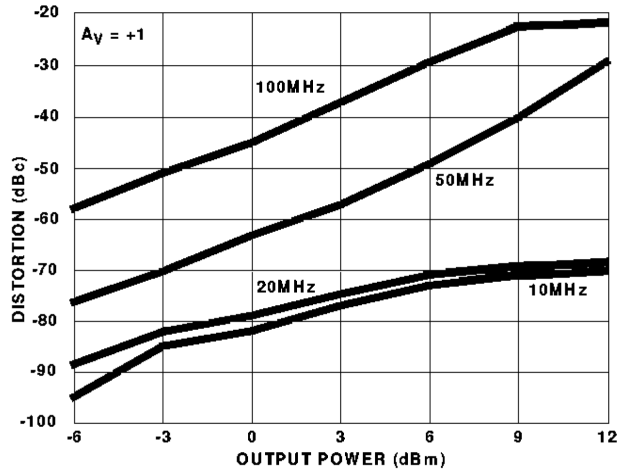



FIGURE 15. 3rd HARMONIC DISTORTION vs $P_{OUT}$

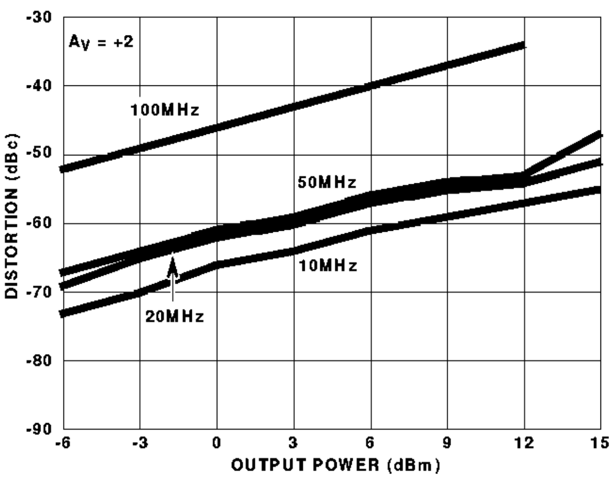



FIGURE 16. 2nd HARMONIC DISTORTION vs $P_{OUT}$

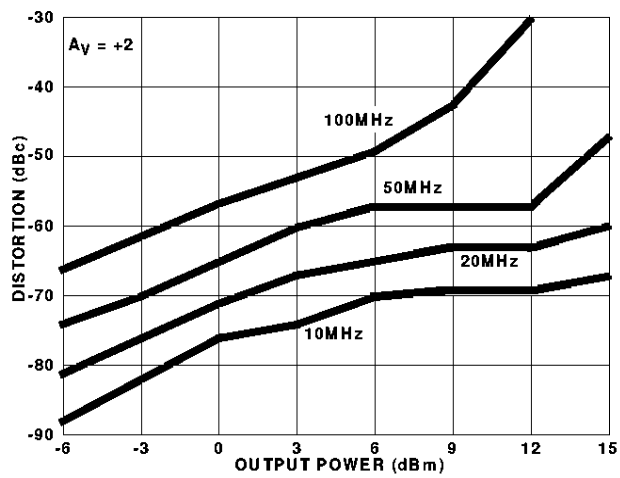



FIGURE 17. 3rd HARMONIC DISTORTION vs $P_{OUT}$

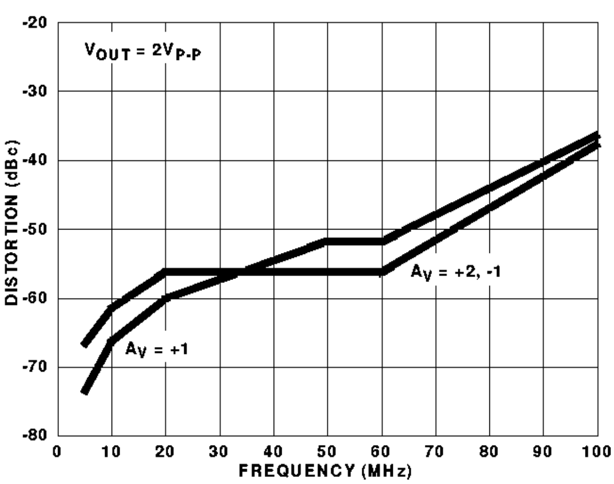



FIGURE 18. 2nd HARMONIC DISTORTION vs FREQUENCY

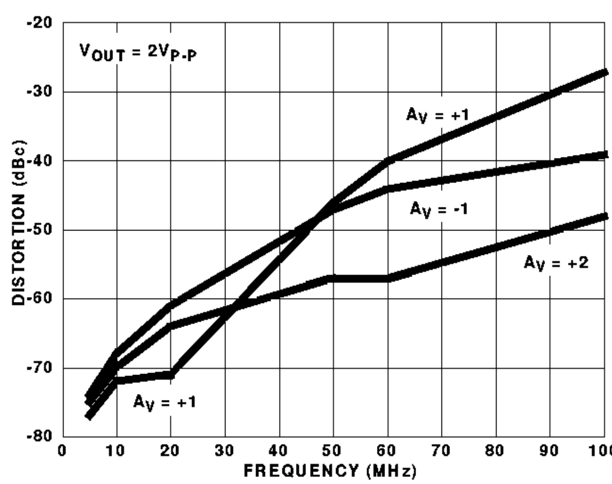



FIGURE 19. 3rd HARMONIC DISTORTION vs FREQUENCY

## Typical Performance Curves
$V_{SUPPLY}$ = ±5V, $T_A$ = 25°C, $R_F$ = Value From the Optimum Feedback Resistor Table, $R_L$ = 100Ω, Unless Otherwise Specified **(Continued)**

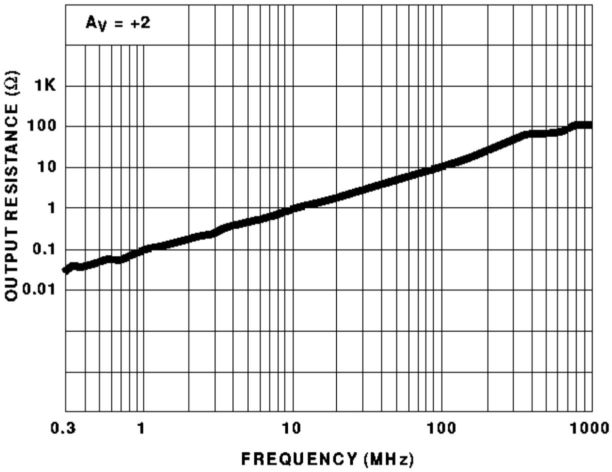



FIGURE 20. CLOSED LOOP OUTPUT RESISTANCE

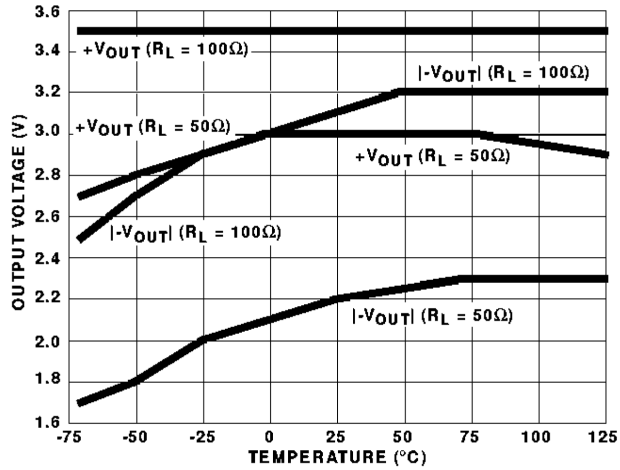



FIGURE 21. OUTPUT VOLTAGE vs TEMPERATURE

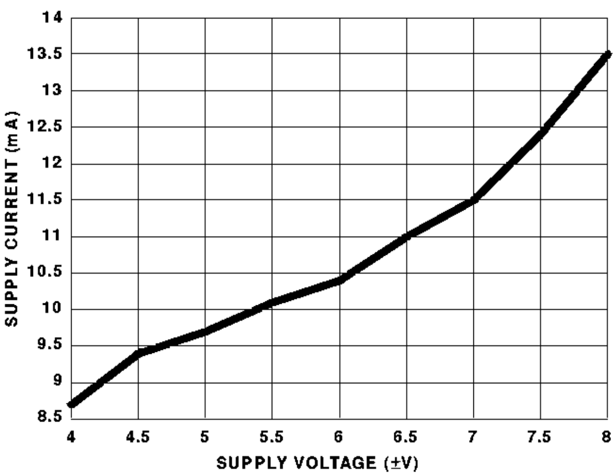



FIGURE 22. SUPPLY CURRENT vs SUPPLY VOLTAGE

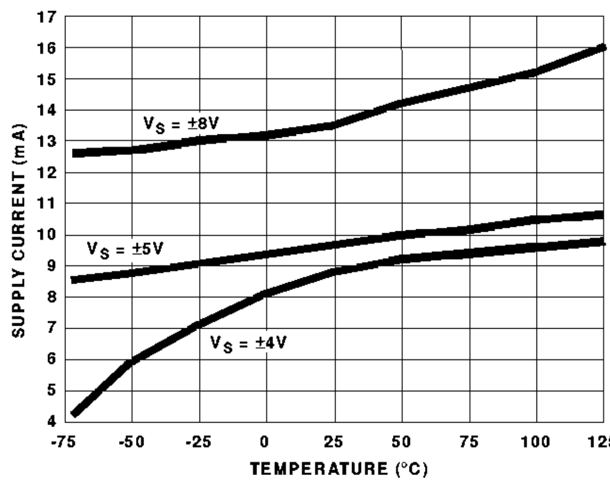



FIGURE 23. SUPPLY CURRENT vs TEMPERATURE

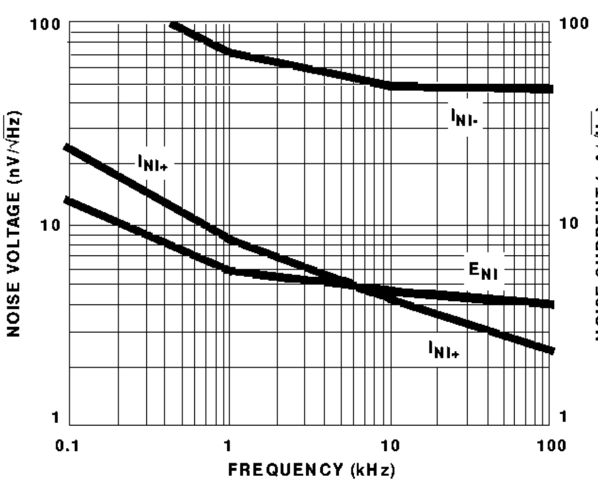



FIGURE 24. INPUT NOISE CHARACTERISTICS

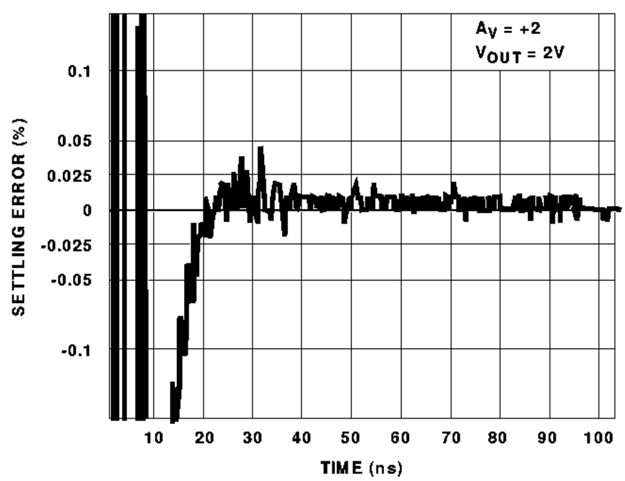



FIGURE 25. SETTLING RESPONSE

## Die Characteristics

**DIE DIMENSIONS:**

59 mils x 80 mils x 19 mils
1500µm x 2020µm x 483µm

**METALLIZATION:**

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ  0.8kÅ

**GLASSIVATION:**

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

**TRANSISTOR COUNT:**

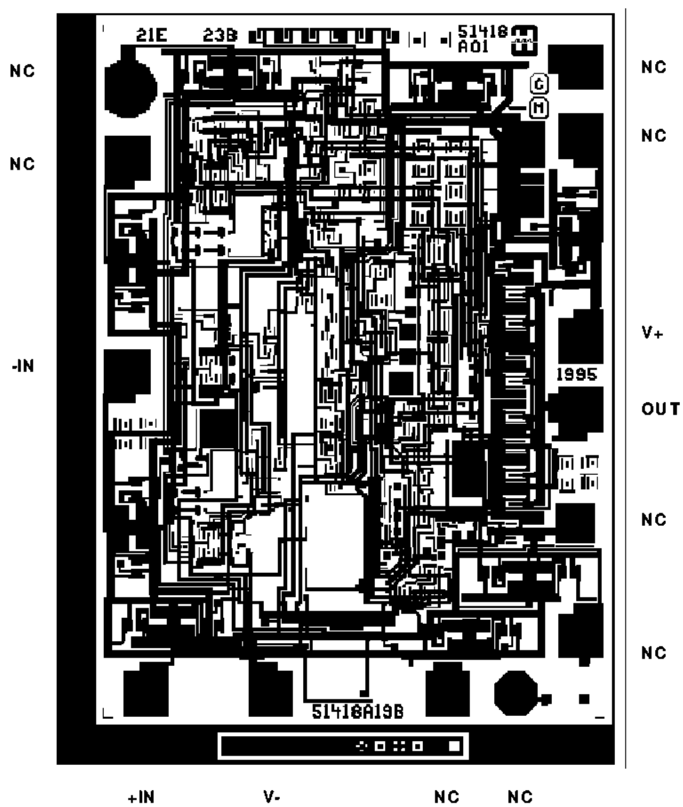
130

**SUBSTRATE POTENTIAL (Powered Up):**

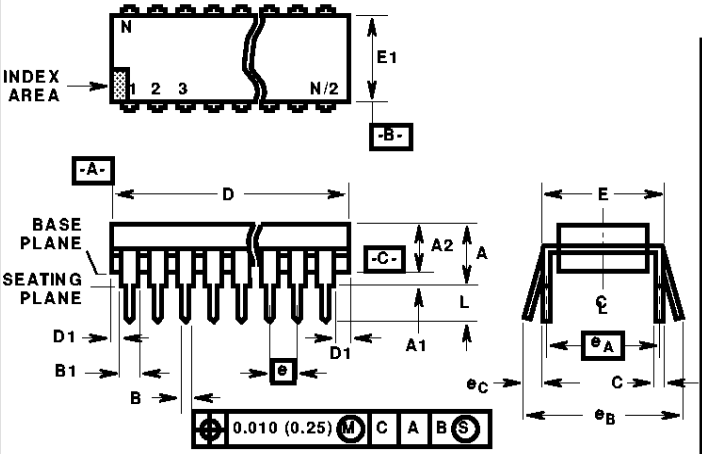
Floating (Recommend Connection to V-)

## Metallization Mask Layout

**HFA1109**



## Dual-In-Line Plastic Packages (PDIP)




NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E8.3** (JEDEC MS-001-BA ISSUE D)
**8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

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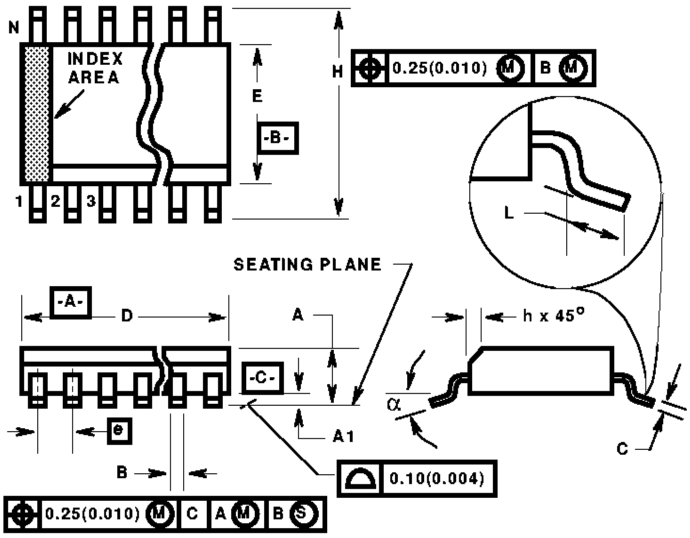
## Small Outline Plastic Packages (SOIC)




**M8.15** (JEDEC MS-012-AA ISSUE C)
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | NOTES |
|---|---|---|---|---|---|
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

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NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.



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