



Integrated Device Technology, Inc.

3.3V CMOS 20-BIT BUFFERS

IDT74FCT163827A/B/C

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

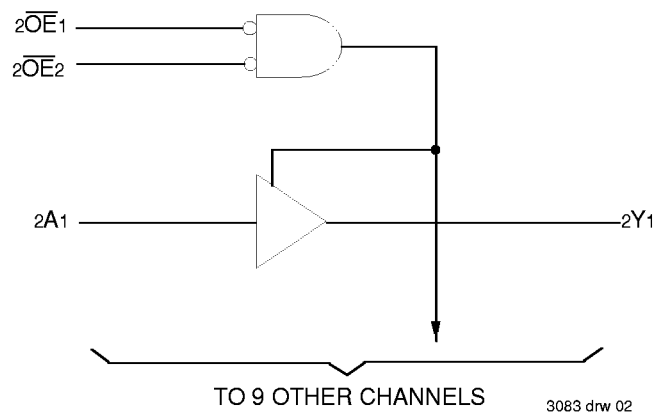
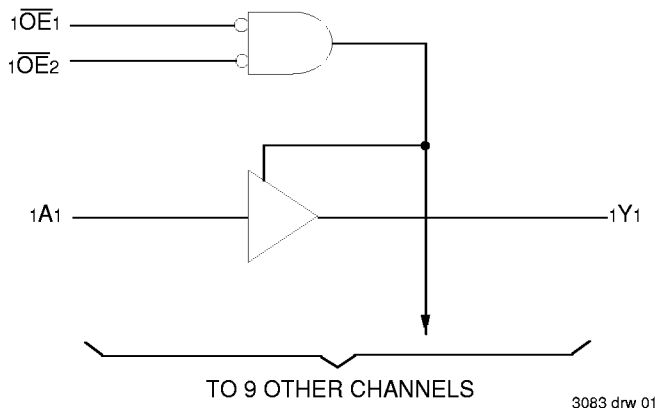
DESCRIPTION:

The FCT163827A/B/C 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163827A/B/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors.

The inputs of the FCT163827A/B/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM

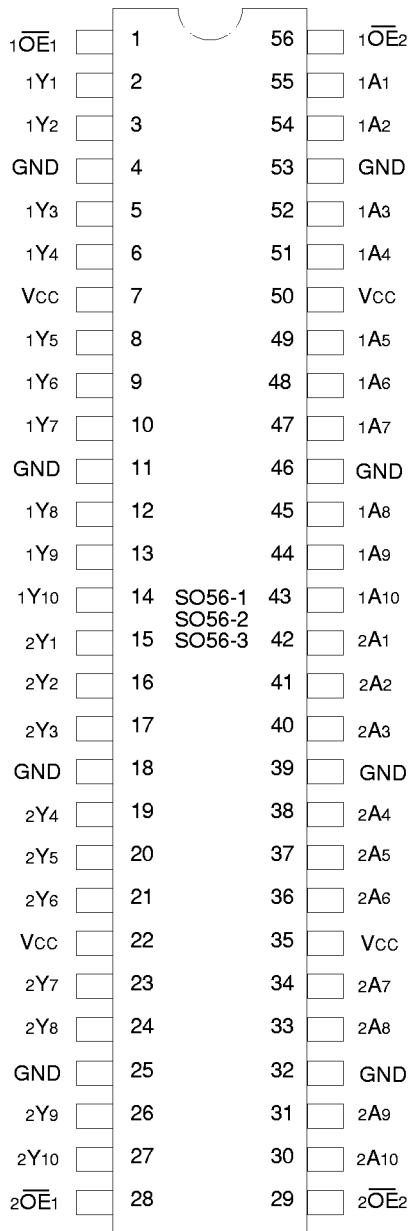


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EXTENDED COMMERCIAL TEMPERATURE RANGE

AUGUST 1996

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}x$	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
$V_{TERM}^{(4)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Output and I/O terminals.

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
$\overline{xOE}1$	$\overline{xOE}2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

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- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8.0	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: TA = -40°C to +85°C, VCC = 2.7V to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit		
VIH	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V		
	Input HIGH Level (I/O pins)		2.0	—	VCC+0.5			
VIL	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V		
IIH	Input HIGH Current (Input pins)	VCC = Max.	VI = 5.5V	—	—	±1	µA	
	Input HIGH Current (I/O pins)							VI = VCC
IIL	Input LOW Current (Input pins)		VI = GND	—	—	—		±1
	Input LOW Current (I/O pins)			VI = GND	—	—		—
IOZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	VO = VCC	—	—	±1	µA	
IOZL			VO = GND	—	—	±1		
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18mA	—	-0.7	-1.2	V		
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA		
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA		
VOH	Output HIGH Voltage	VCC = Min.	IOH = -0.1mA	VCC-0.2	—	—	V	
		VIN = VIH or VIL	IOH = -3mA	2.4	3.0	—		
		VCC = 3.0V VIN = VIH or VIL	IOH = -8mA	2.4 ⁽⁵⁾	3.0	—		
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 0.1mA	—	—	0.2	V	
			IOL = 16mA	—	0.2	0.4		
			IOL = 24mA	—	0.3	0.55		
		VCC = 3.0V VIN = VIH or VIL	IOL = 24mA	—	0.3	0.50		
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max., VO = GND ⁽³⁾	-60	-135	-240	mA		
VH	Input Hysteresis	—	—	150	—	mV		
ICCL	Quiescent Power Supply Current	VCC = Max., VIN = GND or VCC	—	0.1	10	µA		
ICCH								
ICCZ								

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE}_1 = \overline{xOE}_2 = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	50	75	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE}_1 = \overline{xOE}_2 = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.7	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.5	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE}_1 = \overline{xOE}_2 = \text{GND}$ Twenty Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.5	3.7 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2.5	4.1 ⁽⁵⁾	

NOTES:

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- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Conditions ⁽¹⁾	FCT163827A		FCT163827B		FCT163827C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	5.0	1.5	4.4	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	
tpZH tpZL	Output Enable Time xOEx to xYx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	
tPHZ tPLZ	Output Disable Time xOEx to xYx	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.7	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	ns

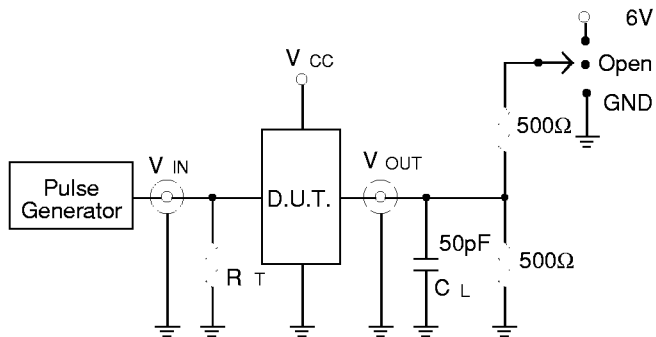
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

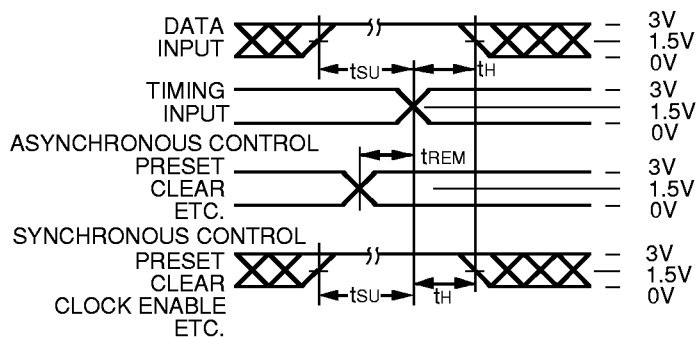
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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DEFINITIONS:

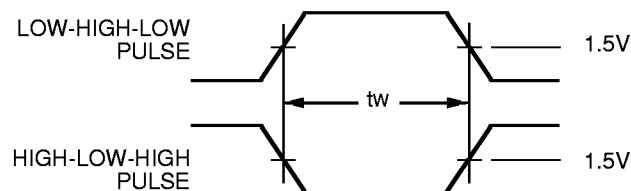
C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



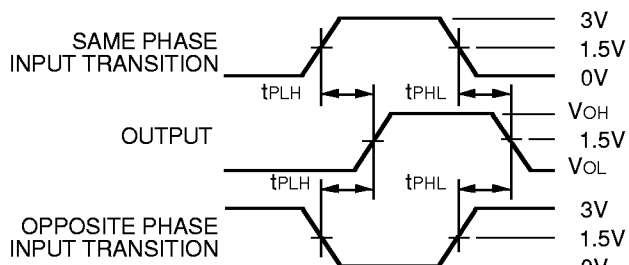
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PULSE WIDTH



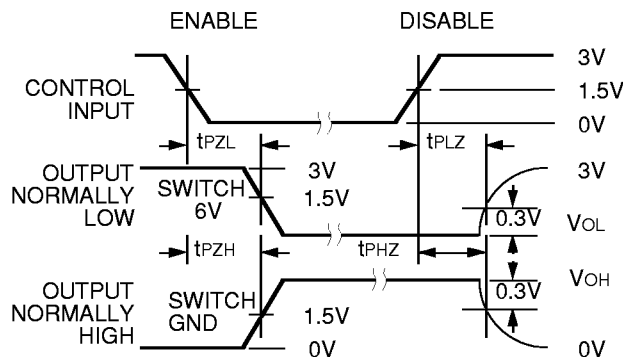
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

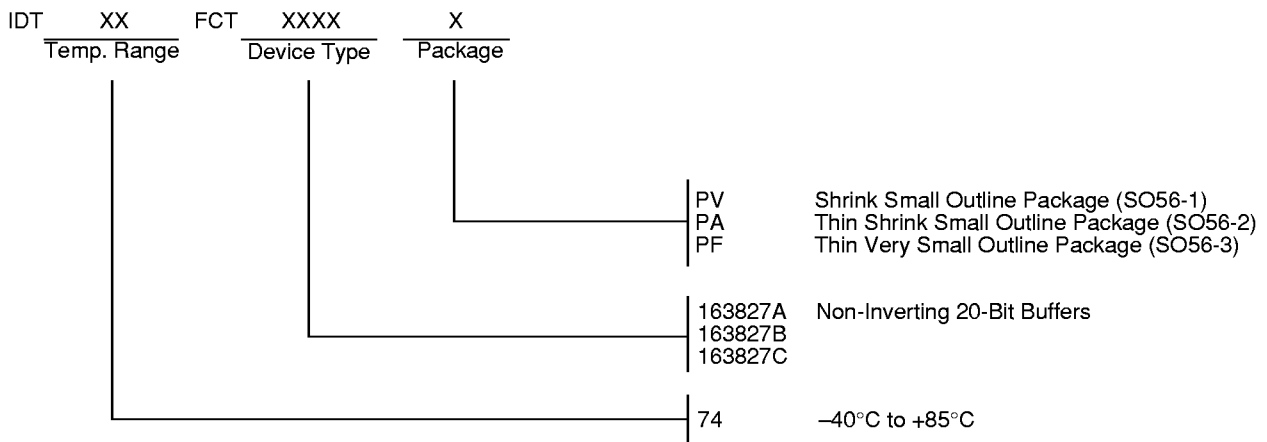


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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_f \leq$ 2.5ns; $t_r \leq$ 2.5ns.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION



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