

# CD74FCT240T, CD74FCT241T, CD74FCT244T, CD74FCT540T, CD74FCT541T, CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T

October 1996

## Fast CMOS Octal Buffer and Line Drivers

### Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs

### Description

These devices are 8-bit wide driver circuits, designed to be used in applications requiring high-speed and high-output drive. Ideal applications would include bus drivers, memory drivers, address drivers, and system clock drivers.

The CD74FCT540T, CD74FCT541T and CD74FCT2541T provide similar driver capabilities, but have their pins physically grouped by function. All inputs are located on one side of the package, while outputs are on the opposite side, allowing for a much simpler and denser board layout.

All CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT240TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541TM	-40 to 85	20 Ld SOIC	M20.3-P

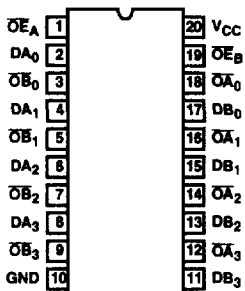
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT541ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2240TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2240ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2244CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2244TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541CTQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

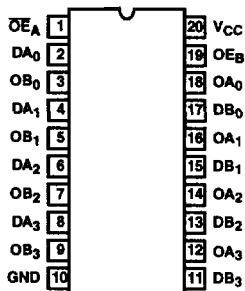
**CD74FCT240T/241T/244T, CD74FCT540T/541T, CD74FCT2240T/2241T/2244T/2541T**

**Pinouts**

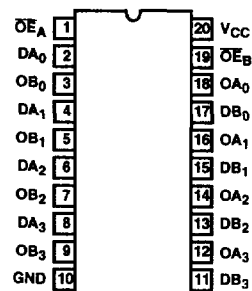
**CD74FCT240T, CD74FCT2240T**  
(SOIC, QSOP)  
TOP VIEW



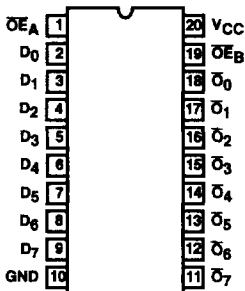
**CD74FCT241T, CD74FCT2241T**  
(SOIC, QSOP)  
TOP VIEW



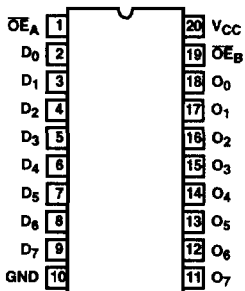
**CD74FCT244T, CD74FCT2244T**  
(SOIC, QSOP)  
TOP VIEW



**CD74FCT540T**  
(SOIC, QSOP)  
TOP VIEW

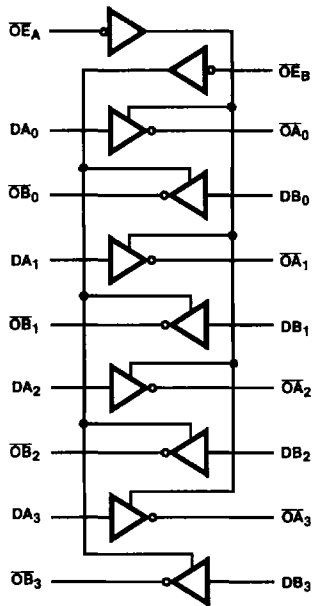


**CD74FCT541T, CD74FCT2541T**  
(SOIC, QSOP)  
TOP VIEW

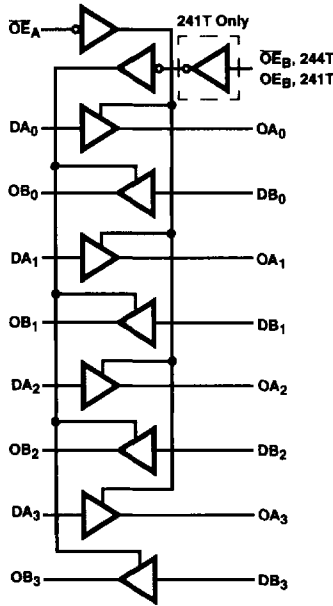


**Functional Block Diagrams**

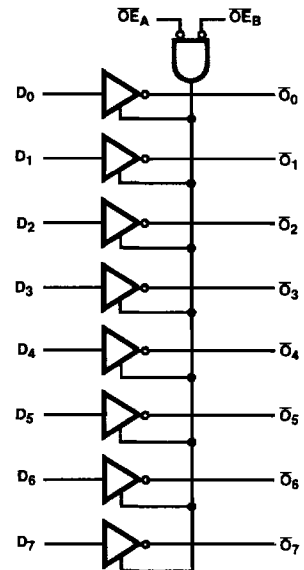
CD74FCT240T, CD74FCT2240T



CD74FCT241T, CD74FCT2241T,  
CD74FCT244T, CD74FCT2244T



CD74FCT540T, CD74FCT541T,  
CD74FCT2541T (Note)



NOTE: The logic diagram shown for the 540T, 541T, 2541T is the non-inverting option.

TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS				
OE <sub>A</sub>	OE <sub>B</sub>	(NOTE 2) OE <sub>B</sub>	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES:

- H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care  
Z = High Impedance
- OE<sub>B</sub> for CD74FCT241T only.

**Pin Descriptions**

PIN NAME	DESCRIPTION
OE <sub>A</sub> , OE <sub>B</sub>	3-State Output Enable Inputs (Active LOW)
OE <sub>B</sub> (NOTE 3)	3-State Output Enable Input (Active HIGH)
D <sub>xx</sub>	Inputs
O <sub>xx</sub>	Outputs
GND	Ground
V <sub>CC</sub>	Power

NOTE:

- OE<sub>B</sub> for CD74FCT241T only.

**CD74FCT240T/241T/244T, CD74FCT540T/541T, CD74FCT2240T/2241T/2244T/2541T**

**Absolute Maximum Ratings**

DC Input Voltage ..... -0.5V to 7.0V  
 DC Output Current ..... 120mA

**Operating Conditions**

Operating Temperature Range ..... -40°C to 85°C  
 Supply Voltage to Ground Potential  
 Inputs and Vcc Only ..... -0.5V to 7.0V  
 Supply Voltage to Ground Potential  
 Outputs and D/O Only ..... -0.5V to 7.0V

**Thermal Information**

Thermal Resistance (Typical, Note 4)  $\theta_{JA}$  (°C/W)  
 SOIC Package ..... 87  
 QSOP Package ..... 110  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- 4.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS	
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$							
Output HIGH Voltage	$V_{OH}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15.0\text{mA}$	2.4	3.0	-	V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 64\text{mA}$	-	0.3	0.50	V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 12\text{mA}$ (25 $\Omega$ series)	-	0.3	0.50	V
Input HIGH Voltage	$V_{IH}$	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	$V_{IL}$	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	$I_{IH}$	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1	$\mu\text{A}$
Input LOW Current	$I_{IL}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1	$\mu\text{A}$
High Impedance Output Current	$I_{OZH}$	$V_{CC} = \text{Max}$	$V_{OUT} = 2.7\text{V}$			1	$\mu\text{A}$
	$I_{OZL}$		$V_{OUT} = 0.5\text{V}$			-1	$\mu\text{A}$
Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{Min}$ , $I_{IN} = -18\text{mA}$		-	-0.7	-1.2	V
Short Circuit Current	$I_{OS}$	$V_{CC} = \text{Max}$ (Note 7), $V_{OUT} = \text{GND}$		-60	-120	-	mA
Power Down Disable	$I_{OFF}$	$V_{CC} = \text{GND}$ , $V_{OUT} = 4.5\text{V}$		-	-	100	$\mu\text{A}$
Input Hysteresis	$V_H$			-	200	-	mV
<b>CAPACITANCE</b> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$							
Input Capacitance (Note 8)	$C_{IN}$	$V_{IN} = 0\text{V}$		-	6	10	pF
Output Capacitance (Note 8)	$C_{OUT}$	$V_{OUT} = 0\text{V}$		-	8	12	pF
<b>POWER SUPPLY SPECIFICATIONS</b>							
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	500	$\mu\text{A}$
Supply Current per Input at TTL HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 9)	-	0.5	2.5	mA

**4**

OCTAL 5V FCT  
5V FCT 25 $\Omega$

**CD74FCT240T/241T/244T, CD74FCT540T/541T, CD74FCT2240T/2241T/2244T/2541T**

**Electrical Specifications (Continued)**

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6)	MAX	UNITS
					TYP		
Supply Current per Input per MHz (Note 10)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open $\overline{OE}_A$ or $\overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ , $\overline{OE}_B = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 12)	$I_C$	$V_{CC} = \text{Max}$ , Outputs Open $f_I = 10\text{MHz}$ , 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ , $\overline{OE}_B = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 11)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.8	4.5 (Note 11)	mA
		$V_{CC} = \text{Max}$ , Outputs Open $f_I = 2.5\text{MHz}$ , 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ , $\overline{OE}_B = V_{CC}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.0	6.0 (Note 11)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	5.0	14.0 (Note 11)	mA

**Switching Specifications Over Operating Range**

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		(NOTE 16) DT		UNIT
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
			<b>CD74FCT240T, CD74FCT2240T</b>								
Propagation Delay $D_N$ to $\overline{O}_N$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	ns
Output Enable Time $\overline{OE}_X$ to $\overline{O}_N$	$t_{PZH}$ , $t_{PZL}$		1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to $\overline{O}_N$	$t_{PHZ}$ , $t_{PLZ}$		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	ns
<b>CD74FCT241T, CD74FCT2241T</b>											
Propagation Delay $D_N$ to $O_N$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
Output Enable Time $\overline{OE}_A/\overline{OE}_B$ to $O_N$	$t_{PZH}$ , $t_{PZL}$		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_A/\overline{OE}_B$ to $O_N$	$t_{PHZ}$ , $t_{PLZ}$		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns
<b>CD74FCT244T, CD74FCT2244T</b>											
Propagation Delay $D_N$ to $O_N$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
Output Enable Time $\overline{OE}_X$ to $O_N$	$t_{PZH}$ , $t_{PZL}$		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to $O_N$	$t_{PHZ}$ , $t_{PLZ}$		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns

Switching Specifications Over Operating Range (Continued)

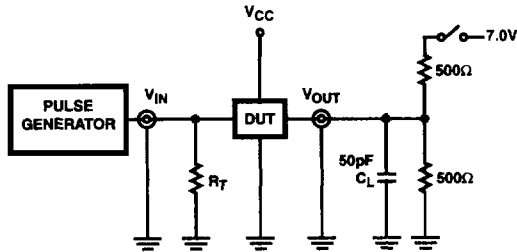
PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		(NOTE 16) DT		UNIT
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
<b>CD74FCT540T</b>											
Propagation Delay $D_N$ to $\bar{O}_N$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50pF$ $R_L = 500\Omega$	1.5	5.5	1.5	4.8	1.5	4.3	1.5	3.8	ns
Output Enable Time $\bar{O}E_X$ to $\bar{O}_N$	$t_{PZH}$ , $t_{PZL}$		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.2	ns
Output Disable Time (Note 15) $\bar{O}E_X$ to $\bar{O}_N$	$t_{PHZ}$ , $t_{PLZ}$		1.5	6.0	1.5	5.6	1.5	5.2	1.5	5.2	ns
<b>CD74FCT541T, CD74FCT2541T</b>											
Propagation Delay $D_N$ to $O_N$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50pF$ $R_L = 500\Omega$	1.5	6.0	1.5	4.8	1.5	4.1	1.5	3.8	ns
Output Enable Time $\bar{O}E_X$ to $O_N$	$t_{PZH}$ , $t_{PZL}$		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.2	ns
Output Disable Time (Note 15) $\bar{O}E_X$ to $O_N$	$t_{PHZ}$ , $t_{PLZ}$		1.5	6.5	1.5	5.6	1.5	5.2	1.5	5.2	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $25^\circ C$  ambient and maximum loading, except as noted.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_I$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_I$   
 All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Suffix DT Speed for types FCT240T/241T/244T/540T/541T only.

4  
OCTAL 5V FCT  
5V FCT 25Ω

**Test Circuits and Waveforms**



SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

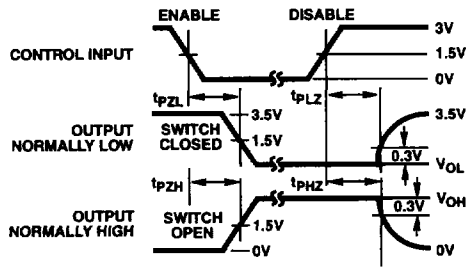
**DEFINITIONS:**

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

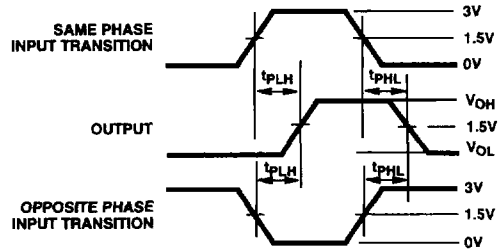
**NOTE:**

17. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f, t_r \leq 2.5\text{ns}$ .

**FIGURE 1. TEST CIRCUIT**



**FIGURE 2. ENABLE AND DISABLE TIMING**



**FIGURE 3. PROPAGATION DELAY**