



Am29827/Am29828

High Performance Buffers

DISTINCTIVE CHARACTERISTICS

- High-speed buffers and inverters
 - Noninverting $t_{PD} = 5.0$ ns typ
 - Inverting $t_{PD} = 4.5$ ns typ
- 200 mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and -down
- Outputs have Schottky clamp to ground
- 48 mA commercial I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0 V and 2.4 V
- 24-pin 0.3" space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted OXide isolated process

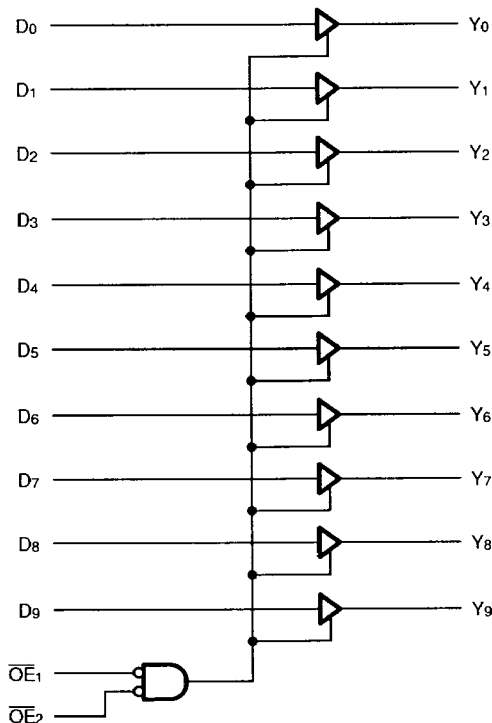
GENERAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200 mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

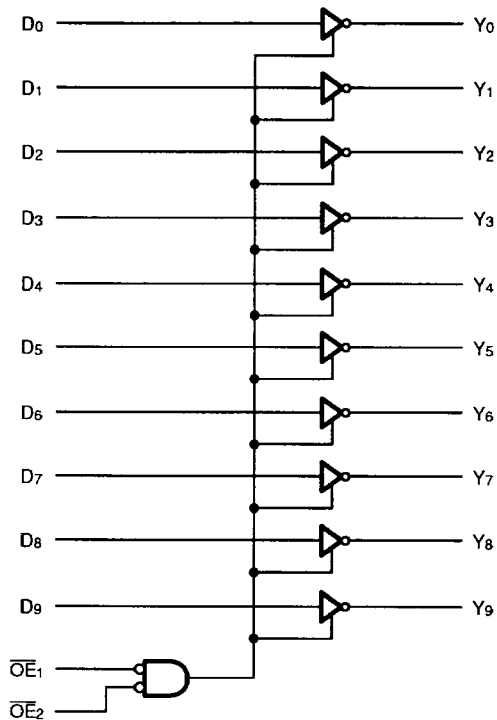
BLOCK DIAGRAMS

Am29827



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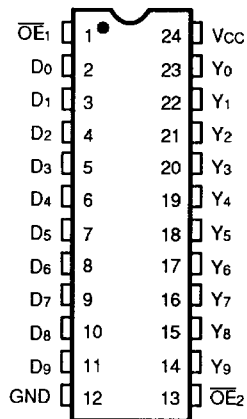
BLOCK DIAGRAMS (Continued)
Am29828



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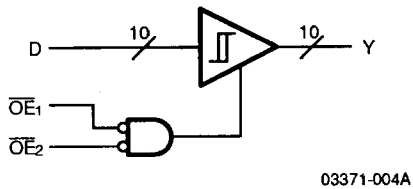
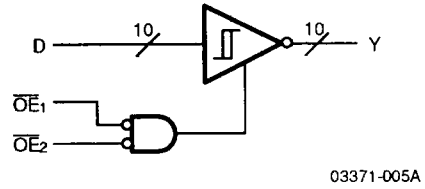
CONNECTION DIAGRAM

DIP



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LOGIC SYMBOLS

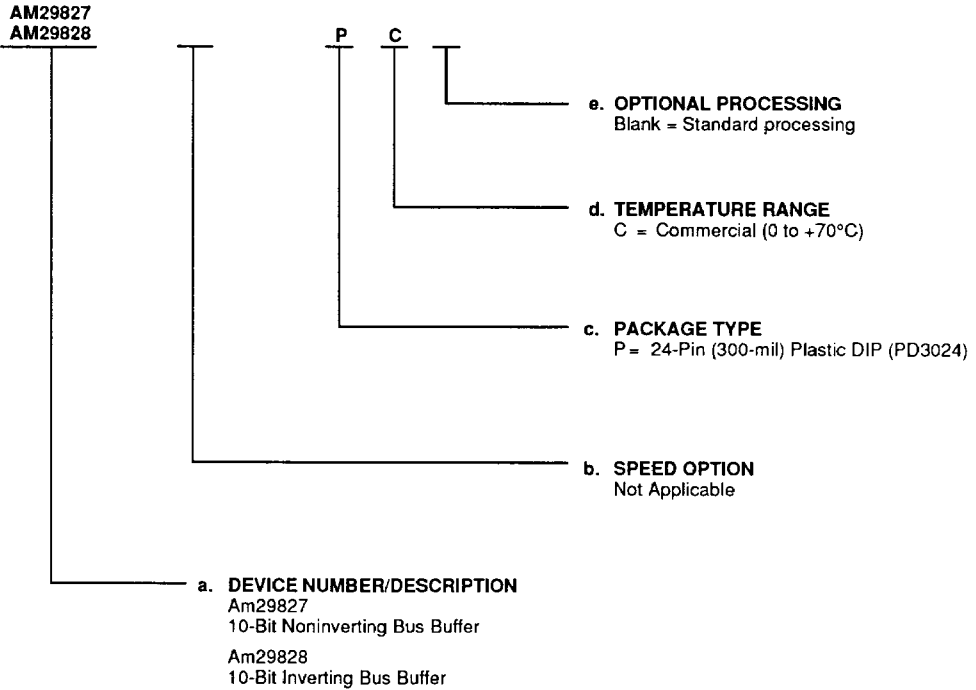
**Am29827 (Noninverting)****Am29828 (Inverting)**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM29827	PC
AM29828	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION \overline{OE}_i

When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are HI-Z.

 Y_i

10-bit data output.

 D_i

10-bit data input.

FUNCTION TABLES**Am29827 (Noninverting)**

Inputs		Outputs	Function
\overline{OE}	D_i	Y_i	
L	H	H	Transparent
L	L	L	Transparent
H	X	Z	HI-Z

Am29828 (Inverting)

Inputs		Outputs	Function
\overline{OE}	D_i	Y_i	
L	H	L	Transparent
L	L	H	Transparent
H	X	Z	HI-Z

H = HIGH

L = LOW

X = Don't Care

Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Output for High Output State	-1.5 V to +5.5 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	-30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature, (T _A)	0°C to +70°C
Supply Voltage, (V _{CC})	5.0 V ± 10% 4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 4.5 V		2.4	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15 mA		
V _{OL}	Output LOW Voltage	V _{CC} = 4.5 V		2.0	V
		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA		
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0		V
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		0.8	V
V _I	Input Clamp Voltage	V _{CC} = 4.5 V, I _{IN} = -18 mA		-1.2	V
V _{HYST}	Input Hysteresis	Output under test connected to AC load test circuit	200		mV
I _{IL}	Input LOW Current	V _{CC} = 5.5 V, V _{IN} = 0.4 V		-1.0	mA
I _{IH}	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 2.7 V		50	μA
I _I	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 5.5 V		1.0	mA
I _{OZH}	Output Off-State Output Current (HI-Z)	V _{CC} = 5.5 V, V _O = 2.4 V		50	μA
I _{OZL}	Output Off-State Output Current (HI-Z)	V _{CC} = 5.5 V, V _O = 0.4 V		-50	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5.5 V	-75	-250	mA
I _{CC}	Supply Current	V _{CC} = 5.5 V		80	mA
		Outputs Open	Over Temperature Range +70°C	75	

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Typ.	Max.	Unit
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	$C_L = 50\text{ pF}$		4.8	6.0	ns
t_{PHL}				5.2	6.2	ns
t_{PLH}		$C_L = 300\text{ pF}$		8.0	11	ns
t_{PHL}				10.8	13.2	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	$C_L = 50\text{ pF}$		4.0	5.2	ns
t_{PHL}				4.9	5.9	ns
t_{PLH}		$C_L = 300\text{ pF}$		7.3	10	ns
t_{PHL}				10.5	12.9	ns
t_{ZH}	Output Enable Time \overline{OE} to Y_i	$C_L = 50\text{ pF}$		6.5	12	ns
t_{ZL}				9.5	12	ns
t_{ZH}		$C_L = 300\text{ pF}$		11	17	ns
t_{ZL}				18	21	ns
t_{HZ}	Output Disable Time \overline{OE} to Y_i	$C_L = 5\text{ pF}$		3.5	8.0	ns
t_{LZ}				3.5	8.0	ns
t_{HZ}		$C_L = 50\text{ pF}$		11.2	16	ns
t_{LZ}				4.5	11	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

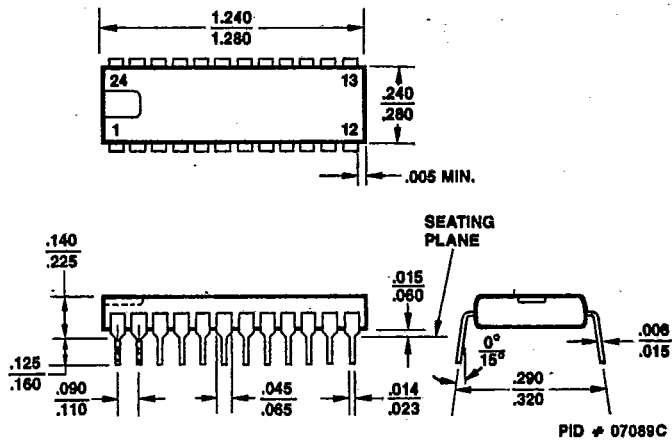
Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	$C_L = 50\text{ pF}$		8	ns
t_{PHL}				8	ns
t_{PLH}		$C_L = 300\text{ pF}$		15	ns
t_{PHL}				15	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	$C_L = 50\text{ pF}$		7.0	ns
t_{PHL}				7.5	ns
t_{PLH}		$C_L = 300\text{ pF}$		14	ns
t_{PHL}				14	ns
t_{ZH}	Output Enable Time \overline{OE} to Y_i	$C_L = 50\text{ pF}$		15	ns
t_{ZL}				15	ns
t_{ZH}		$C_L = 300\text{ pF}$		20	ns
t_{ZL}				23	ns
t_{HZ}	Output Disable Time \overline{OE} to Y_i	$C_L = 5\text{ pF}$		9	ns
t_{LZ}				9	ns
t_{HZ}		$C_L = 50\text{ pF}$		17	ns
t_{LZ}				12	ns

*See Test Circuit and Waveforms (Chapter 2).

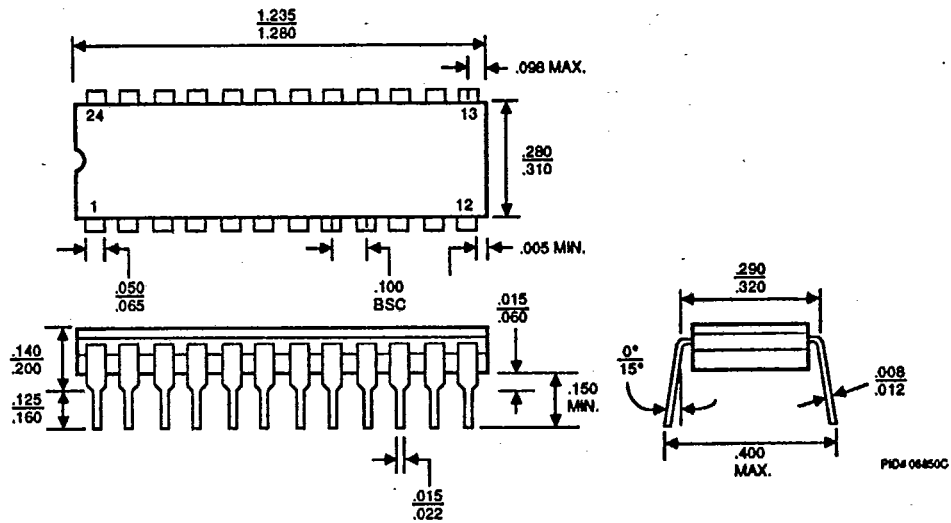
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

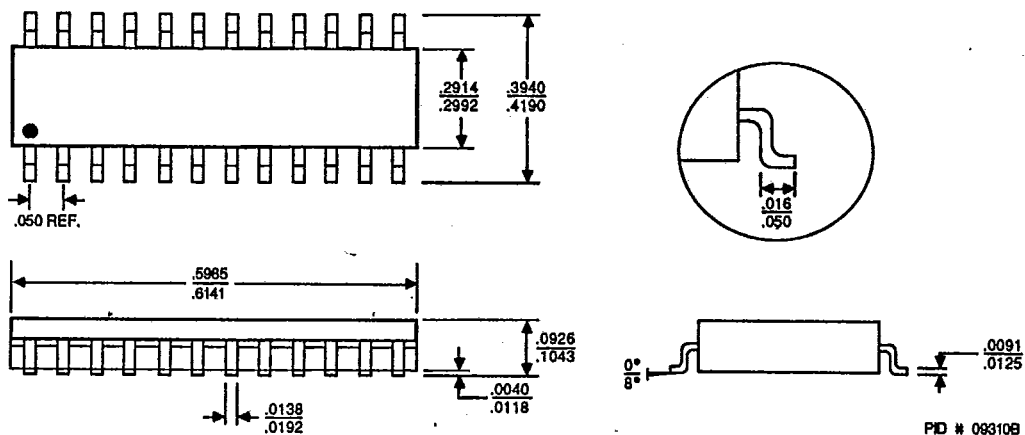


*For reference only.

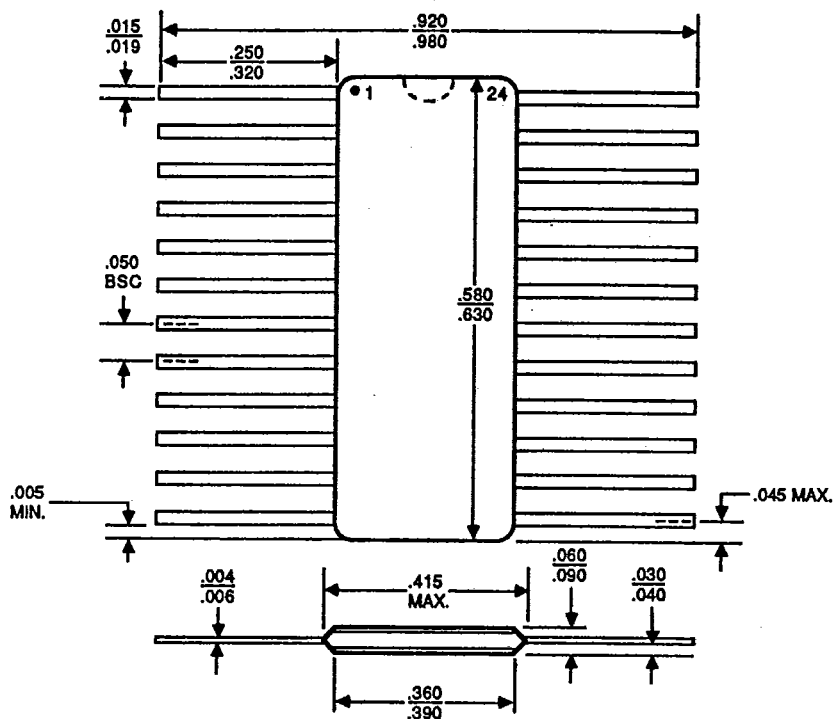
PACKAGE OUTLINES (Cont'd.)

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SO 024



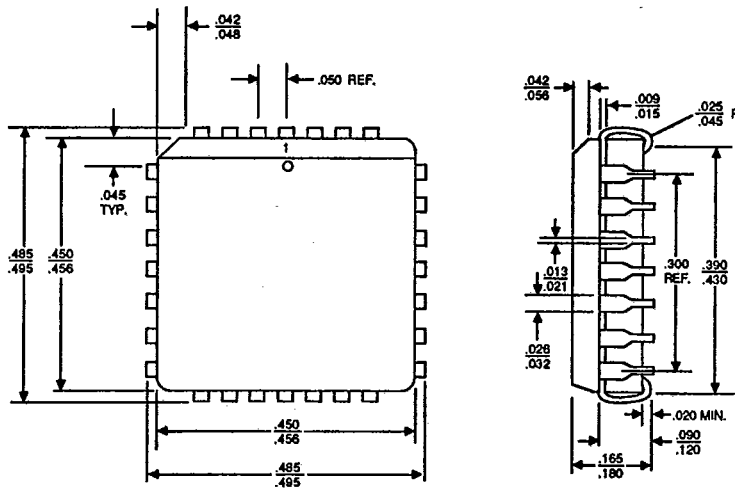
CFM024



PACKAGE OUTLINES (Cont'd.)

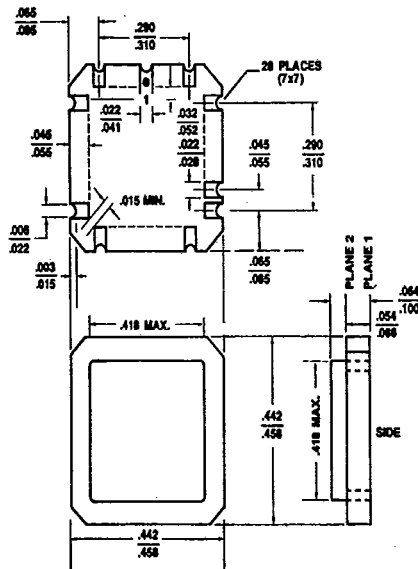
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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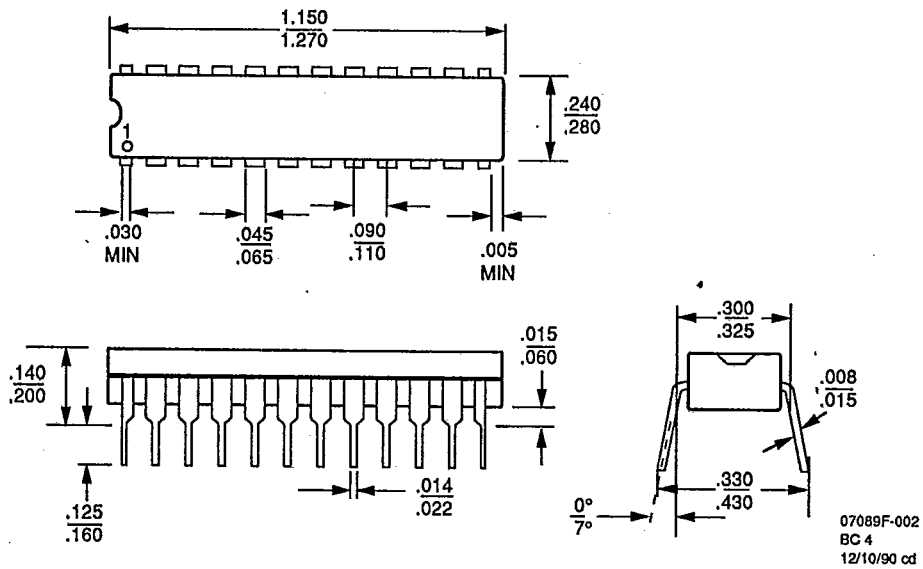


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PD3024
24-Pin 300-mil Plastic SKINNYDIP

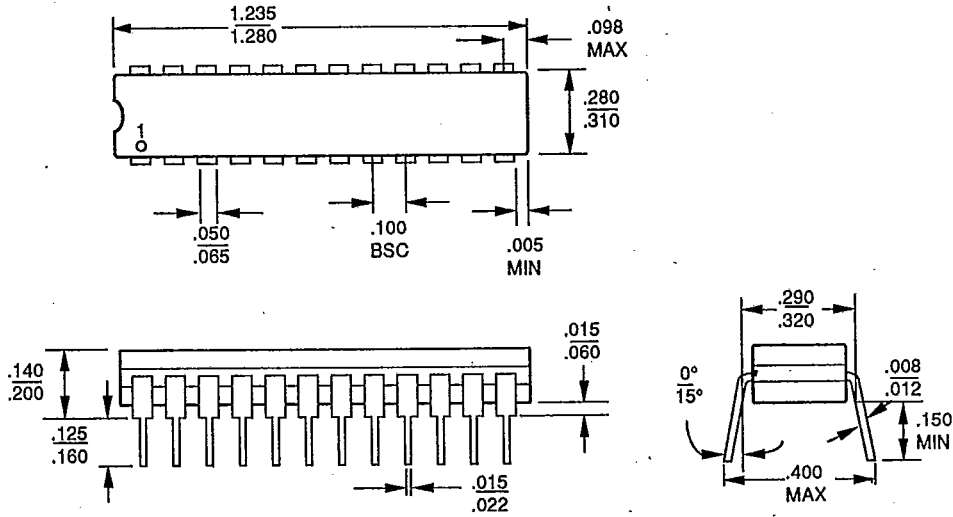
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Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

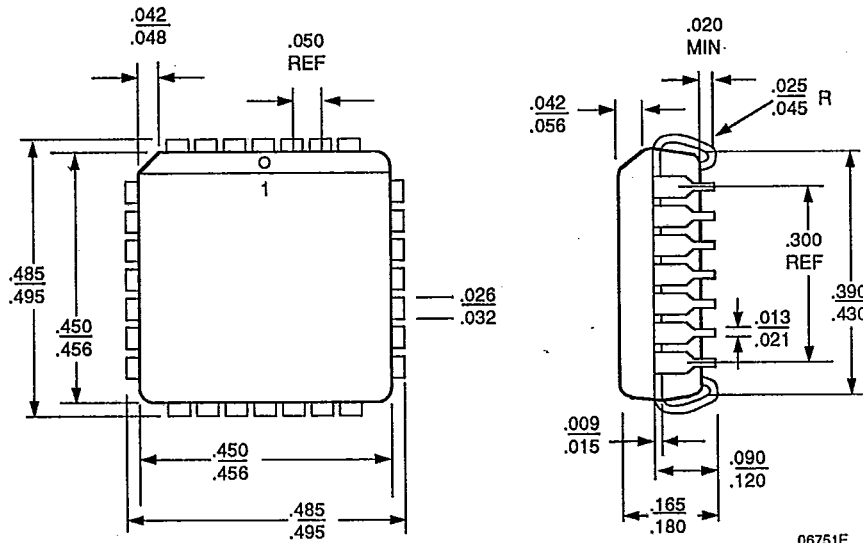
T-90-20

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



06850C

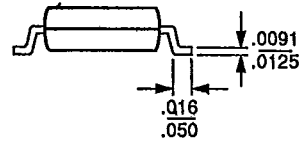
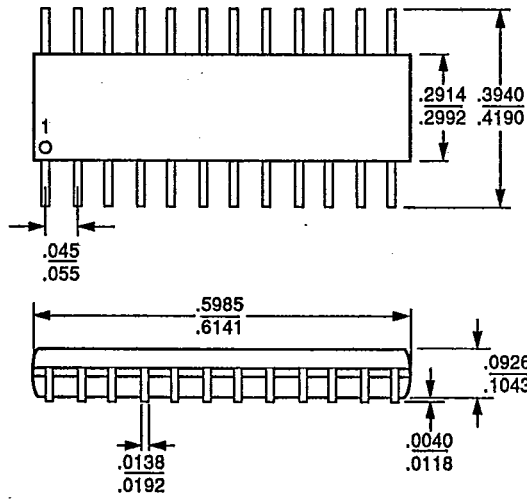
PL 028
28-Pin Plastic Leaded Chip Carrier



06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20



09310B