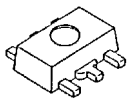
Low Output Voltage Low Dropout Regulator

■ GENERAL DESCRIPTION

The NJM2841 is a low output voltage, low drop out regulators.
It delivers up to 500mA output current with the output voltage of 0.8 to 2.5V.
The use of an external bias voltage can improve the transient response and the ripple rejection characteristics while maintaining minimum input to output voltage.

■ PACKAGE OUTLINE

NJM2841F

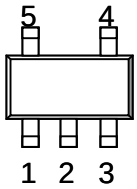


NJM2841U2

■ FEATURES

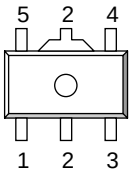
- Output Voltage Range 0.8V to 2.5V
- High Ripple Rejection 86 dB typ. (V_O=1.2V version)
- Output Noise Voltage V_{NO}=40μVrms(V_O=1.2V version)
- Output Current I_O(min)=500mA
- High Precision Output V_O±1.0%
- Dual Supply Voltage Type V_{IN}, V_{BIAS}(sequence free)
- High Stability for Load 0.002%/mA (max)
- Output Capacitor with 4.7μF ceramic capacitor
- Low Dropout Voltage 0.1V typ. @I_O=300mA
- ON/OFF Control
- Built-in Thermal Overload Protection and Over Current Protection
- Bipolar Technology
- Package Outline SOT-23-5, SOT-89-5

■ PIN CONNECTION



1. CONTROL
2. GND
3. V_{OUT}
4. V_{IN}
5. V_{BIAS}

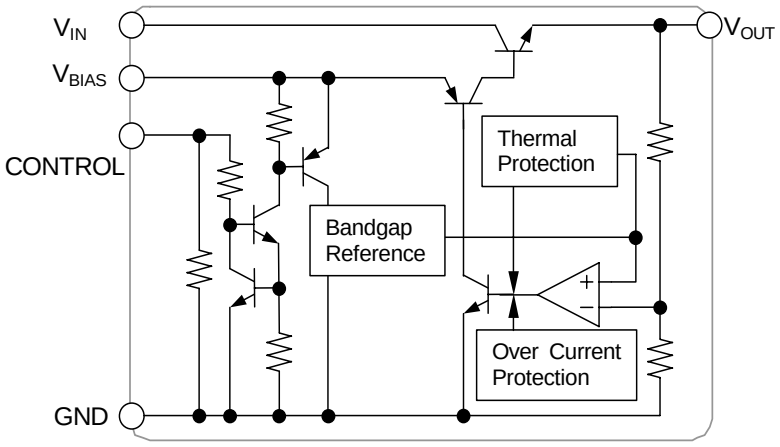
NJM2841F



1. V_{OUT}
2. GND
3. CONTROL
4. V_{BIAS}
5. V_{IN}

NJM2841U2

■ BLOCK DIAGRAM



■ OUTPUT VOLTAGE RANK LIST

Device Name	V_{out}	Device Name	V_{out}	Device Name	V_{out}
NJM2841F008	0.8V	NJM2841F017	1.7V	NJM2841U2-012	1.2V
NJM2841F009	0.9V	NJM2841F018	1.8V		
NJM2841F010	1.0V	NJM2841F019	1.9V		
NJM2841F011	1.1V	NJM2841F020	2.0V		
NJM2841F012	1.2V	NJM2841F021	2.1V		
NJM2841F013	1.3V	NJM2841F022	2.2V		
NJM2841F014	1.4V	NJM2841F023	2.3V		
NJM2841F015	1.5V	NJM2841F024	2.4V		
NJM2841F016	1.6V	NJM2841F025	2.5V		

Output Voltage Range: 0.8V to 2.5V (0.1V step)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	RATINGS		UNIT
Input Voltage	V_{IN}	+10		V
Bias Voltage	V_{BIAS}	+10		V
Control Voltage	V_{CONT}	+10		V
Power Dissipation	P_D	SOT-23-5	480(*1)	mW
			640(*2)	
		SOT-89-5	625(*3)	
			2400(*4)	
Operating Temperature	Topr	-40 ~ +85		°C
Storage Temperature	Tstg	-50 ~ +150		°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

(*3): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm^2)

(*4): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ BIAS VOLTAGE RANGE

V_{BIAS}= +2.5V to +10V (V_O<1.5V)

V_{BIAS}= V_O+1V to +10V (V_O≥1.5V)

■ ELECTRICAL CHARACTERISTICS

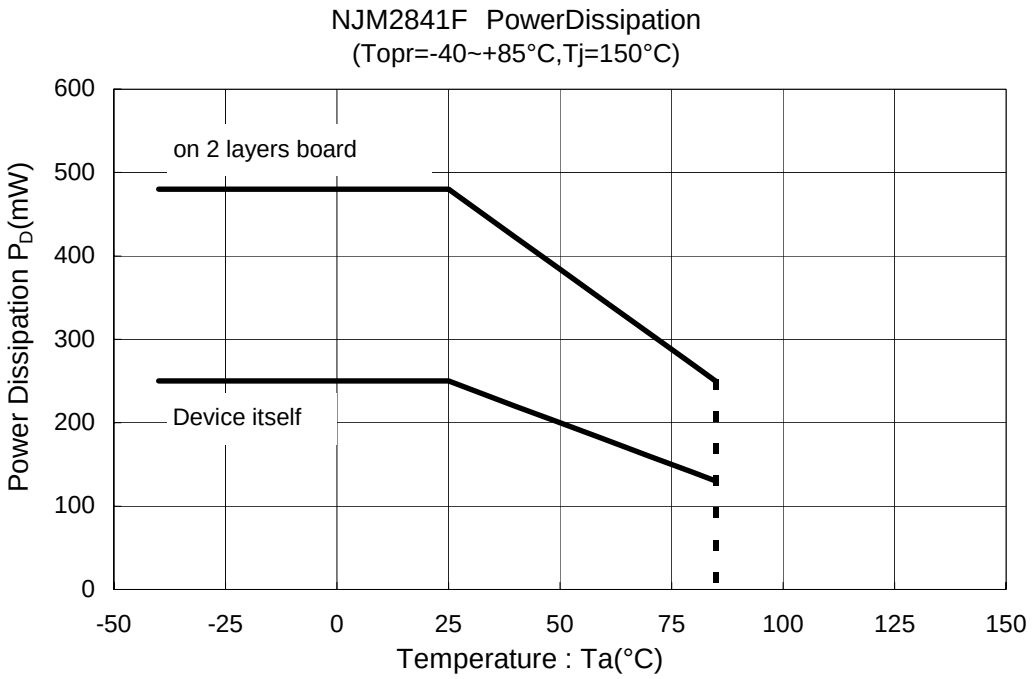
(V_{BIAS}=2.5V(Vo≥1.5V : V_{BIAS}=Vo+1V), V_{IN}=Vo+1V, C_{BIAS}=0.1μF, C_{IN}=4.7μF, Co=4.7μF, Ta=25°C)

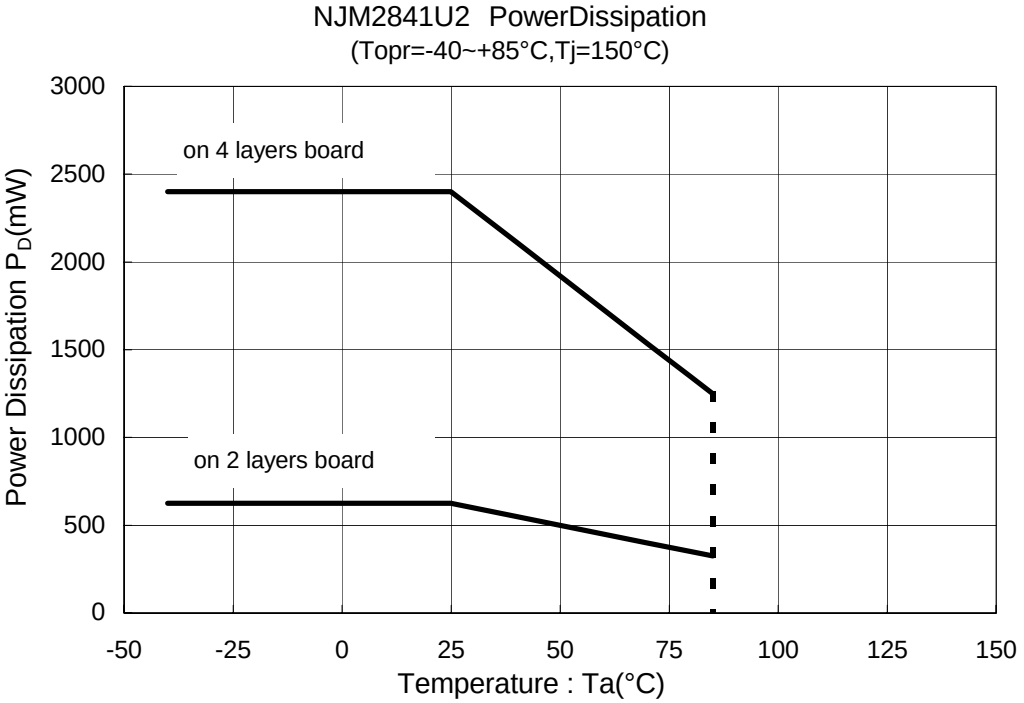
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	I_O=30mA	-1.0%	-	+1.0%	V
Unloaded Bias Current	I_{BIAS}	I_O=0mA, except I_{CONT}	-	180	300	μA
Unloaded Input Current	I_{IN}	I_O=0mA, except I_{CONT}	-	-	20	μA
Bias Current at Control OFF	$I_{BIAS(OFF)}$	V_{CONT}=0V	-	-	100	nA
Input Current at Control OFF	$I_{IN(OFF)}$	V_{CONT}=0V	-	-	100	nA
Output Current	I_O	V_O x 0.9V	500	650	-	mA
Line Regulation 1 (V_{BIAS})	$\Delta V_O/\Delta V_{BIAS}$	V_{BIAS}=2.5V to V_O+6V(V_O<1.5V) V_{BIAS}=V_O+1V to V_O+6V(V_O≥1.5V) I_O=30mA	-	-	0.10	%/V
Line Regulation 2 (V_{IN})	$\Delta V_O/\Delta V_{IN}$	V_{IN}=V_O+1V to V_O+6V, I_O=30mA	-	-	0.10	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_O=30 to 500mA	-	-	0.002	%/mA
Dropout Voltage	ΔV_{I-O}	I_O=300mA	-	0.10	0.18	V
Ripple Rejection Ratio 1 (V_{BIAS})	RR1(V_{BIAS})	V_{BIAS}=3.5V, e_{BIAS}=200mVrms, f=1kHz, I_O=10mA	Refer to Table 1			dB
Ripple Rejection Ratio 2 (V_{IN})	RR2(V_{IN})	e_{IN}=200mVrms, f=1kHz, I_O=10mA	Refer to Table 1			dB
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta Ta$	Ta=0 to +85°C, I_O=10mA	-	±50	-	ppm/°C
Output Noise Voltage	V_{NO}	f=10Hz to 80kHz, I_O=10mA	Refer to Table 1			μVrms
Control Current	I_{CONT}	V_{CONT}=1.6V	-	3	12	μA
Control Voltage for ON-state	$I_{CONT(ON)}$		1.6	-	-	V
Control Voltage for OFF-state	$V_{CONT(ON)}$		-	-	0.6	V
Bias Voltage	V_{BIAS}		-	-	10	V
Input Voltage	V_{IN}		-	-	9	V

• Table1

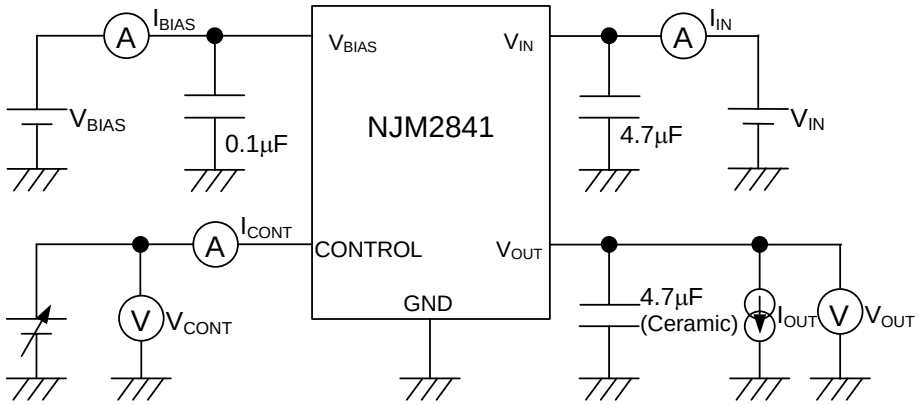
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Ripple Rejection Ratio 1 (V_{BIAS})	RR(V_{BIAS})	V_{BIAS}=3.5V, e_{BIAS}=200mVrms, f=1kHz, Io=10mA	V_O=0.8V	-	80	-	dB
			V_O=0.9V	-	80	-	
			V_O=1.0V	-	79	-	
			V_O=1.2V	-	77	-	
			V_O=1.5V	-	75	-	
		V_{BIAS}=4.5V, e_{BIAS}=200mVrms, f=1kHz, Io=10mA	V_O=2.5V	-	70	-	
Ripple Rejection Ratio 2 (V_{IN})	RR(V_{IN})	e_{in}=200mVrms, f=1kHz, Io=10mA	V_O=0.8V	-	87	-	dB
			V_O=0.9V	-	87	-	
			V_O=1.0V	-	87	-	
			V_O=1.2V	-	86	-	
			V_O=1.5V	-	85	-	
			V_O=2.5V	-	75	-	
Output Noise Voltage	V_{NO}	f=10Hz~80kHz, Io=10mA,	V_O=0.8V	-	27	-	μVrms
			V_O=0.9V	-	30	-	
			V_O=1.0V	-	34	-	
			V_O=1.2V	-	40	-	
			V_O=1.5V	-	48	-	
			V_O=2.5V	-	75	-	

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



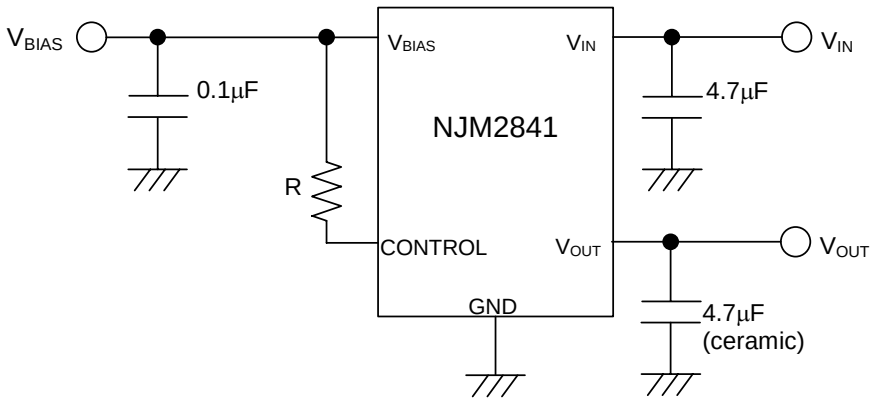


■ TEST CIRCUIT



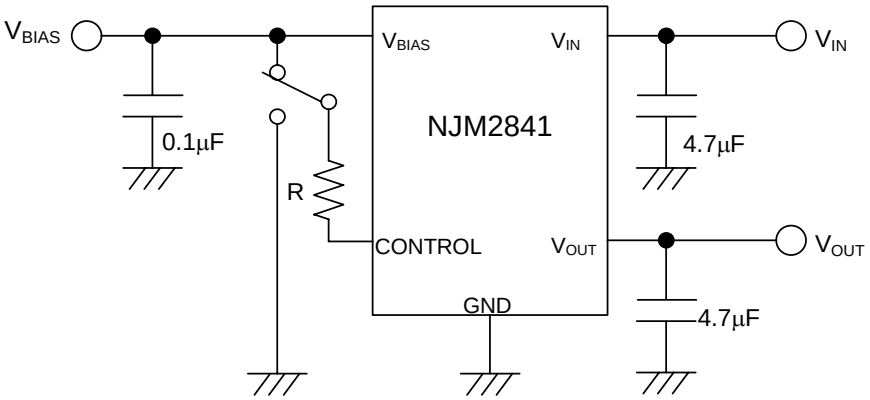
■ TYPICAL APPLICATION

a) In case of where ON/OFF control is not required:



Connect control pin to V_{BIAS} pin.
Though the I_{CONT} decreases by inserting "R" to between Control pin and V_{BIAS} pin, the minimum operating voltage is increased due to the resistor "R".

b) In use of ON/OFF control:



State of control pin:
"H" → output is enabled.
"L" or "open" → output is disabled.

* Bias Capacitor C_{BIAS} and an Input Capacitor C_{IN}

C_{BIAS} and C_{IN} are required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use recommended C_{BIAS} and C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between V_{BIAS} - GND, V_{IN} - GND as shortest path as possible to avoid the problem.

*Output Capacitor C_O

Output capacitor (C_O) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

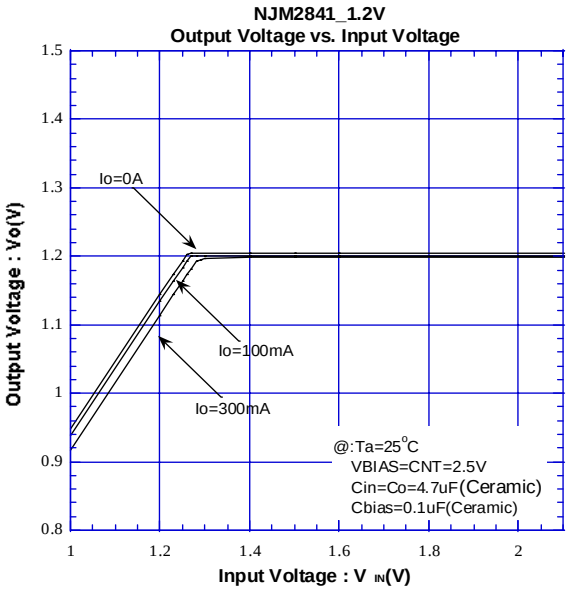
On the other hand, Use of a larger C_O reduces output noise and ripple output, and also improves output transient response when rapid load change.

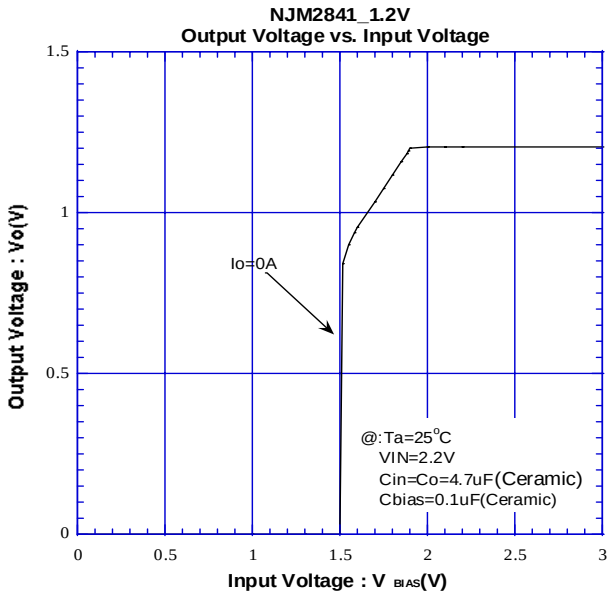
Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation

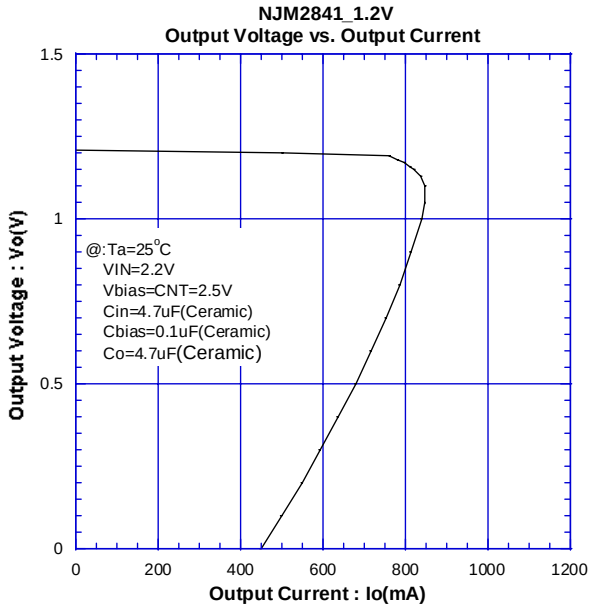
In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

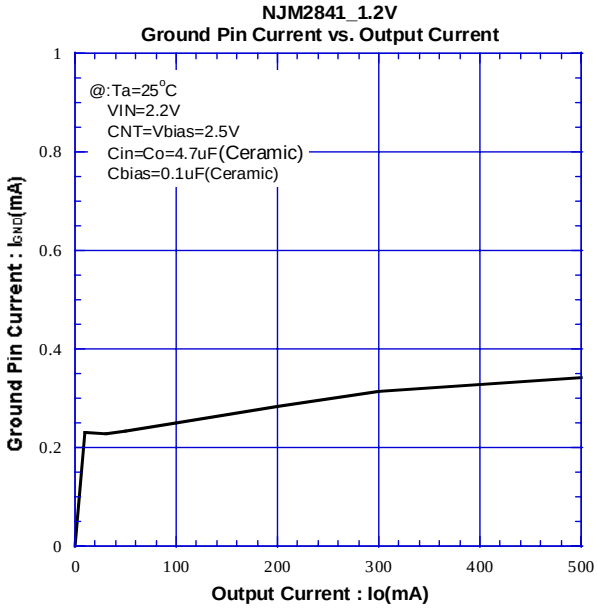
When selecting C_O, recommend that have withstand voltage margin against output voltage and superior temperature characteristic though this product is designed stability works with wide range ESR of capacitor including low ESR products.

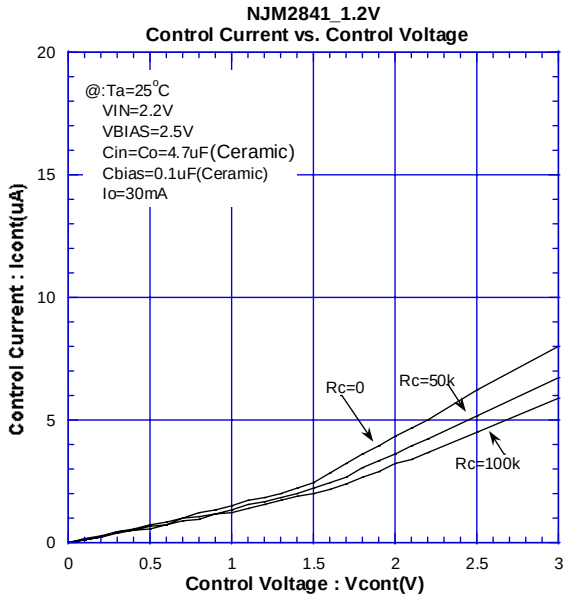
■ TYPICAL CHRACTERISTICS

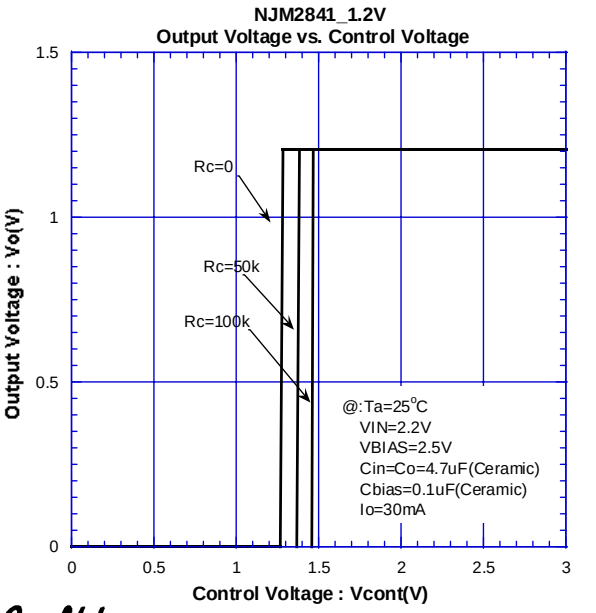




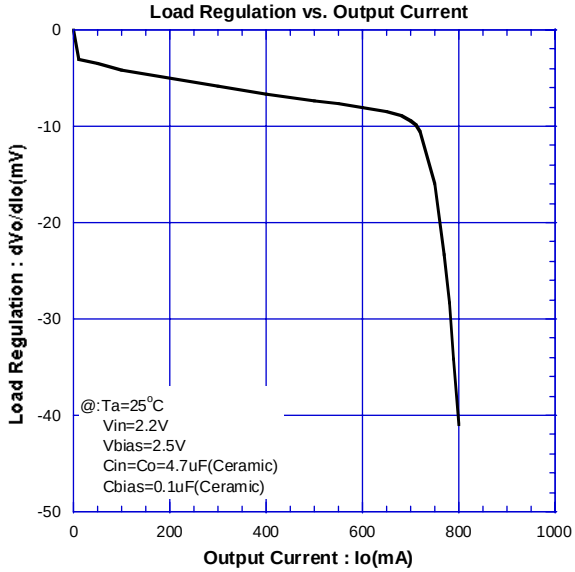




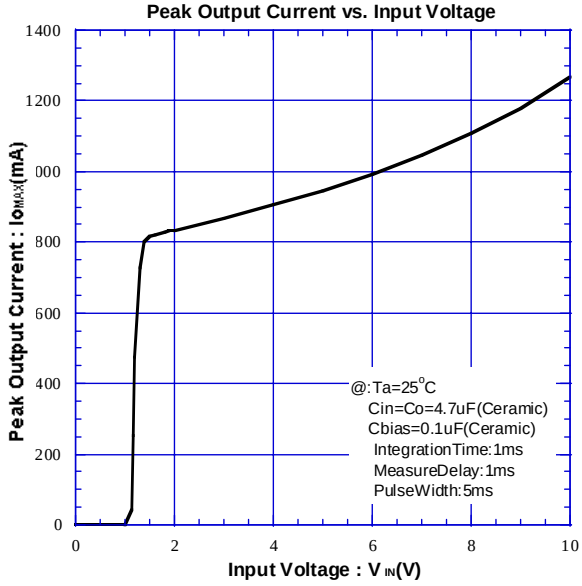




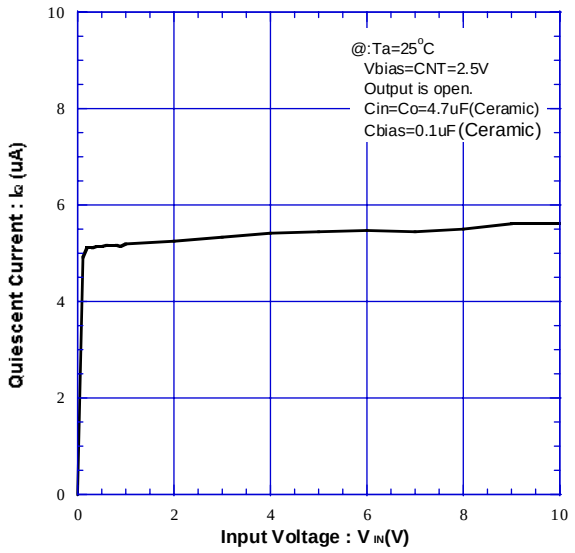
NJM2841_1.2V
Load Regulation vs. Output Current



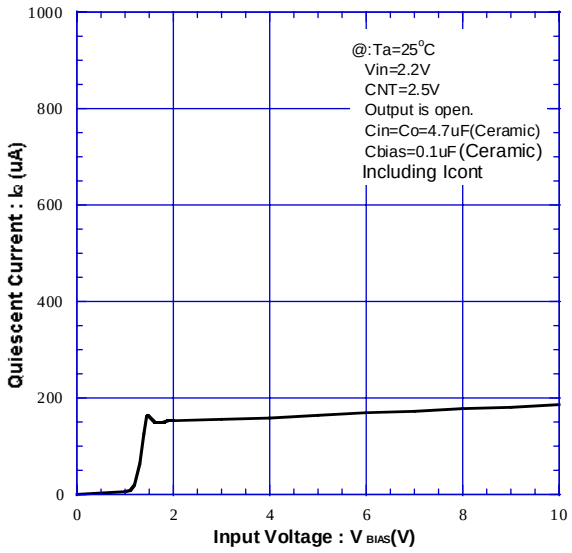
NJM2841_1.2V
Peak Output Current vs. Input Voltage



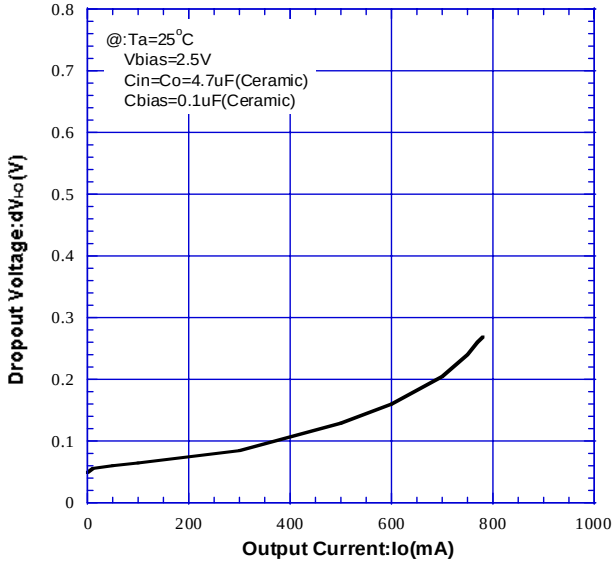
NJM2841_1.2V
Quiescent Current v.s. Input Voltage



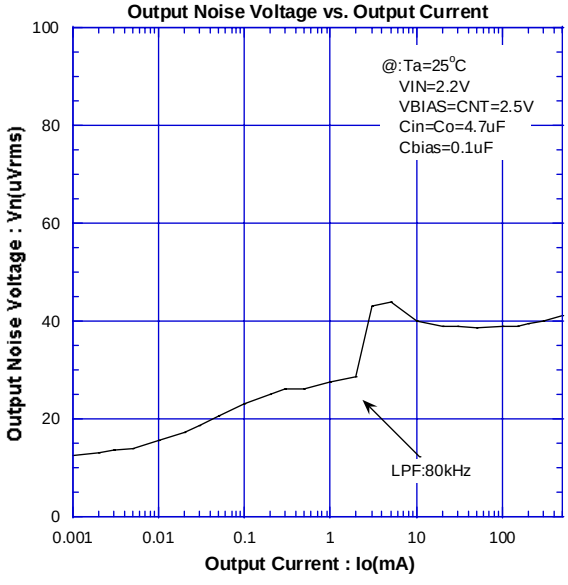
NJM2841_1.2V
Quiescent Current v.s. Input Voltage



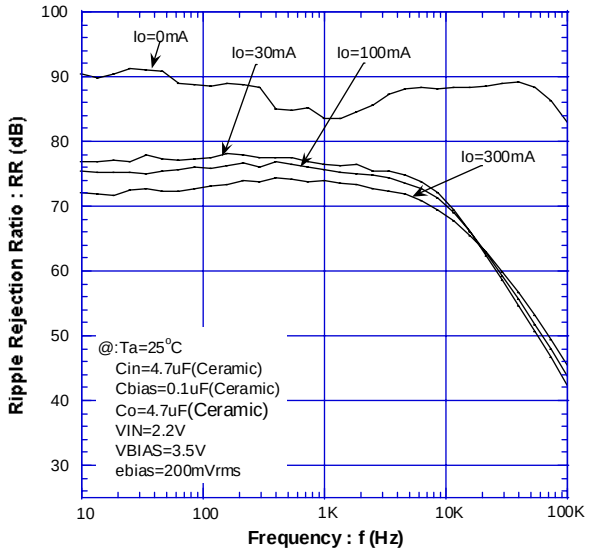
NJM2841_1.2V
Dropout Voltage vs. Output Current



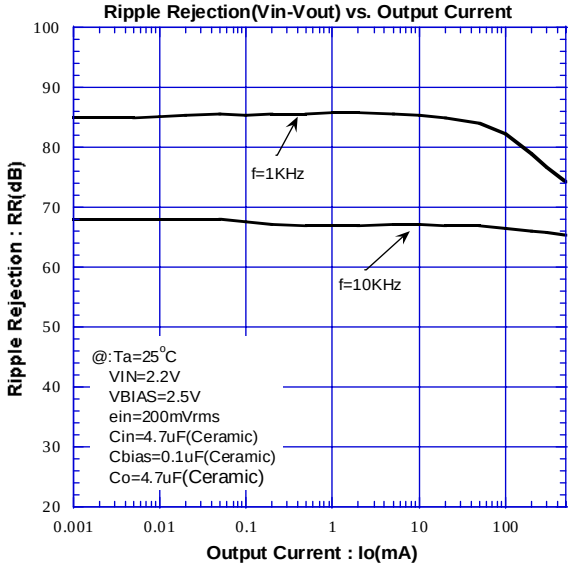
NJM2841_1.2V
Output Noise Voltage vs. Output Current



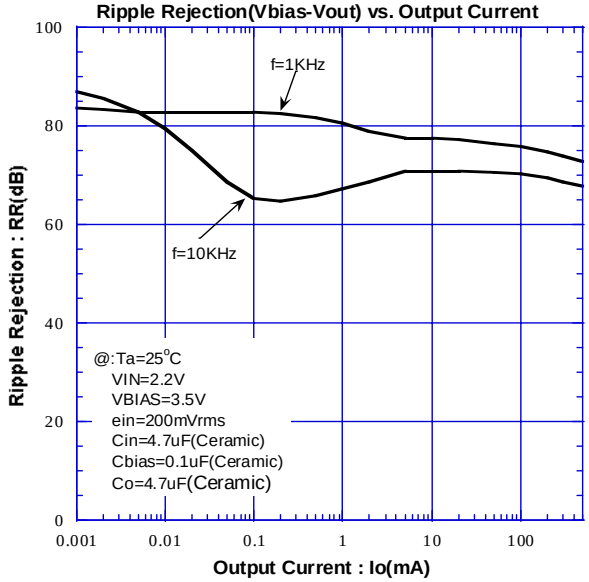
NJM2841_1.2V
Ripple Rejection Ratio[Vbias] v.s. Frequency



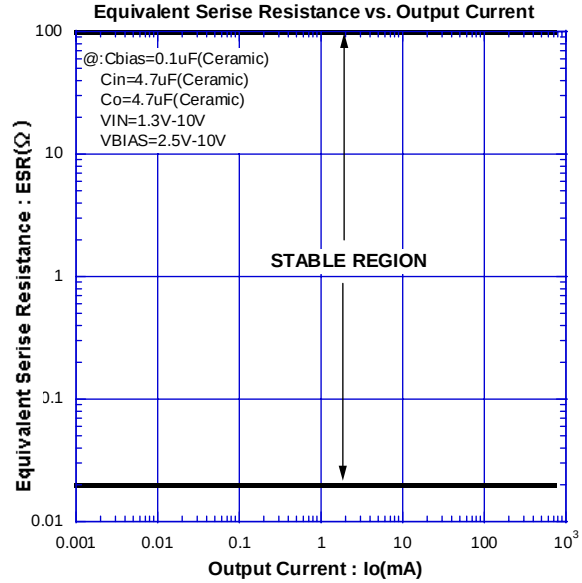
NJM2841_1.2V
Ripple Rejection(Vin-Vout) vs. Output Current



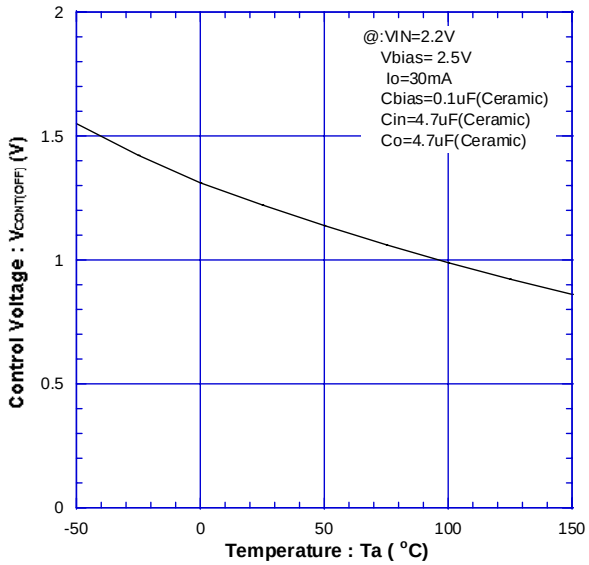
NJM2841_1.2V
Ripple Rejection(Vbias-Vout) vs. Output Current



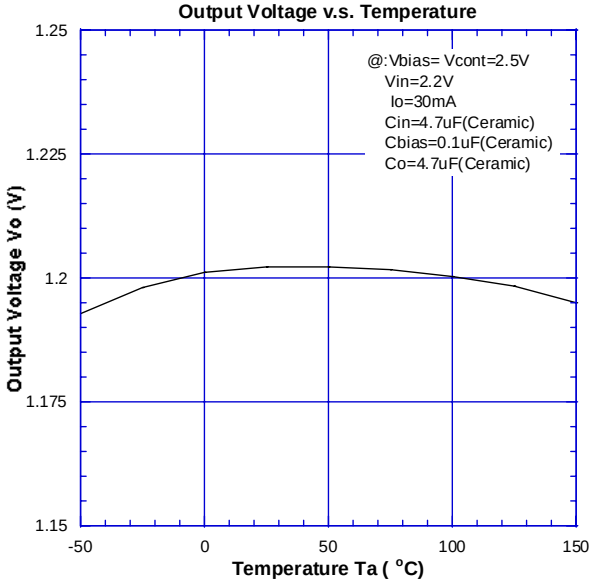
NJM2841_1.2V
Equivalent Serise Resistance vs. Output Current



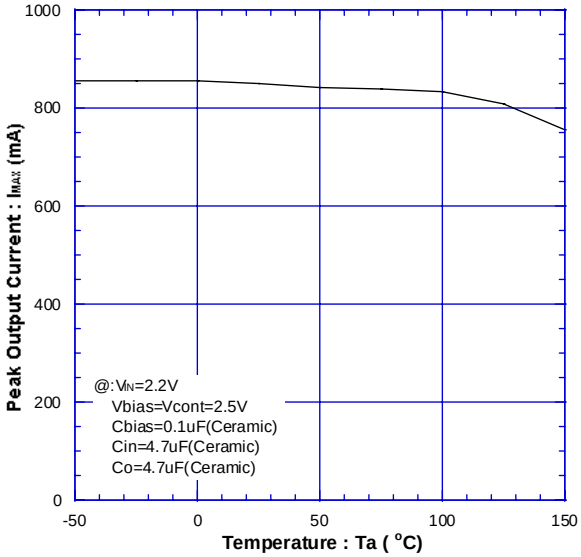
NJM2841_1.2V
Control Voltage v.s. Temperature



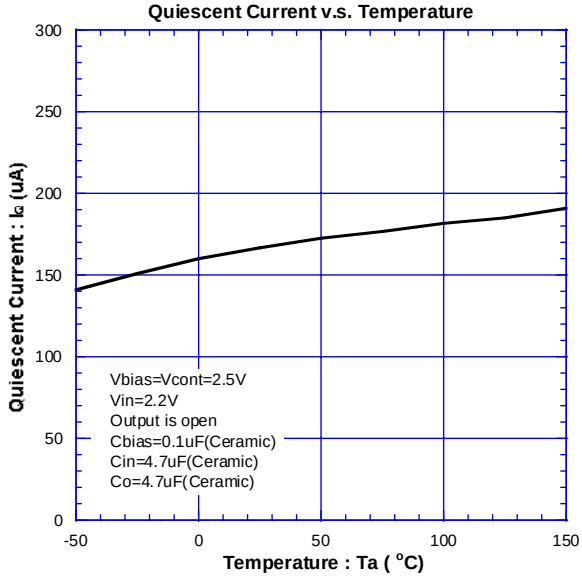
NJM2841_1.2V
Output Voltage v.s. Temperature



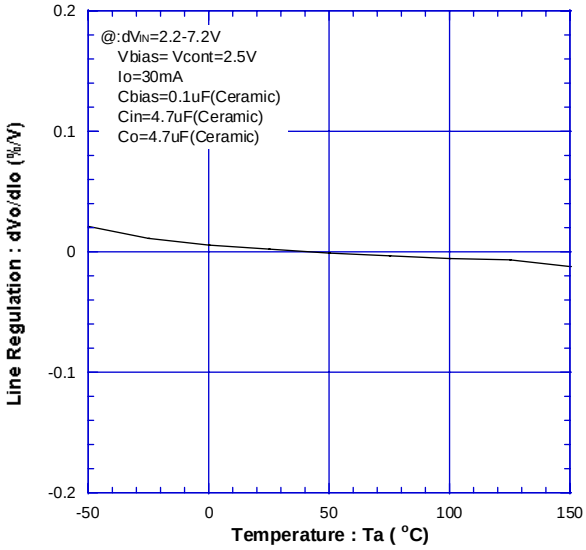
NJM2841_1.2V
Peak Output Current v.s. Temperature



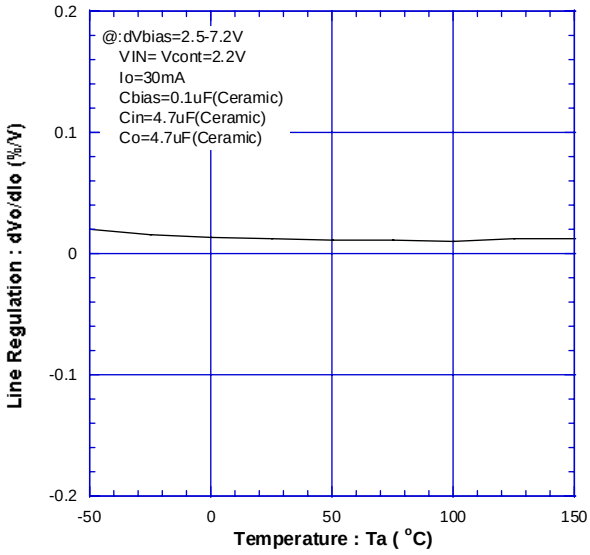
NJM2841_1.2V
Quiescent Current v.s. Temperature



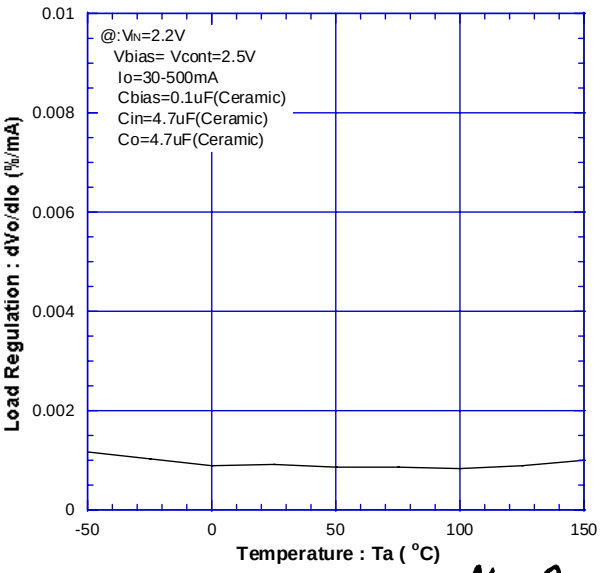
NJM2841_1.2V
Line Regulation(VIN) v.s. Temperature



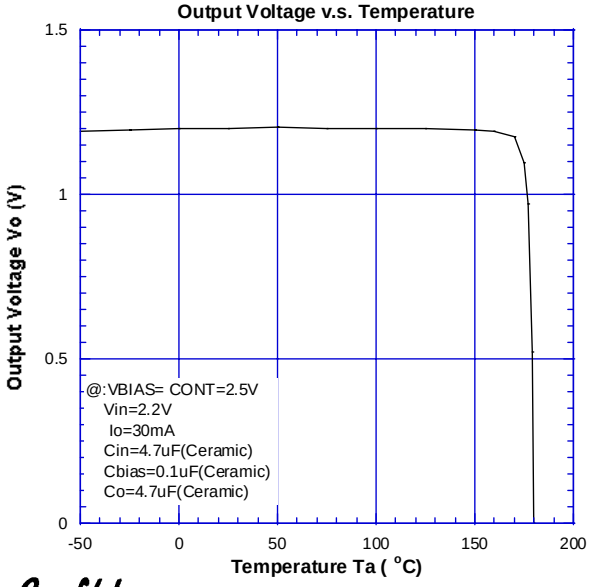
NJM2841_1.2V
Line Regulation(VBIAS) v.s. Temperature

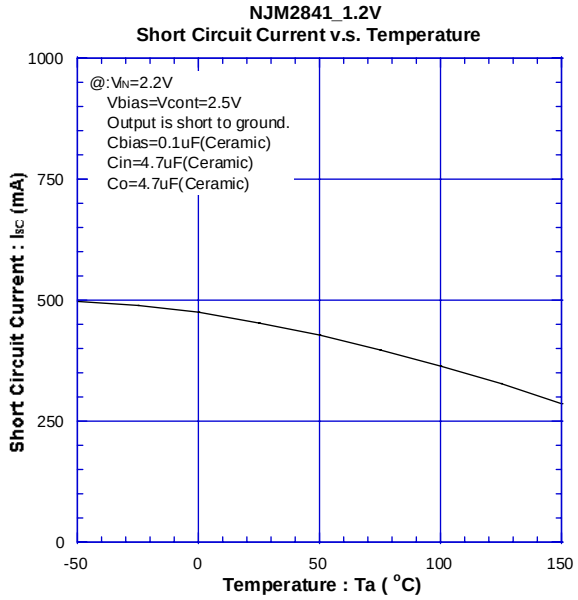


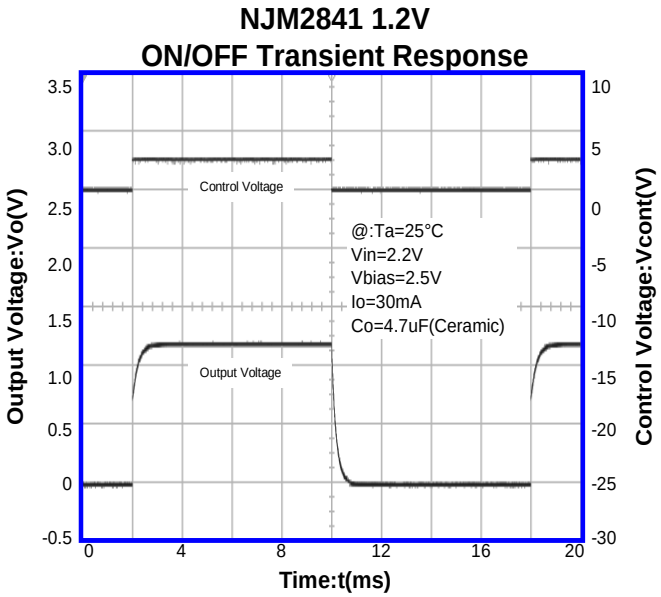
NJM2841_1.2V
Load Regulation v.s. Temperature

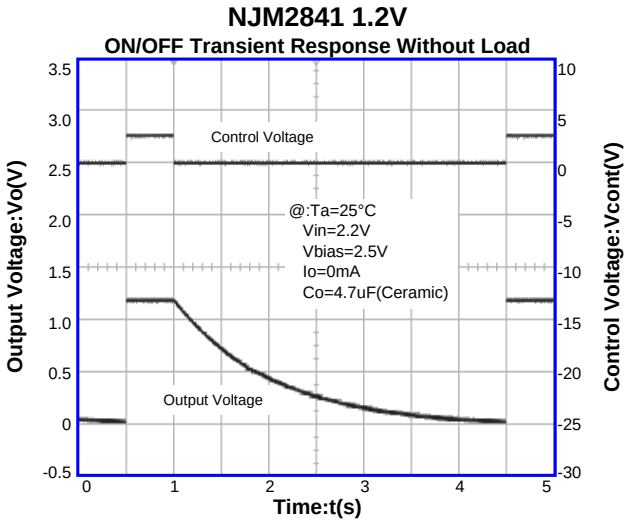


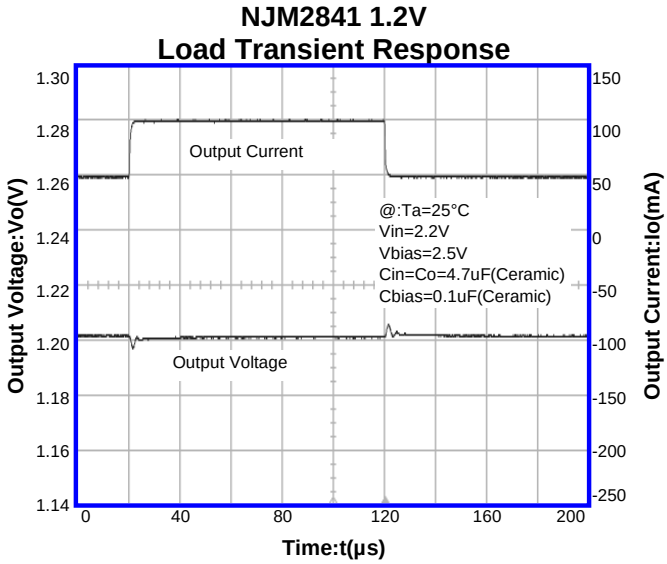
NJM2841_1.2V
Output Voltage v.s. Temperature

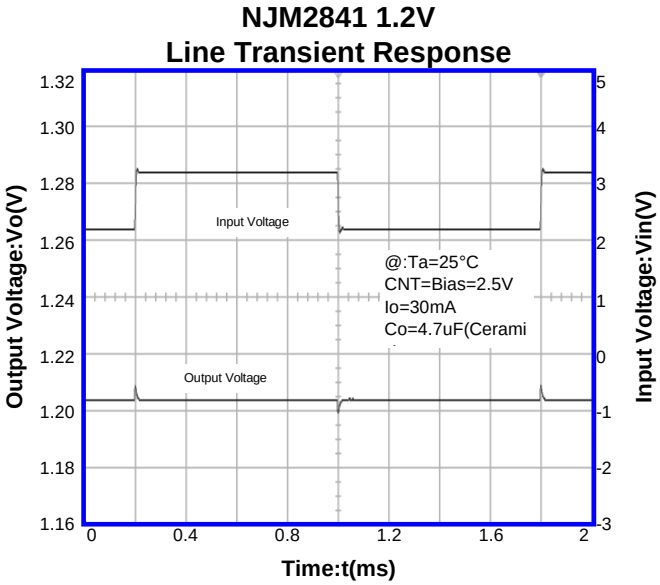


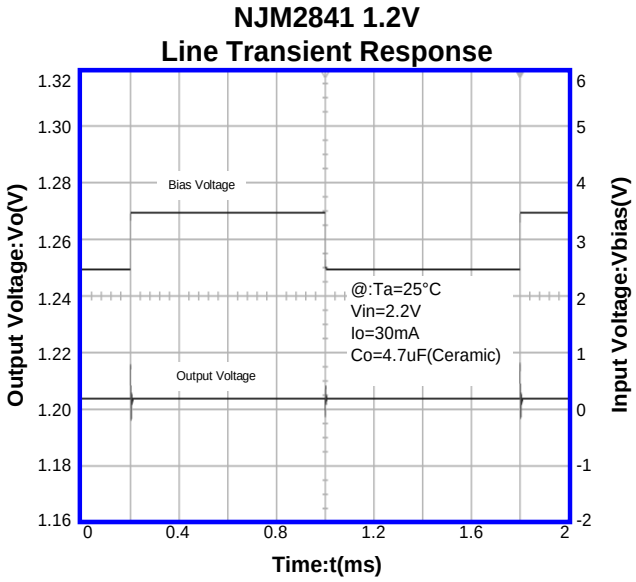

NJM2841_1.2V
Short Circuit Current v.s. Temperature
@:VIN=2.2V
Vbias=Vcont=2.5V
Output is short to ground.
Cbias=0.1uF(Ceramic)
Cin=4.7uF(Ceramic)
Co=4.7uF(Ceramic)
Short Circuit Current : Isc (mA)
Temperature : Ta (°C)


NJM2841 1.2V
ON/OFF Transient Response
Control Voltage
Output Voltage
@:Ta=25°C
Vin=2.2V
Vbias=2.5V
Io=30mA
Co=4.7uF(Ceramic)
Output Voltage:Vo(V)
Control Voltage:Vcont(V)
Time:t(ms)


NJM2841 1.2V
ON/OFF Transient Response Without Load
Control Voltage
Output Voltage
@:Ta=25°C
Vin=2.2V
Vbias=2.5V
Io=0mA
Co=4.7uF(Ceramic)
Output Voltage:Vo(V)
Control Voltage:Vcont(V)
Time:t(s)


NJM2841 1.2V
Load Transient Response
Output Current
Output Voltage
@:Ta=25°C
Vin=2.2V
Vbias=2.5V
Cin=Co=4.7uF(Ceramic)
Cbias=0.1uF(Ceramic)
Output Voltage:Vo(V)
Output Current:Io(mA)
Time:t(µs)


NJM2841 1.2V
Line Transient Response
Input Voltage
Output Voltage
@:Ta=25°C
CNT=Bias=2.5V
Io=30mA
Co=4.7uF(Cerami
Output Voltage:Vo(V)
Input Voltage:Vin(V)
Time:t(ms)


NJM2841 1.2V
Line Transient Response
Bias Voltage
Output Voltage
@:Ta=25°C
Vin=2.2V
Io=30mA
Co=4.7uF(Ceramic)
Output Voltage:Vo(V)
Input Voltage:Vbias(V)
Time:t(ms)

[CAUTION]
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