Low Input / Output 1.5 A Low Dropout Regulator

No.EA-585-230706

OVERVIEW

The RP120 is a very low dropout regulator which operates from input voltage as low as 0.768 V (@V_{SET} = 0.6 V, V_{BIAS} = 3.3 V, I_{OUT} = 1.5 A). The LDO uses an internal low on-resistance (67 mΩ @V_{SET} = 0.6 V, V_{BIAS} = 3.3 V, I_{OUT} = 1 A) NMOS transistor as the driver. The VBIAS pin provides the higher supply necessary for the LDO circuitry while the output current comes directly from the VIN input for high efficiency regulation.

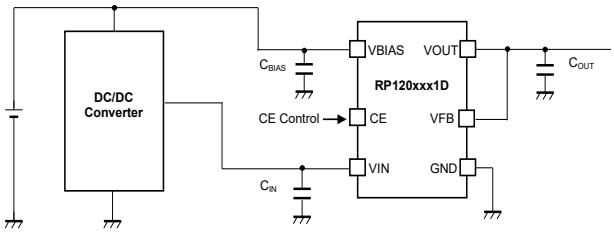
KEY BENEFITS

- High PSRR, high output current, and fast response characteristics.
- Suitable for sensitive sensors, high-quality audio, and RF devices.
- Very small WLCSP package (1.2 mm x 0.8 mm x 0.29 mm).

KEY SPECIFICATIONS

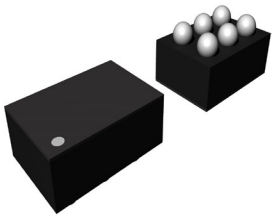
- Input Voltage Range :
  V_{IN} = V_{SET} + V_{DIFF} to V_{BIAS}
  (Ex. Min. 0.768 V @V_{SET} = 0.6 V, V_{BIAS} = 3.3 V, I_{OUT} = 1.5 A)
  V_{BIAS} = 2.4 V to 5.5 V
- Output Voltage Setting Range:
  Internal Fixed Type: 0.6 V to 2.0 V
  Adjustable Output Type: 0.6 V to 3.6 V
- Output Current: I_{OUTMAX} = 1.5 A
- Supply Current: Typ. 35 µA
- Output Noise: Typ. 50 µVrms (V_{SET} = 0.6 V)
- Power Supply Ripple Rejection:
  Typ. 95 dB (f = 1 kHz, Ripple in V_{IN})
  Typ. 60 dB (f = 100 kHz, Ripple in V_{IN})
- Dropout Voltage: Typ. 102 mV
  (I_{OUT} = 1.5 A, V_{SET} = 0.6 V, V_{BIAS} = 3.3 V)
- Inrush Current Limit: Typ. 600 mA
- Short Circuit Current Protection: Typ. 600 mA
- Thermal Shutdown: Typ. 165 °C
- Ceramic Capacitor: C_{OUT} 4.7 µF

TYPICAL APPLICATION



RP120 (Internal Fixed Type)
Typical Application Circuit

PACKAGE (unit: mm)



WLCSP-6-P11
1.2 x 0.8 x 0.29

APPLICATIONS

- Portable communication devices, battery-powered devices, camera, video, audio.
- Communication devices such as RF modules, clock generation devices such as VCOs and PLLs.
- Constant voltage source for analog circuits of FPGA and SoC.

SELECTION GUIDE

SELECTION GUIDE

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP120Zxx1Dy-E2-F	WLCSP-6-P11	5,000 pcs	YES	YES

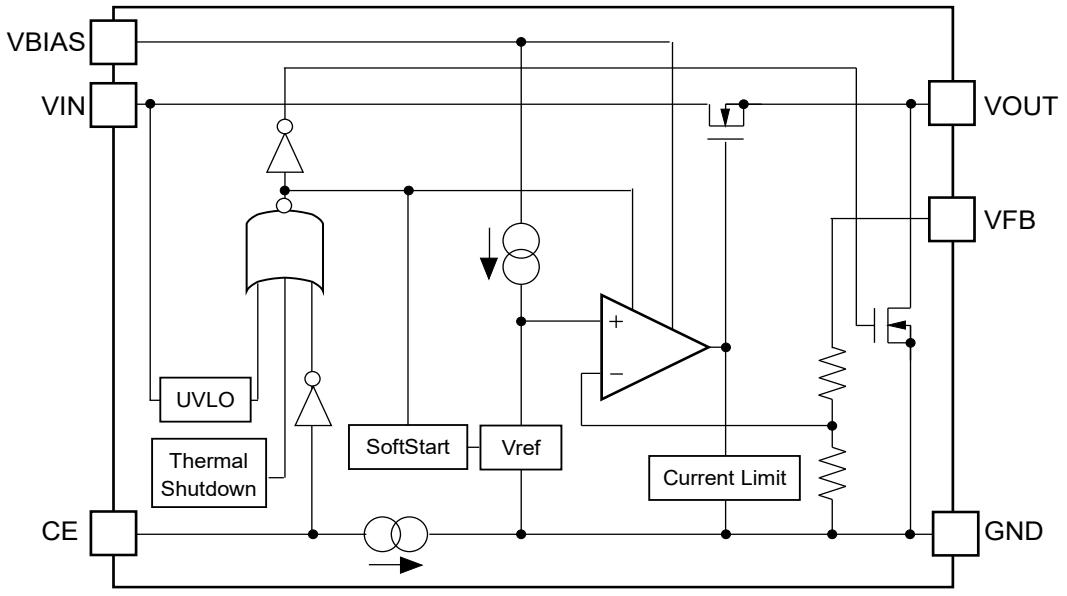
xx : Specify the output voltage from 0.6 V (06) to 2.0 V (20) in 0.1 V increments.

Output voltage external setting type is fixed to (00).

y : Used when specifying in units of 10mv such as 0.75V

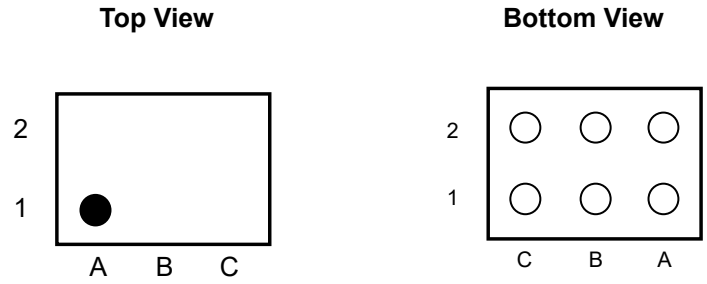
Example: RP120Z071D5

BLOCK DIAGRAM



RP120xxx1D Block Diagram

PIN DESCRIPTIONS



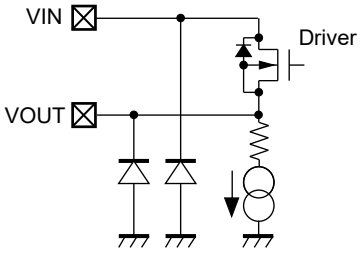
WLCSP-6-P11 Pin Configuration

RP120Z(WLCSP-6-P11) Pin Description

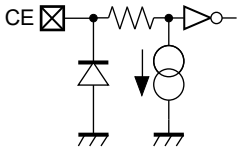
Symbol	Pin No.	I/O	Description
VOUT	A1	O	Output voltage pin. The VOUT pin supplies power to the load. A minimum output capacitance shown in “Phase Compensation” section is required to ensure stability. See the “Phase Compensation“ section for more information on output capacitance.
VFB	B1	I	Output Feedback Pin For the type that fixes the output voltage internally, connect this pin to the VOUT pin. For the type that sets the output voltage externally, connect this pin to a resistor divider from VOUT pin to GND.
GND	C1	-	Ground pin of the internal circuit.
VIN	A2	I	Power supply pin of the NMOS driver. Input Supply Voltage. Output load current is supplied directly from VIN. The VIN pin should be locally bypassed to GND.
CE	B2	I	Chip Enable Pin. Logic "High" input : LDO is active, Logic “Low” input: the LDO into shutdown. This pin is pulled down internally.
VBIAS	C2	I	Analog Power Supply Pin Must be connected to an external supply voltage. The VBIAS pin should be locally bypassed to GND.

Please refer to “*TYPICAL APPLICATION CIRCUITN*“ or “*OPERATION*“ for details.

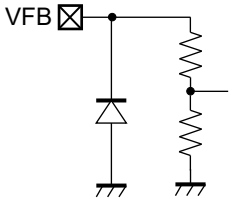
Internal Equivalent Circuit Diagram of Pin



Internal equivalent circuit diagram of VIN and VOUT pin



Internal equivalent circuit diagram of CE pin



Internal equivalent circuit diagram of VFB pin

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Unit
V_{BIAS}	Analog Power Supply Voltage	−0.3 to 6.5	V
V_{IN}	NMOS driver power input voltage	−0.3 to V_{BIAS} + 0.3 ≤ 6.5	V
V_{CE}	Input Voltage (CE pin)	−0.3 to 6.5	V
V_{OUT}	Output Voltage	−0.3 to V_{IN} + 0.3 ≤ 6.5	V
V_{FB}	VFB pin Voltage	−0.3 to V_{OUT} + 0.3 ≤ 6.5	V
Tj	Junction Temperature Range[*1]	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

[*1] Calculate the power loss of the IC from the usage conditions, and calculate the junction temperature using it and the thermal resistance. Please refer to "Thermal characteristics" for thermal resistance and thermal parameters under our measurement board conditions.

ELECTROSTATIC DISCHARGE(ESD) RATINGS

Symbol	Conditions	Ratings	Unit
V_{HBM}	HBM C=100pF、R=1.5kΩ	±2000	V
V_{CDM}	CDM	±1000	

Electrostatic Discharge Ratings
The electrostatic discharge test is done based on JESD47. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Ratings	Unit
V_{BIAS}	Input Voltage	2.4 to 5.5 (V_{SET} < 0.9) V_{SET} + 1.5V to 5.5 (V_{SET} ≥ 0.9)	V
V_{IN}		V_{SET} + V_{DIF} to V_{BIAS} (Max. 5.5)	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = V_{CE} = 3.6 V, V_{IN} = V_{SET} + 0.5 V, I_{OUT} = 1 mA, C_{BIAS} = C_{IN} = 1.0 µF, C_{OUT} = 4.7 µF unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP120xxx1D (Ta = 25°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	V_{SET} > 1.2V	x 0.993		x 1.007	V
			V_{SET} ≤ 1.2V	- 0.009		+ 0.009	
		−40°C ≤ Ta ≤ 85°C	V_{SET} > 1.2V	[x 0.985]		[x 1.015]	
			V_{SET} ≤ 1.2V	[- 0.018]		[+ 0.018]	
I_{BIAS}	VBIAS Pin Supply Current	I_{OUT} = 0mA			35	[50]	µA
I_{IN}	VIN Pin Supply Current	I_{OUT} = 0mA			1.5	[2.8]	µA
I_{STBB}	VBIAS pin Standby Current	V_{BIAS} = 5.5V, V_{CE} = 0V			0	0.2	µA
I_{STBI}	VIN pin Standby Current	V_{BIAS} = 5.5V, V_{CE}= 0V			0	0.2	µA
I_{CEH}	CE Pin Input Current ”H”	V_{BIAS} = V_{CE} = 5.5 V		[0.05]	0.25	[0.6]	µA
ΔV_{OUT} /ΔI_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 1.5A		[-1.7]	0.1	[1.7]	%
ΔV_{OUT} /ΔV_{IN}	V_{IN} Line Regulation	V_{SET} + 0.1V ≤ V_{IN} ≤ 3.6V		[-0.25]		[0.25]	%/V
ΔV_{OUT} /ΔV_{BIAS}	V_{BIAS} Line Regulation	V_{SET} + 1.5V ≤ V_{BIAS} ≤ 5.5V		[-0.25]		[0.25]	%/V
R_{DISTR}	Auto-discharge NMOS On-resistance	V_{BIAS} = 3.6V, V_{CE} = 0V			50		Ω
V_{CEH}	CE Pin Input Voltage ”H”			[0.9]		[5.5]	V
V_{CEL}	CE Pin Input Voltage ”L”			[0]		[0.4]	V
V_{DIF}	Dropout Voltage	V_{BIAS} = 3.3V (V_{SET} ≤ 1.8V) V_{BIAS} = V_{SET} + 1.5V (1.8V < V_{SET})		Refer to the “*PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS*”			V
t_{SS}	Soft Start Time (1)			[100]	185	[320]	µs
I_{SC}	Short-circuit Current	V_{OUT}= 0V			0.6		A
$I_{LIMRISE}$	Limit Current at Start-up	V_{OUT}= 0V			0.6		A
V_{UVLOF}	UVLO Detection Voltage	V_{BIAS} = V_{CE} = 3.6V, V_{IN} Falling		[0.26]	0.3	[0.34]	V
V_{UVLOR}	UVLO Release Voltage	V_{BIAS} = V_{CE} = 3.6V, V_{IN} Rising		[0.36]	0.4	[0.44]	V

All products are tested under the condition of Tj ≈ Ta = 25°C.

(1) It is specified based on the measurement result of the time when the VOUT pin voltage rises from 10% to 90%, and converted it to 100% time by calculation.

V_{BIAS} = V_{CE} = 3.6V, V_{IN} = 1.1V, I_{OUT} = 1mA, C_{BIAS} = C_{IN} = 1.0µF, C_{OUT} = 4.7µF unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP120x001D (Ta = 25°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{FB}	Feedback pin Output Voltage	Ta = 25°C		0.591	0.6	0.609	V
		−40°C ≤ Ta ≤ 85°C		[0.582]	0.6	[0.618]	
I_{BIAS}	VBIAS Pin Supply Current	I_{OUT} = 0mA			35	[50]	µA
I_{IN}	VIN Pin Supply Current	I_{OUT} = 0mA			1.5	[2.8]	µA
I_{STBB}	VBIAS pin Standby Current	V_{BIAS} = 5.5V , V_{CE} = 0V			0	0.2	µA
I_{STBI}	VIN pin Standby Current	V_{BIAS} = 5.5V , V_{CE} = 0V			0	0.2	µA
I_{CEH}	CE Pin Input Current ”H”	V_{BIAS} = V_{CE} = 5.5V		[0.05]	0.25	[0.6]	µA
Δ V_{OUT} /Δ I_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 1.5A		[-1.7]	0.1	[1.7]	%
Δ V_{OUT} /Δ V_{IN}	V_{IN} Line Regulation	V_{SET} + 0.1V ≤ V_{IN} ≤ 3.6V		[-0.25]		[0.25]	%/V
Δ V_{OUT} /Δ V_{BIAS}	V_{BIAS} Line Regulation	V_{SET} + 1.5V ≤ V_{BIAS} ≤ 5.5V		[-0.25]		[0.25]	%/V
R_{DISTR}	Auto-discharge NMOS On-resistance	V_{CE} = 0V			50		Ω
V_{CEH}	CE Pin Input Voltage ”H”			[0.9]		[5.5]	V
V_{CEL}	CE Pin Input Voltage ”L”			[0]		[0.4]	V
V_{DIF}	Dropout Voltage	V_{SET} = 0.6V, V_{BIAS} = 3.3V	I_{OUT} = 1.0A		0.067	[0.115]	V
			I_{OUT} = 1.5A		0.102	[0.168]	
t_{SS}	Soft Start Time (1)			[100]	185	[320]	µs
I_{SC}	Short-circuit Current	V_{OUT}= 0V			0.6		A
$I_{LIMRISE}$	Limit Current at Start-up	V_{OUT}= 0V			0.6		A
V_{UVLOF}	UVLO Detection Voltage	V_{BIAS} = V_{CE} = 3.6V, V_{IN} Falling		[0.26]	0.3	[0.34]	V
V_{UVLOR}	UVLO Release Voltage	V_{BIAS} = V_{CE} = 3.6V, V_{IN} Rising		[0.36]	0.4	[0.44]	V

All test items listed under Electrical Characteristics are done with short-circuiting VOUT pin and VFB pin, and under the pulse load condition (Tj ≈ Ta = 25°C).

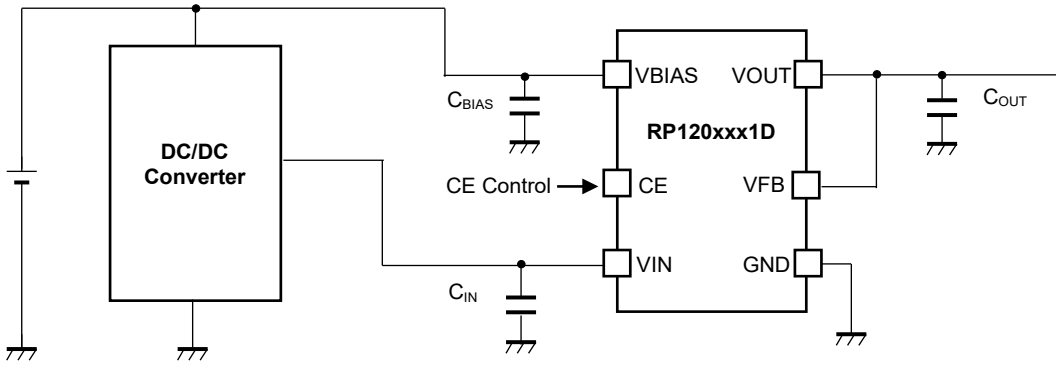
(1) It is specified based on the measurement result of the time when the VOUT pin voltage rises from 10% to 90%, and converted it to 100% time by calculation.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C

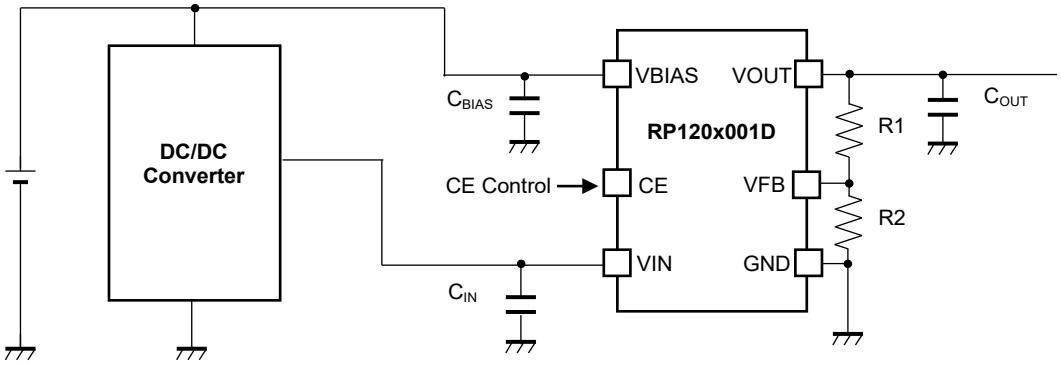
RP120Zxx1D Product-specific Electrical Characteristics

Product Name	V_{OUT} [V]					V_{DIF} [mV]			
	Typ.	Ta = 25°C		−40°C ≤ Ta ≤ 85°C		I_{OUT}=1.0A		I_{OUT}=1.5A	
		Min.	Max.	Min.	Max.	Typ.	Max.	Typ.	Max.
RP120Z061D	0.6	0.591	0.609	[0.582]	[0.618]	67	[115]	102	[168]
RP120Z071D	0.7	0.691	0.709	[0.682]	[0.718]	68	[117]	104	[171]
RP120Z071D5	0.75	0.741	0.759	[0.732]	[0.768]	69	[121]	107	[175]
RP120Z081D	0.8	0.791	0.809	[0.782]	[0.818]	69	[121]	107	[175]
RP120Z081D5	0.85	0.841	0.859	[0.832]	[0.868]	72	[127]	110	[178]
RP120Z091D	0.9	0.891	0.909	[0.882]	[0.918]	72	[127]	110	[178]
RP120Z101D	1.0	0.991	1.009	[0.982]	[1.018]	73	[131]	113	[185]
RP120Z111D	1.1	1.091	1.109	[1.082]	[1.118]	76	[138]	117	[194]
RP120Z121D	1.2	1.191	1.209	[1.182]	[1.218]	80	[146]	122	[202]
RP120Z131D	1.3	1.291	1.309	[1.281]	[1.319]	84	[153]	131	[218]
RP120Z141D	1.4	1.391	1.409	[1.379]	[1.421]	89	[163]	140	[239]
RP120Z151D	1.5	1.490	1.510	[1.478]	[1.522]	97	[176]	155	[268]
RP120Z161D	1.6	1.589	1.611	[1.576]	[1.624]	104	[187]	170	[302]
RP120Z171D	1.7	1.689	1.711	[1.675]	[1.725]	113	[204]	183	[332]
RP120Z181D	1.8	1.788	1.812	[1.773]	[1.827]	123	[225]	193	[368]
RP120Z191D	1.9	1.887	1.913	[1.872]	[1.928]	123	[225]	193	[368]
RP120Z201D	2.0	1.986	2.014	[1.970]	[2.030]	123	[225]	193	[368]

TYPICAL APPLICATION CIRCUIT



RP120xxx1D (Internal Fixed Type) Typical Application Circuit



RP120x001D (Adjustable Output Type) Typical Application Circuit

External Components

VIN, VBIAS pins should be locally bypassed to GND to make their impedance low. If their impedance is high, making unexpected noise or unstable operation may result. A capacitor (C_{BIAS}) between VBIAS pin and GND and another capacitor (C_{IN}) between VIN pin and GND should be 1uF or more each.
It is desirable to choose X7R and X5R ceramic capacitors (voltage rating should be more than twice as much as input), which have good temperature characteristics of ESR, ESL, and capacitance.

Phase Compensation

The RP120 is designed to be stable with an output capacitor for phase compensation with whole range of the output load current. An output capacitor of minimum 4.7µF ($V_{SET} \leq 2.0V$), or minimum 10µF ($V_{SET} > 2.0V$) or greater value of C_{OUT} is recommended to ensure stability. Note that bypass capacitors used to decouple individual components powered by the more stable characteristics and are more suitable for use as the output capacitor.
It is desirable to choose X7R and X5R ceramic capacitor for output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Select so that the following effective capacitance can be secured.

Set Output Voltage (V_{SET})	Effective Capacitance
$0.6V \leq V_{SET} < 1.2V$	Min. 2.7µF
$1.2V \leq V_{SET} \leq 2.0V$	Min. 2.4µF
$2.0V < V_{SET} \leq 3.6V$	Min. 6.0µF

External Resistor for Setting Output Voltage

The output voltage is set by the ratio of two external resistors as shown above.

Output Voltage Setting Range : 0.6V to 3.6V
V_{FB} = 0.6V (Typ.)

The set output voltage (V_{SET}) is as follows.

$$V_{SET} = V_{FB} \times ((R1 + R2) / R2)$$

More precisely, the current in R1 is the current in R2 plus the internal current through the resistance (R_{IC}) between VFB pin and GND. The value of the R_{IC} is Typ.3.6MΩ, therefore, $V_{FB} \times R1/R_{IC}$ makes an error.
If R1 << R_{IC}, the error can be reduced.
Use a resistance value, R2 of 20kΩ or less for V_{SET} <1.3V and 10kΩ or less for $V_{SET} \geq 1.3V$.

OPERATION

Chip Enable Function

Input "High" to CE pin, the RP120 is active. Input "Low" to CE pin, the RP120 is into shutdown.
Regardless of the state of V_{IN} and V_{BIAS} voltage, a voltage can be forced to CE pin.
The CE pin is pulled down inside the IC with a constant current of Typ. 0.25μA, therefore, when the CE pin is left floating, the RP120 goes into shutdown state. CE pin must be tied to a valid logic level (such as V_{BIAS}) if not used.

UVLO (Undervoltage Lock Out) Function

An undervoltage lockout comparator (UVLO) is activated while CE pin is “High”.
The UVLO comparator senses VIN pin voltage to ensure that the V_{IN} supply for the LDO is greater than UVLO released voltage (V_{UVLOR}, Typ. 0.4V) before enabling the LDO. If V_{IN} is below the UVLO threshold (V_{UVLOF}, Typ. 0.3V), the UVLO shuts down the LDO, and V_{OUT} is pulled to GND through the external divider and internal auto discharge transistor for Off state. After UVLO is released, the LDO starts up with soft-start.

Thermal Shutdown Function

The RP120 has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. At higher temperatures, or in cases where internal power dissipation cause excessive self-heating on-chip, the thermal shutdown circuitry will shut down LDO when the junction temperature exceeds Typ. 165°C, the RP120 will reenable once the junction temperature drops back to thermal shutdown released threshold (Typ. 125°C), the IC will restart with the soft start operation.

Auto Discharge

When turning off, the V_{OUT} voltage quickly pulled down to near 0V by discharging electric charge stored in output capacitor through the MOSFET connected between the VOUT pin and GND.
The auto discharge function is enabled when CE pin = ”Low”, thermal shutdown detection, or UVLO detection. This function is effective when V_{BIAS} is the minimum operating voltage or higher. The on-resistance of the MOSFET is Typ. 50Ω.

Soft Start / Inrush Current Limit

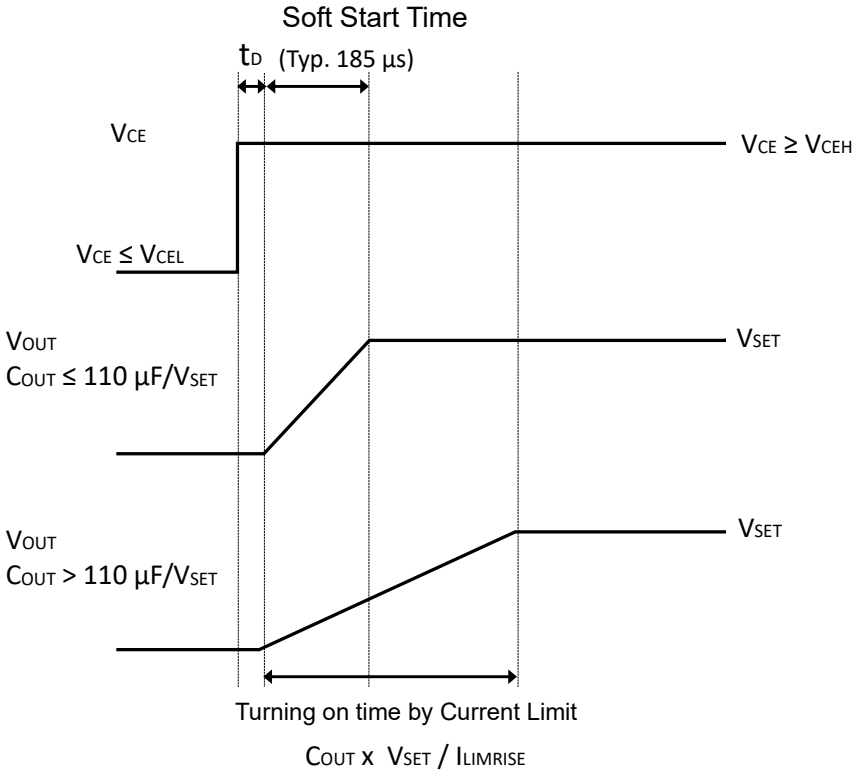
The RP120 includes a soft-start feature to prevent excessive inrush current flow at V_{IN} during start-up. When the LDO is enabled, the soft-start circuitry gradually increases the internal reference voltage of LDO over a period of approximately 185µs.
In addition, the RP120 limits the inrush current up to Typ. 600mA during startup.

The inrush current depends on the capacitance value of C_{OUT}. Connecting a large load and the inrush current value may exceed the threshold of Typ. 600mA during startup, the slew rate is further limited and extended start-up time. If an effective capacitance value of the C_{OUT} is larger than about 110µF / V_{SET} is used, the output voltage ramp up time is determined by the inrush current limit value and C_{OUT} value.

The output turning on time (t_{ON}) can be calculated from the following equation:

$t_{ON} = t_D + C_{OUT} \times V_{SET} / I_{LIMRISE}$
t_D : Delay Time at Start-up 60µs
V_{SET} : Set Output Voltage
$I_{LIMRISE}$: Current Limit at Start-up Typ. 600mA

If the load current (I_{LOAD}) exists other than the charge current to C_{OUT} during start-up, the start-up time is extended. The load current over $I_{LIMRISE}$ may interfere charging of C_{OUT} and the output does not rise up.



Thermal Characteristics 1

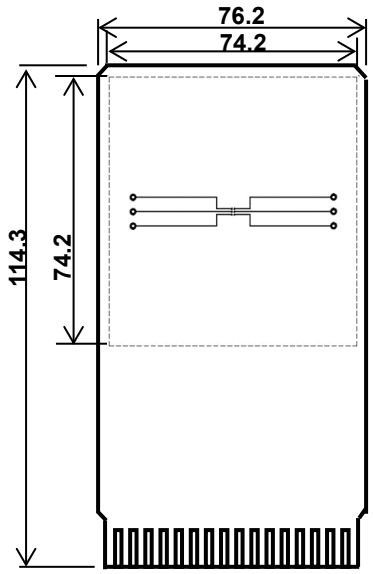
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51

Item	Measurement Result
Thermal Resistance (θja)	θja = 170°C/W
Thermal Parameters (ψjt)	ψjt =41.7°C/W

θja：Junction-to-Ambient Thermal Resistance.
ψjt：Thermal parameters between junction temperature and package mark surface center temperature.

Measurement Condition

Measurement Status	Board Mounting State (Wind speed = 0m/s)
Board Material	Glass Epoxy Resin (4-layer board)
Board Size	76.2mm x 114.3mm x 1.6mm
Wiring Rate	Outer Layer (1-Layer): 10% or less Inner Layers (2 and 3-Layers): 74.2 x 74.2mm 100% Outer Layer (4-Layer): 10% or less



Measurement Board Pattern

Thermal Characteristics 2

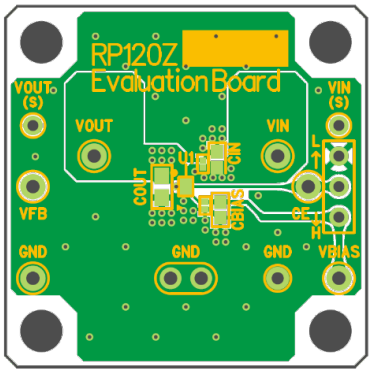
Thermal characteristics depend on the mounting conditions.
The following thermal characteristics are measurement data using our evaluation board.

Item	Measurement Result
Thermal Resistance (θja)	θja = 80°C/W
Thermal Parameters (ψjt)	ψjt =17.1°C/W

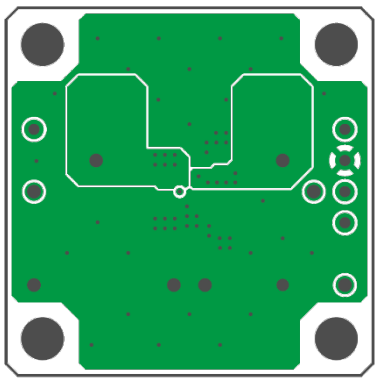
θja : Junction-to-Ambient Thermal Resistance.
ψjt : Thermal parameters between junction temperature and package mark surface center temperature.

Measurement Condition

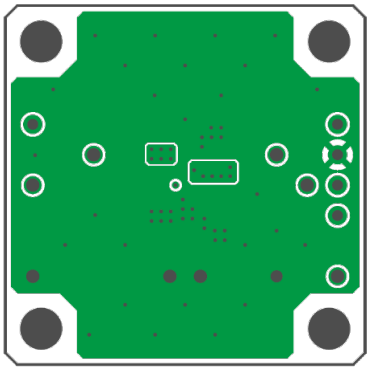
Measurement Status	Board Mounting State（Wind Speed 0m/s）
Board Material	Glass Epoxy Resin (4-Layer Board)
Board Size	30mm × 30mm × 1.0mm
Wiring Rate	Outer Layer (1-Layer): 85% Inner Layers (2 and 3-Layers): 85% Outer Layer (4-Layer): 85%



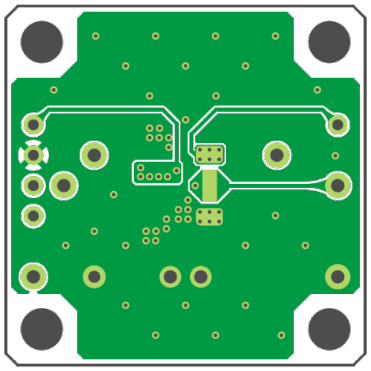
PCB Layout − 1st Layer



PCB Layout − 2nd Layer



PCB Layout − 3rd Layer



PCB Layout − 4th Layer

Calculation Method of Junction Temperature Using Thermal Characteristics

The junction temperature (Tj) inside the IC can be calculated from the thermal characteristics using the following formula.

$$Tj = Ta + \theta ja \times P$$
$$Tj = Tc(top) + \psi jt \times P$$

Ta: Ambient temperature
Tc(top) : Package mark surface center temperature
P : $(V_{IN} - V_{OUT}) \times I_{OUT}$ (Power consumption under customer's usage conditions)

TECHNICAL NOTES

Constraints of the voltage value and the sequence of V_{BIAS} and V_{IN}

V_{IN} voltage must be applied below V_{BIAS} voltage since a forward current flows through the parasitic diode in the IC. $V_{BIAS} \geq V_{IN}$ should be true even when they turn on and off. At startup, supply V_{IN} and V_{BIAS} at the same time, or supply V_{IN} after V_{BIAS}. When turning off the supply voltage of V_{IN} and V_{BIAS}, turn them off at the same time, or turn off V_{IN} before V_{BIAS}.

Thermal Shutdown

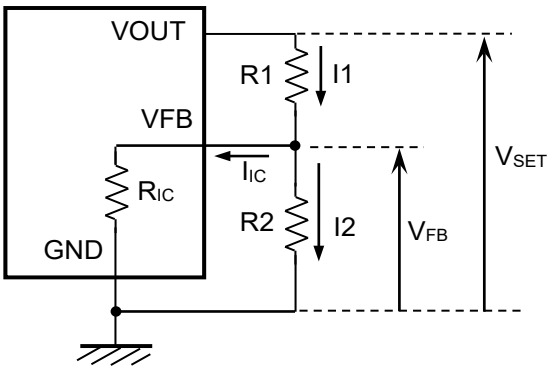
The thermal shutdown function prevents the IC from fuming and firing but does not ensure the IC's reliability or keep the IC below the absolute maximum ratings. The thermal shutdown function does not operate against the heat generated by abnormal IC operation such as latch-up and overvoltage.
The thermal shutdown function operates in a state over the absolute maximum ratings, and should not be used for a system design.

APPLICATION INFORMATION

Adjustable Output Voltage

The output voltage is set by the ratio of two external resistors (R1, R2).

The device servos the output to maintain the VFB pin voltage at 0.6V(referenced to ground). The output voltage (V_{SET}) can be calculated using the formula below.



$I1 = I_{IC} + I2$ ..... (1)

$I2 = V_{FB} / R2$ ..... (2)

(1)、(2)

$I1 = I_{IC} + V_{FB} / R2$ ..... (3)

$V_{SET} = V_{FB} + R1 \times I1$ ..... (4)

I1 can be substituted by formula (3)

$V_{SET} = V_{FB} + R1 \times (I_{IC} + V_{FB} / R2)$

$= V_{FB} \times (1 + R1 / R2) + R1 \times I_{IC}$ ..... (5)

$R1 \times I_{IC}$ in the above formula (5) is the error.

$I_{IC} = V_{FB} / R_{IC}$ ..... (6)

Thus,

$R1 \times I_{IC} = R1 \times V_{FB} / R_{IC}$

$= V_{FB} \times R1 / R_{IC}$ ..... (7)

If $R1 << R_{IC}$, the error can be minimized.

If the error is ignored, the output voltage is calculated by the next formula.

$V_{SET} = V_{FB} \times ((R1 + R2) / R2)$ ..... (8)

R_{IC} of RP120Z001D is Typ.3.6MΩ (Ta=25°C, guaranteed by design value).
The accuracy of the output voltage is determined by the V_{FB} accuracy and resistance accuracy.
The current calculated by V_{SET} / (R1 + R2) flows between the VOUT pin and GND.

V_{FB} of RP120Z001D is typically 0.6V.

Recommended output voltage setting range: 0.6V ≤ V_{SET} ≤ 3.6V

V_{FB} accuracy: 0.6V ± 18mV (guaranteed by design in all temperature range).

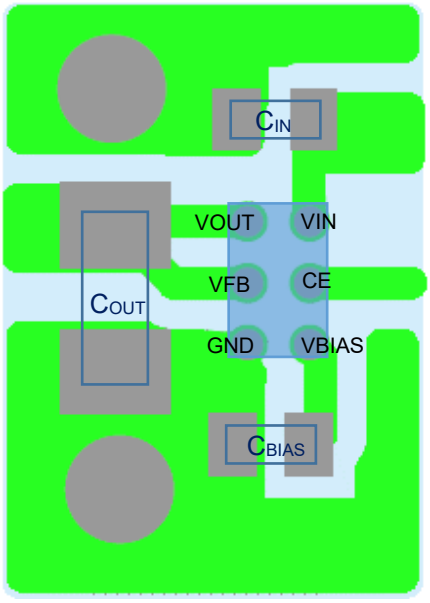
Use a resistance value, R2 of 20kΩ or less for V_{SET} <1.3V and 10kΩ or less for V_{SET} ≥ 1.3V.

Reference Resistance Value Table

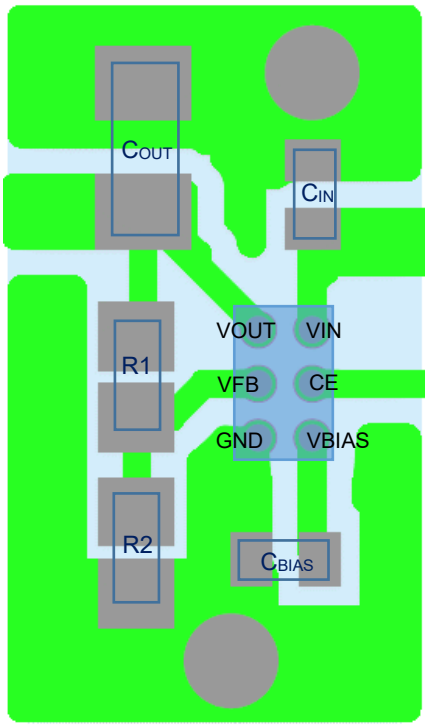
Set Output Voltage [V]	R1 [kΩ]	R2 [kΩ]
0.6	Short	Open
0.7	3.3	20
0.8	6.6	20
0.9	9.9	20
1.05	14.9	20
1.1	16.5	20
1.2	19.9	20
1.3	11.6	10
1.5	14.9	10
1.8	19.9	10
2.5	31.6	10
2.8	36.5	10
3.0	39.9	10
3.3	44.8	10
3.6	49.8	10

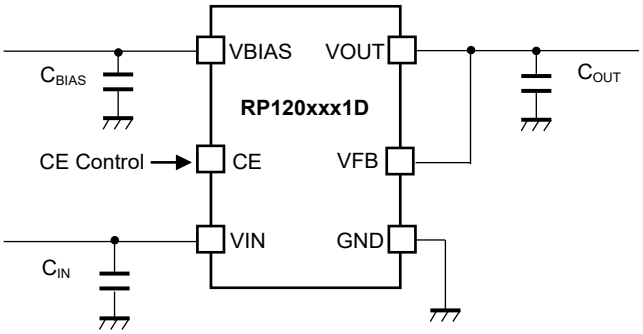
PCB Layout

Internal Fixed Type

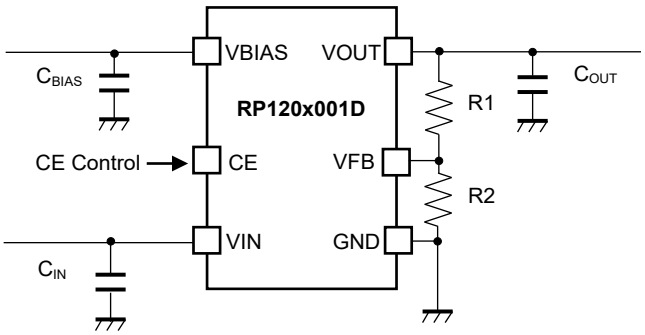


Adjustable Output Type





RP120xxx1D (Internal Fixed Type) Circuit



RP120x001D (Adjustable Output Type) Circuit

TYPICAL CHARACTERISTIC

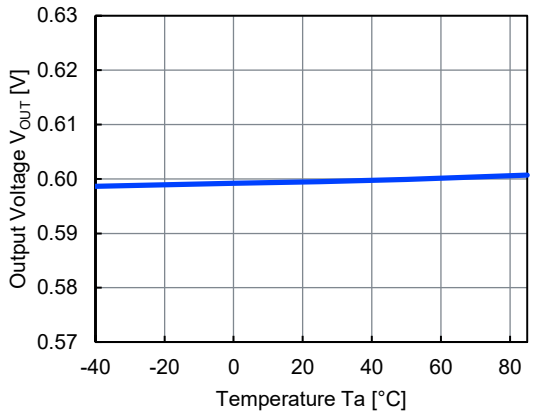
The waveform under the condition V_{BIAS} <V_{IN} describes the characteristics of V_{IN} = V_{BIAS}.

Typical Characteristics are intended to be used as reference data, they are not guaranteed.

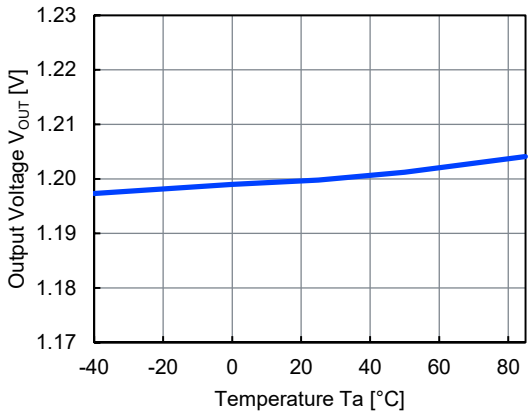
1) Output Voltage vs. Temperature

V_{BIAS} = 3.6 V , CE = V_{BIAS} , I_{OUT} = 1 mA

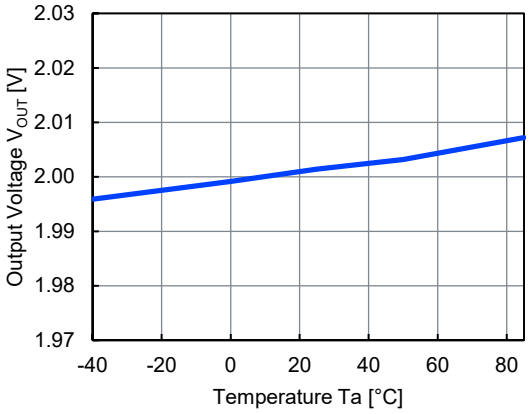
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



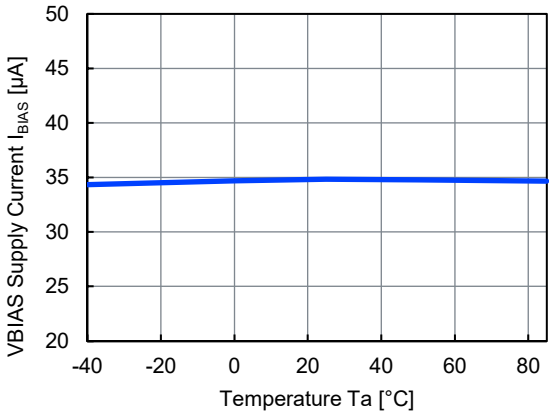
RP120Z201D , V_{IN} = 2.5 V



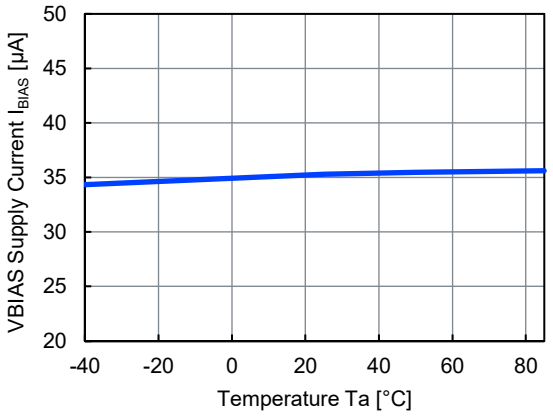
2) VBIAS Supply Current vs. Temperature

V_{BIAS} = 3.6 V , CE = V_{BIAS}

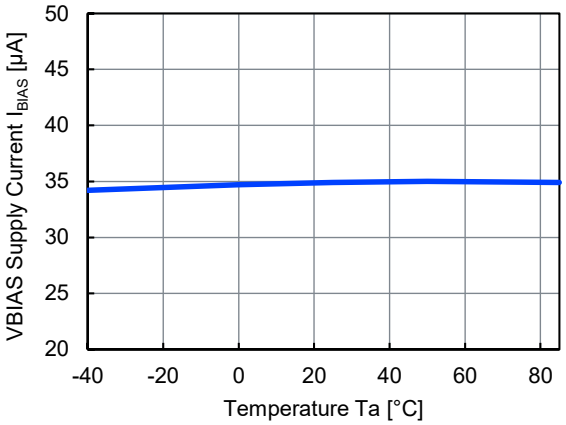
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



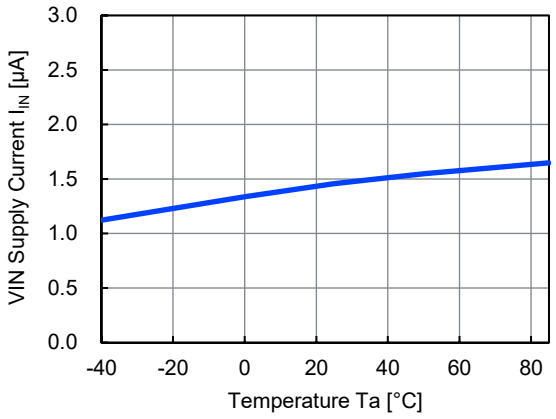
RP120Z201D , V_{IN} = 2.5 V



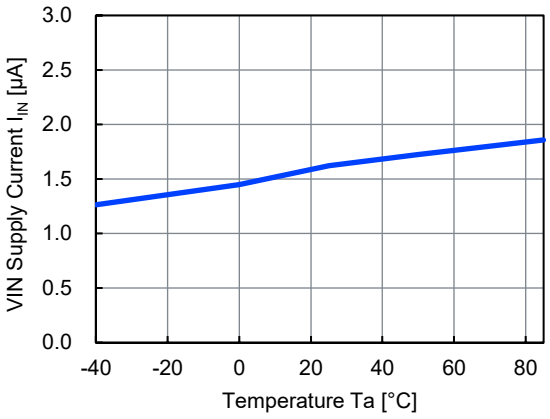
3) VIN pin Supply Current vs. Temperature

V_{BIAS} = 3.6 V , CE = V_{BIAS}

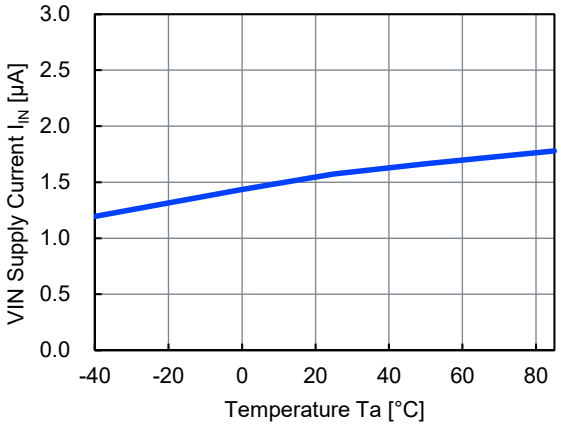
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



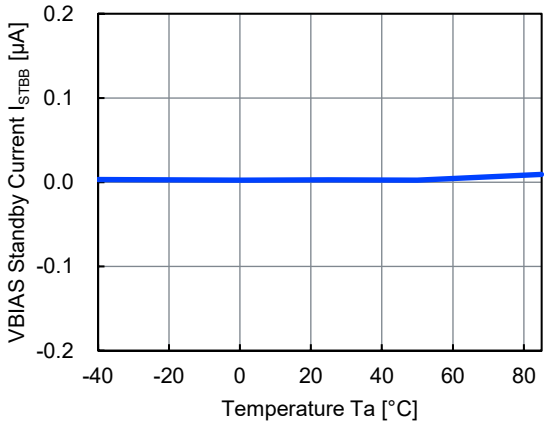
RP120Z201D , V_{IN} = 2.5 V



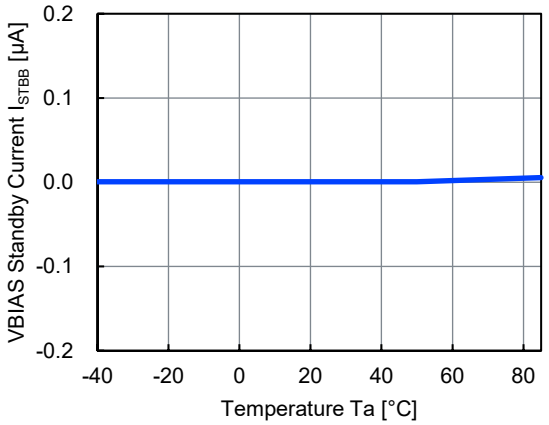
4) VBIAS pin Standby Current vs. Temperature

V_{BIAS} = 5.5 V, CE = 0 V

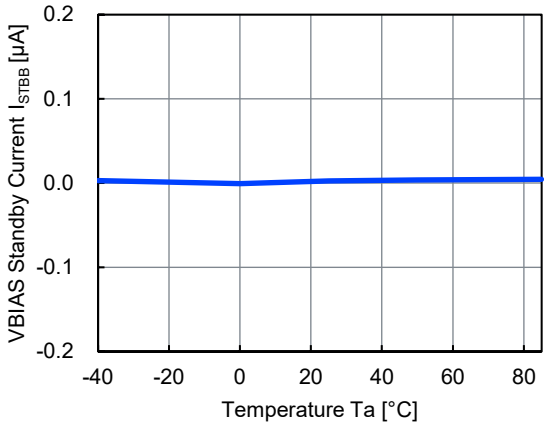
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



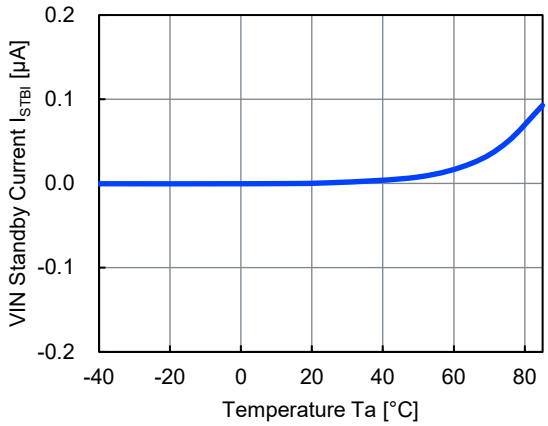
RP120Z201D , V_{IN} = 2.5 V



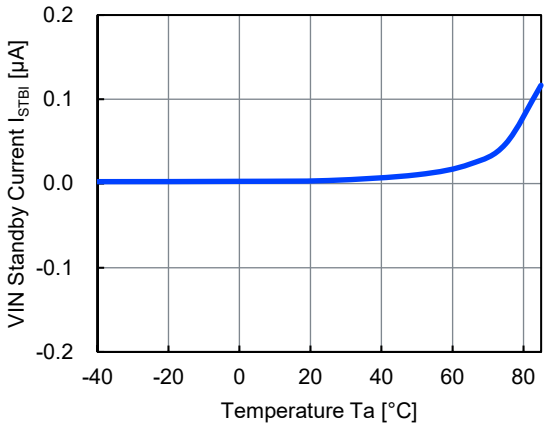
5) VIN pin Standby Current vs. Temperature

V_{BIAS} = 5.5 V, CE = 0 V

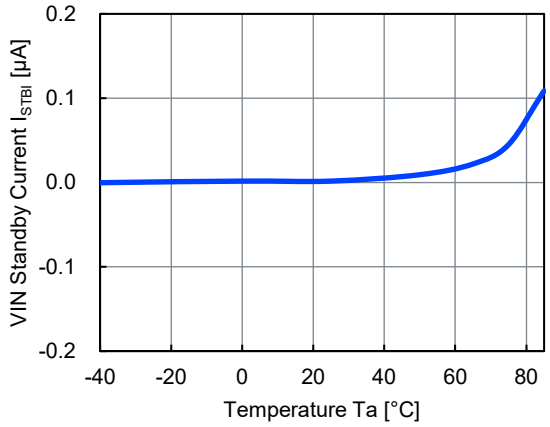
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



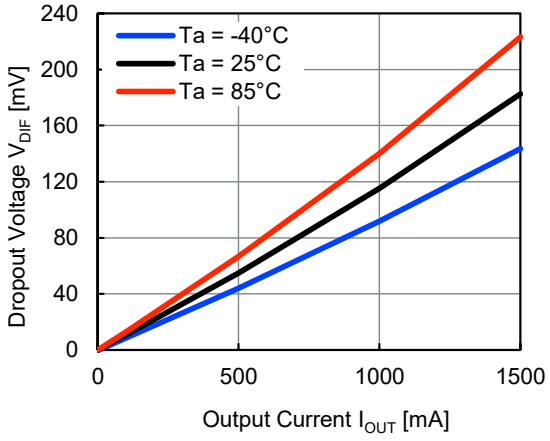
RP120Z201D , V_{IN} = 2.5 V



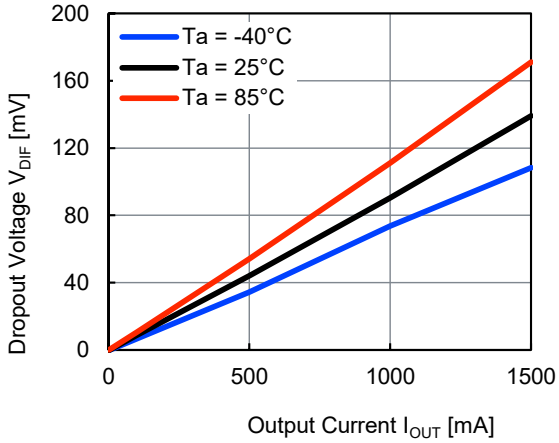
6) Dropout Voltage vs. Output Current

RP120Z121D , CE = V_{BIAS}

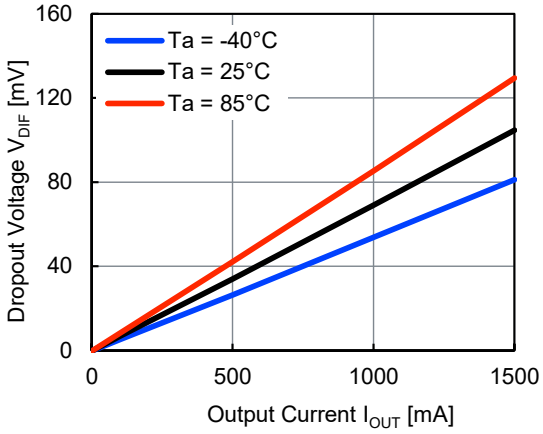
V_{BIAS} = 2.7 V



V_{BIAS} = 3.0 V



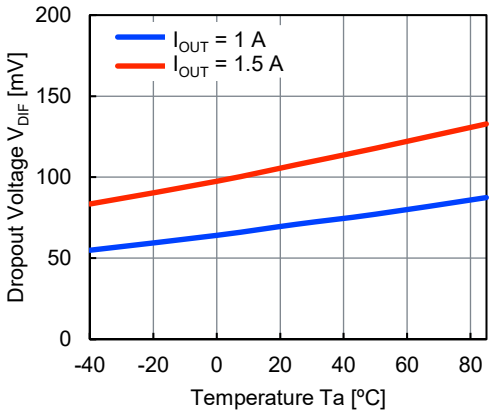
V_{BIAS} = 3.6 V



7） Dropout Voltage vs. Temperature

V_{BIAS} = 3.0 V , CE = V_{BIAS}

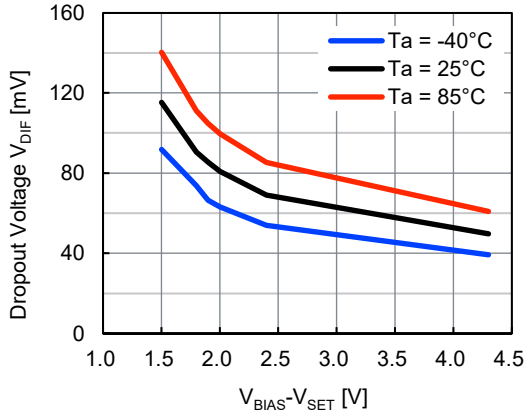
RP120Z061D



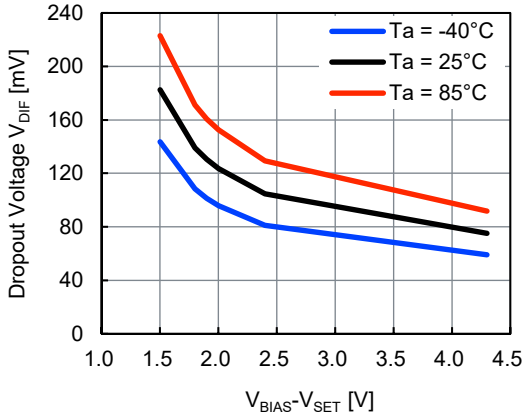
8） Dropout Voltage vs. Driver Drive Voltage（V_{BIAS} - V_{SET}）

RP120Z121D , CE = V_{BIAS}

I_{OUT} = 1.0 A



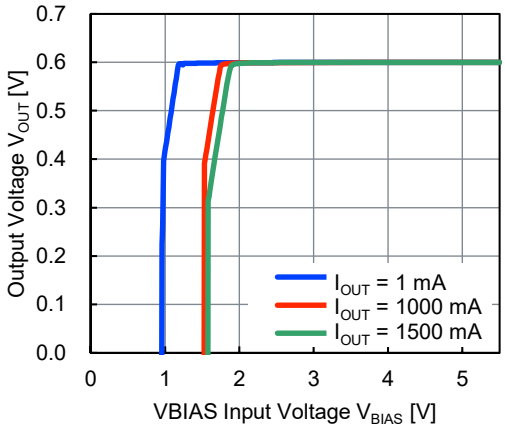
I_{OUT} = 1.5 A



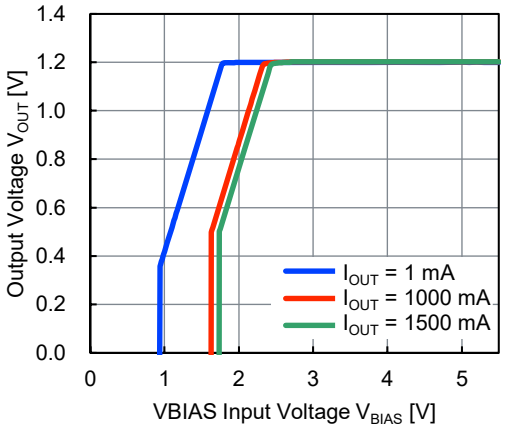
9) Output Voltage vs. VBIAS Input Voltage

V_{BIAS} = 5.5 to 0 V Sweep , CE = V_{BIAS}

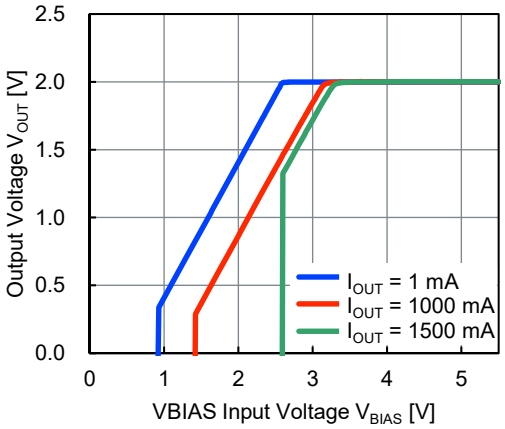
RP120Z061D , V_{IN} = 1.1V



RP120Z121D , V_{IN} = 1.7V



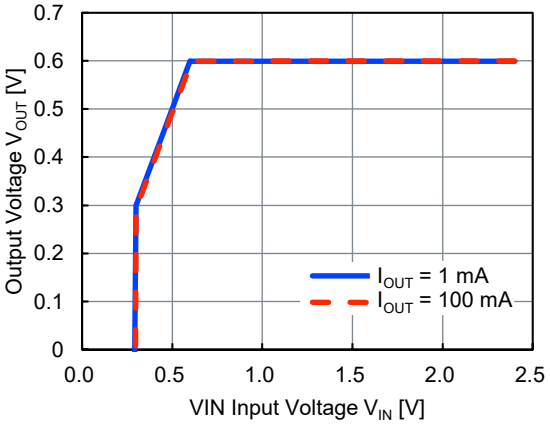
RP120Z201D , V_{IN} = 2.5V



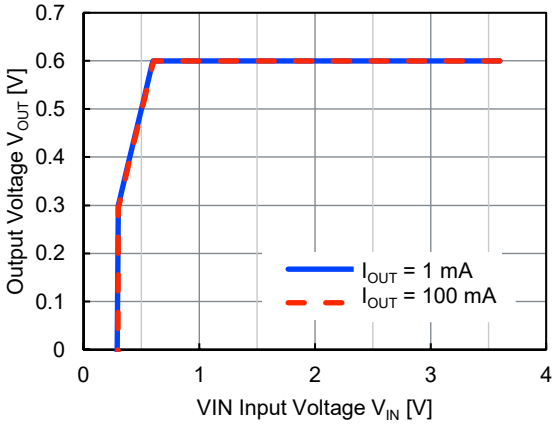
10) Output Voltage vs. VIN Input Voltage

RP120Z061D , V_{IN} = V_{BIAS} to 0 V Sweep , CE = V_{BIAS}

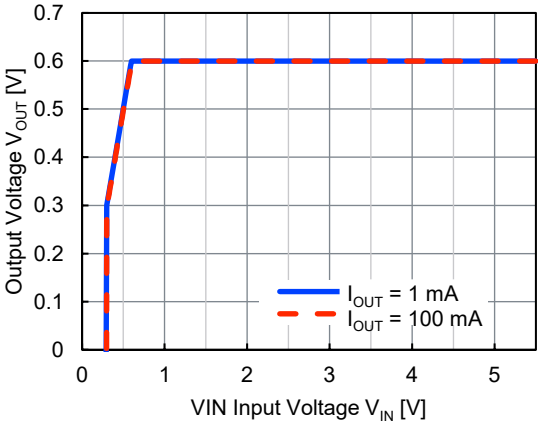
V_{BIAS} = 2.4 V



V_{BIAS} = 3.6 V

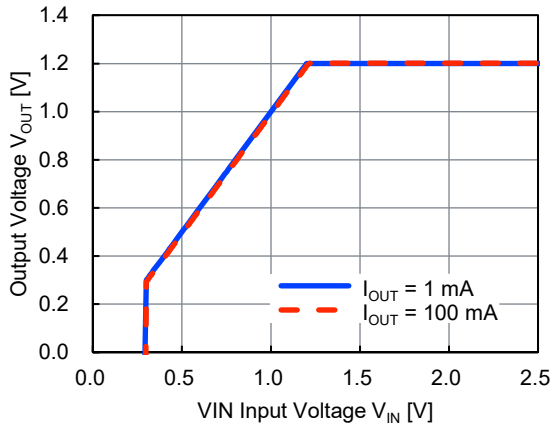


V_{BIAS} = 5.5 V

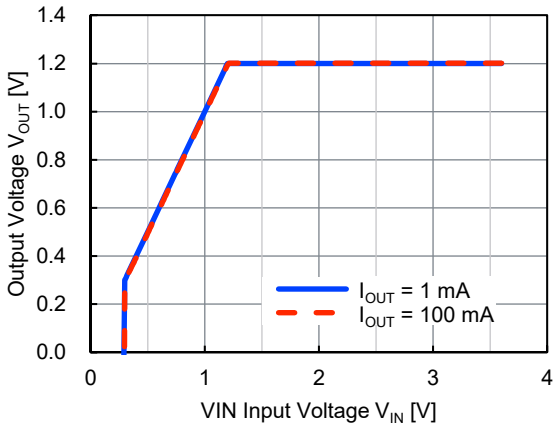


RP120Z121D , V_{IN} = V_{BIAS} to 0 V Sweep , CE = V_{BIAS}

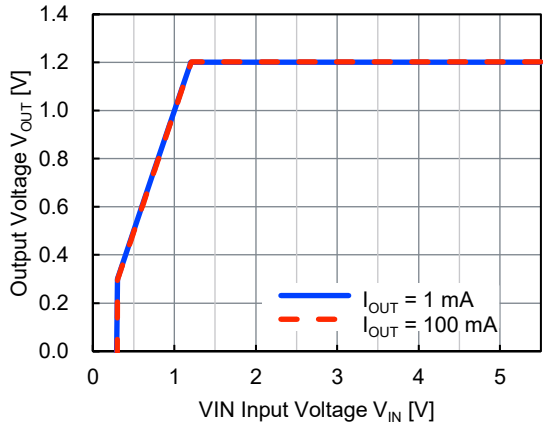
V_{BIAS} = 2.7 V



V_{BIAS} = 3.6 V

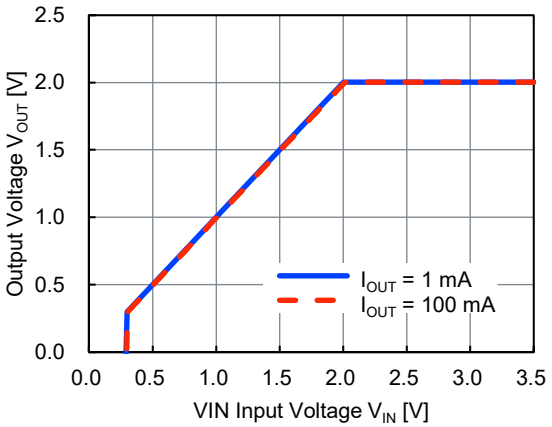


V_{BIAS} = 5.5 V

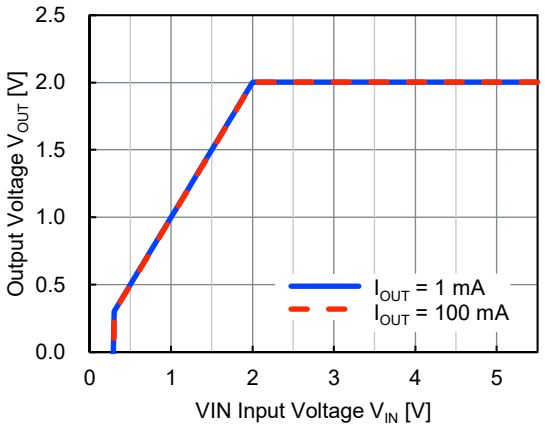


RP120Z201D , V_{IN} = V_{BIAS} to 0 V Sweep , CE = V_{BIAS}

V_{BIAS} = 3.5 V



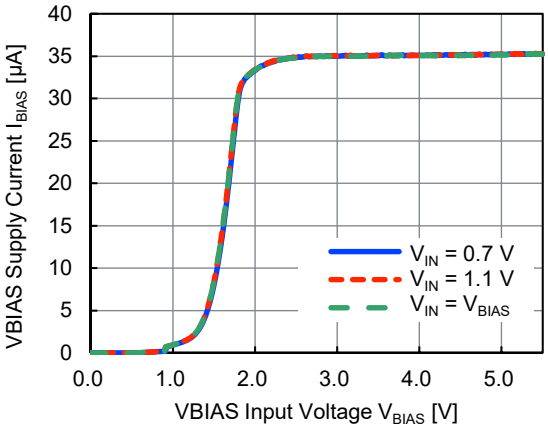
V_{BIAS} = 5.5 V



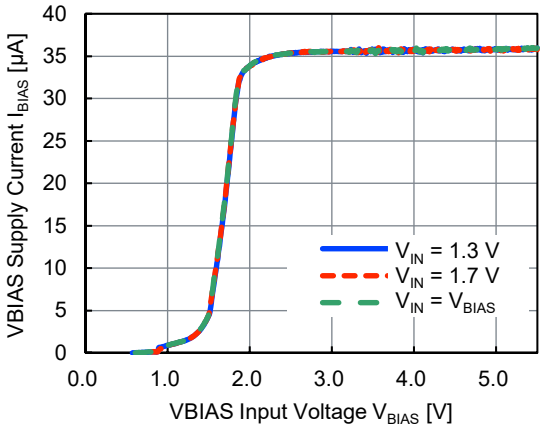
11) VBIAS pin Supply Current vs. VBIAS Input Voltage

V_{BIAS} = 5.5 to 0 V Sweep , CE = V_{BIAS}

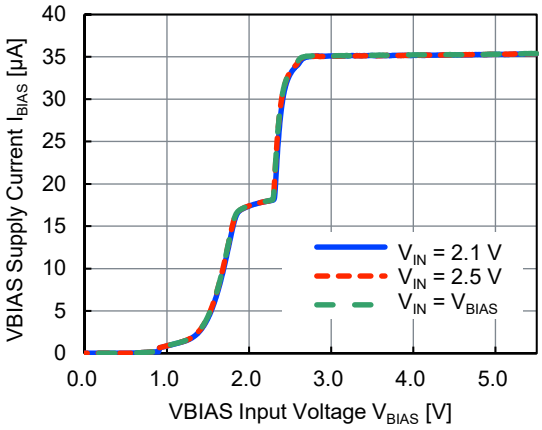
RP120Z061D



RP120Z121D



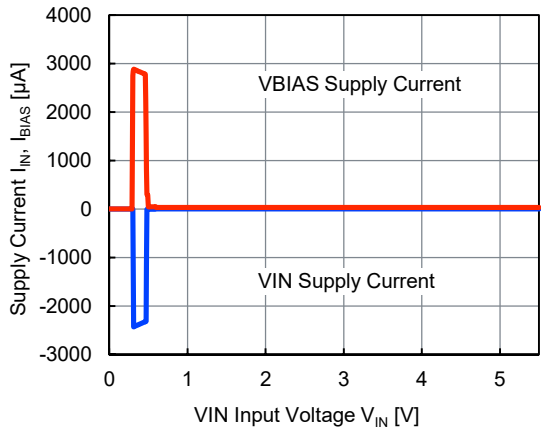
RP120Z201D



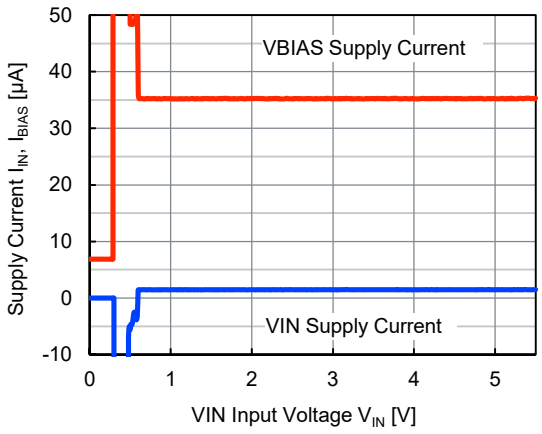
12) Supply Current vs. VIN Input Voltage

RP120Z061D , V_{BIAS} = 5.5 V , V_{IN} = 5.5 to 0 V Sweep , CE = V_{BIAS}

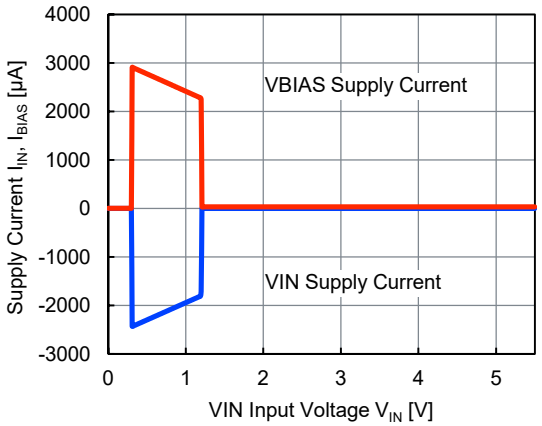
Overall View



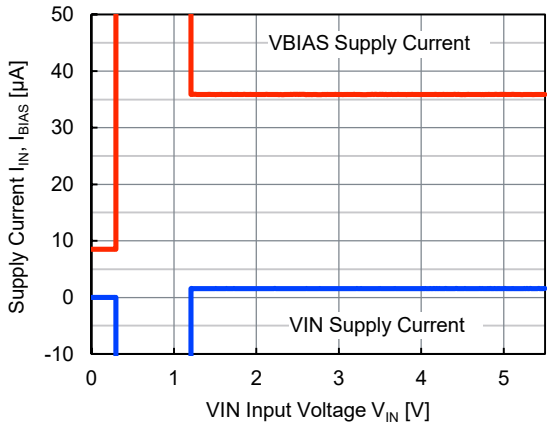
Zoom-in View



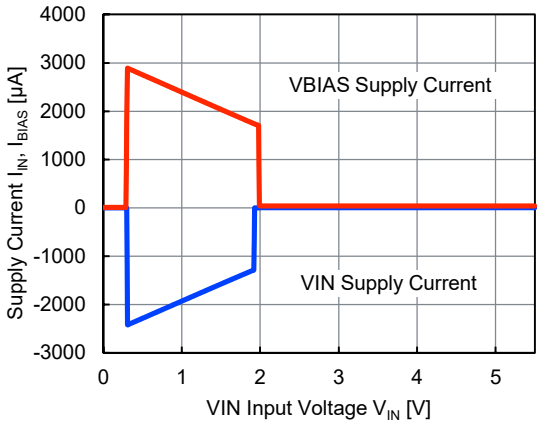
RP120Z121D
Overall View



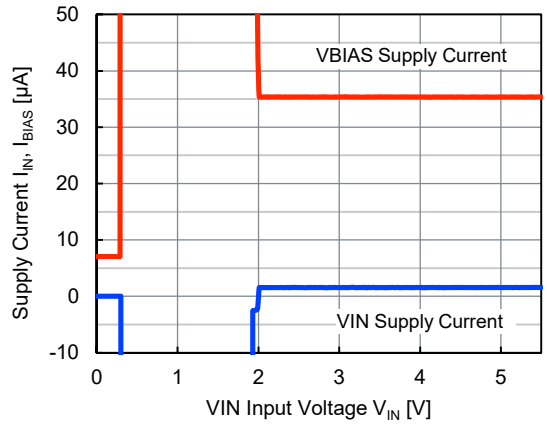
Zoom-in View



RP120Z201D
Overall View



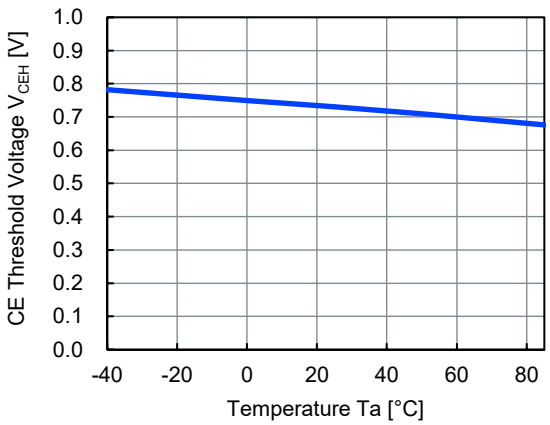
Zoom-in View



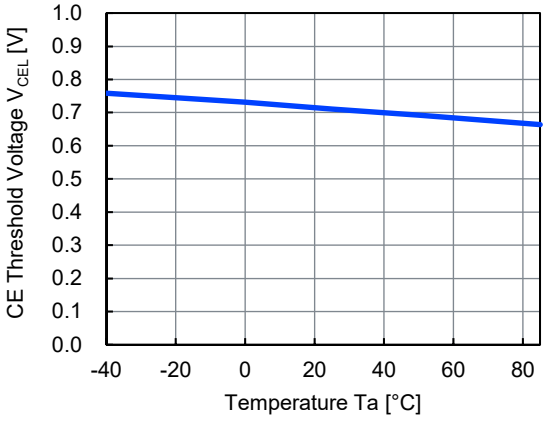
Note that if the input voltage V_{IN} drops below the output set voltage V_{SET}, current will flow from the V_{BIAS} pin to the V_{IN} pin via the inside of the IC. However, it does not flow under the condition that V_{BIAS} decreases at the with V_{IN}.

13) Chip Enable Threshold Voltage vs. Temperature

RP120Z121D , V_{BIAS} = 3.6 V , V_{IN} = 1.7 V
CE = "High"



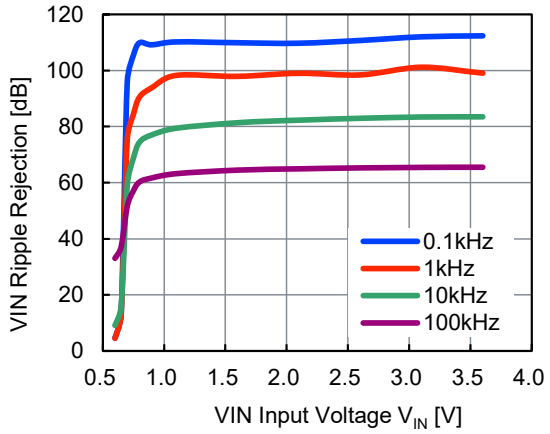
CE = "Low"



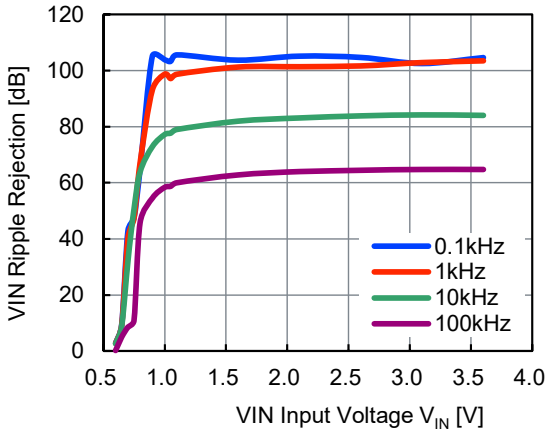
14) VIN **Ripple Rejection vs. VIN Input Voltage**

RP120Z061D , V_{BIAS} = 3.6 V , V_{IN} = V_{BIAS} to 0.6 V , Vripple = 0.2V p-p , CE = V_{BIAS}

I_{OUT} = 1 mA

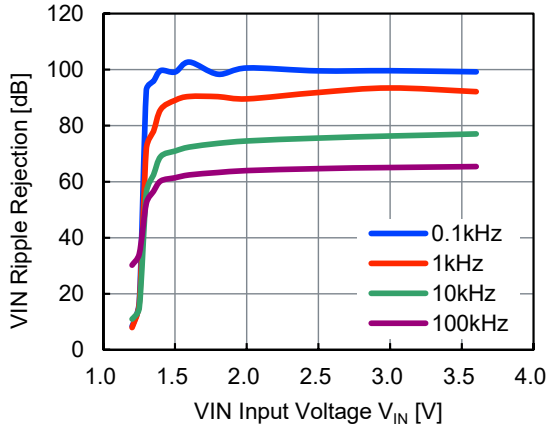


I_{OUT} = 100 mA

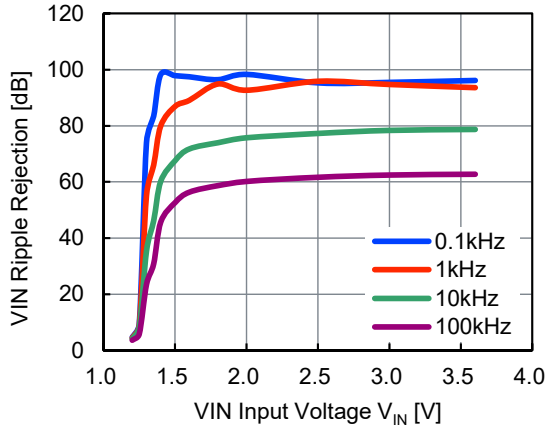


RP120Z121D , V_{BIAS} = 3.6 V , V_{IN} = V_{BIAS} to 1.2 V , Vripple = 0.2V p-p , CE = V_{BIAS}

I_{OUT} = 1 mA

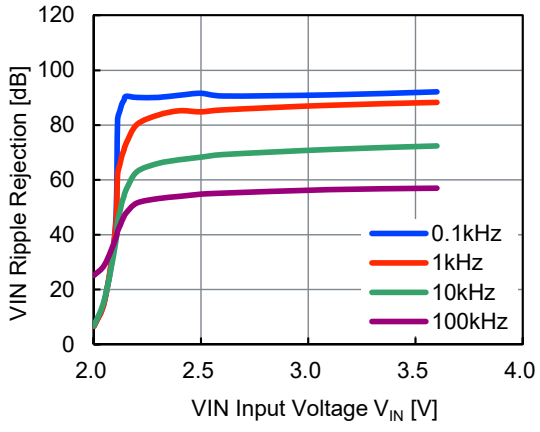


I_{OUT} = 100 mA

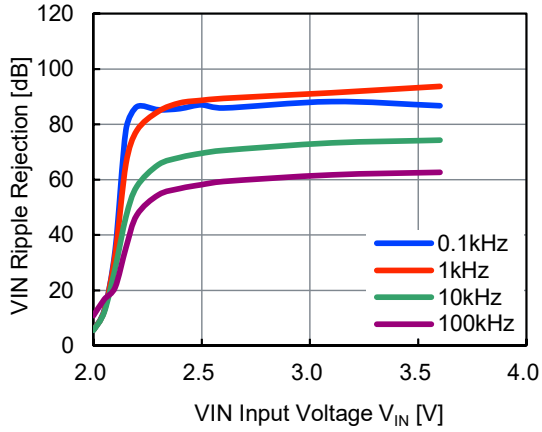


RP120Z201D , V_{BIAS} = 3.6 V , V_{IN} = V_{BIAS} to 2.0 V , Vripple = 0.2V p-p , CE = V_{BIAS}

I_{OUT} = 1 mA



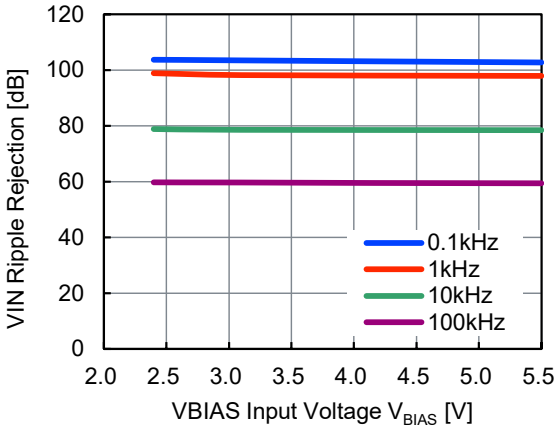
I_{OUT} = 100 mA



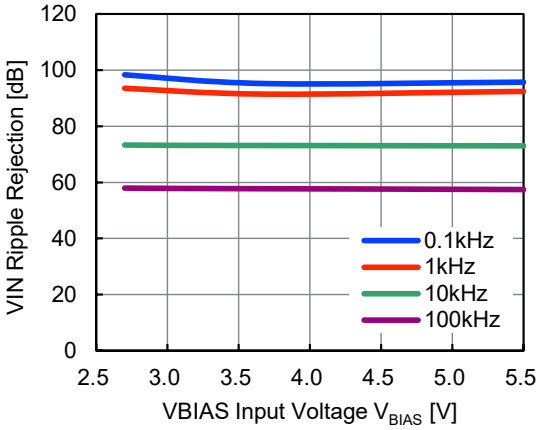
15) VIN Ripple Rejection vs. VBIAS Input Voltage

V_{IN} = 1.1 V , Vripple = 0.2V p-p , CE = V_{BIAS} , I_{OUT} = 100 mA

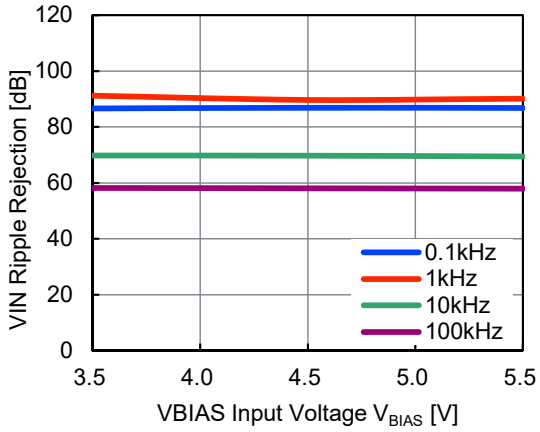
RP120Z061D



RP120Z121D



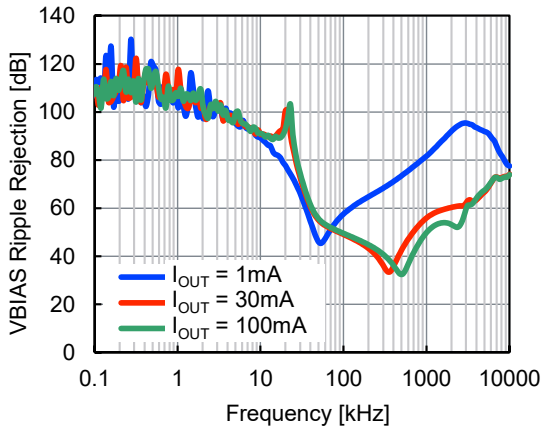
RP120Z201D



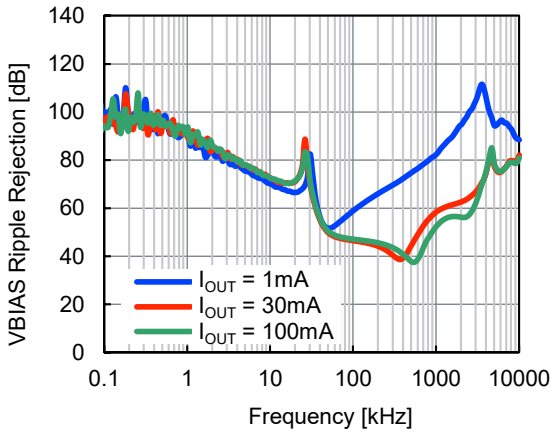
16) VBIAS Ripple Rejection vs. Frequency

V_{BIAS} = 3.6 V , Vripple = 0.2V p-p , CE = V_{BIAS}

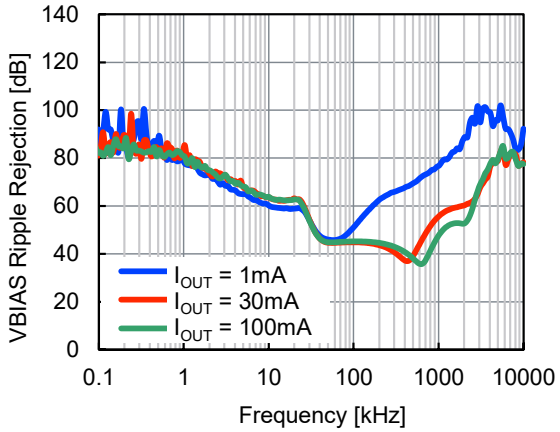
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



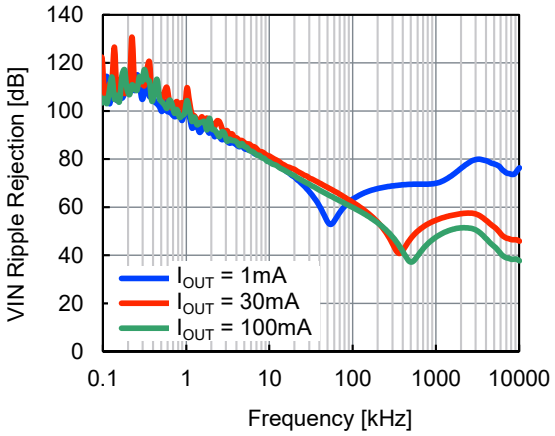
RP120Z201D , V_{IN} = 2.5 V



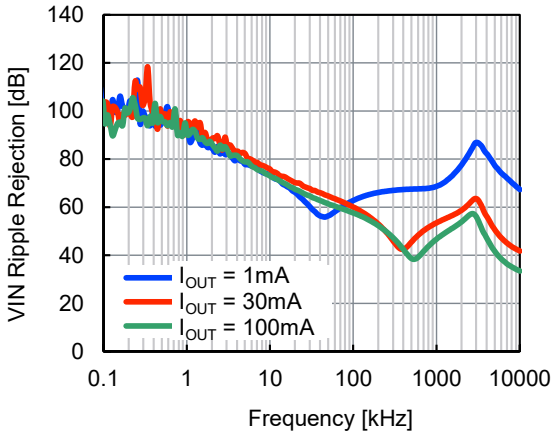
17) VIN **Ripple Rejection vs. Frequency**

V_{BIAS} = 3.6 V

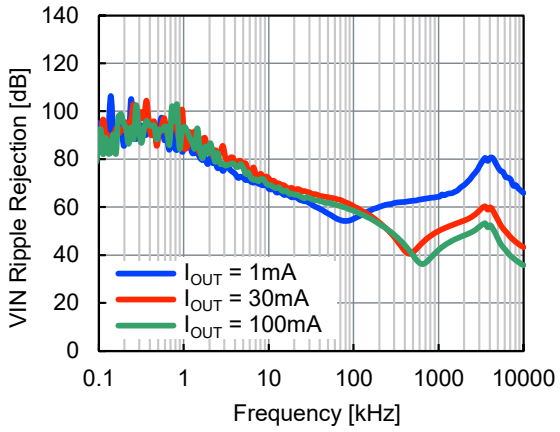
RP120Z061D , V_{IN} = 1.1 V , Vripple = 0.2V p-p



RP120Z121D , V_{IN} = 1.7 V , Vripple = 0.2V p-p



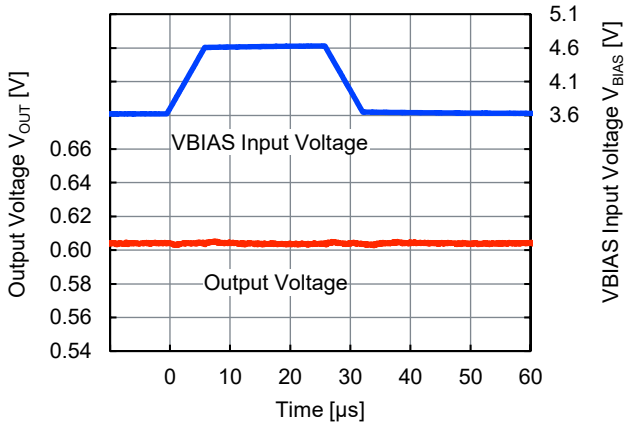
RP120Z201D , V_{IN} = 2.5 V , Vripple = 0.2V p-p



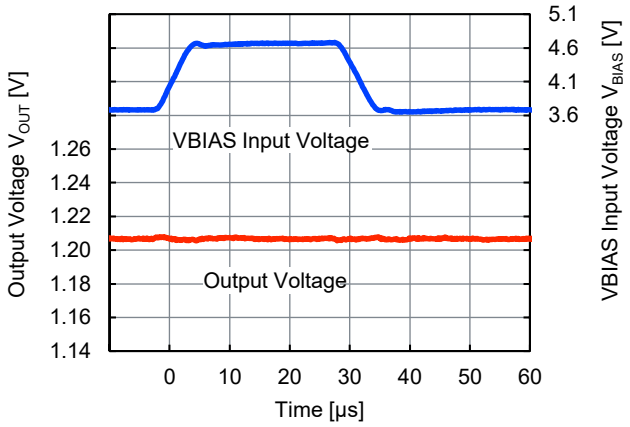
18) VBIAS Input Transient Response

V_{BIAS} = 3.6 ⇔ 4.6 V , CE = V_{BIAS} , I_{OUT} = 10 mA

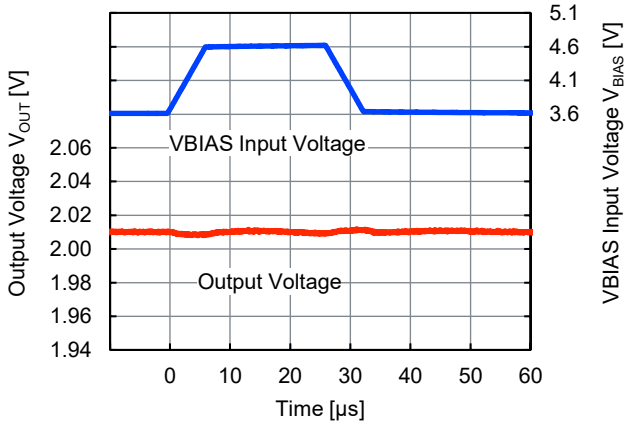
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



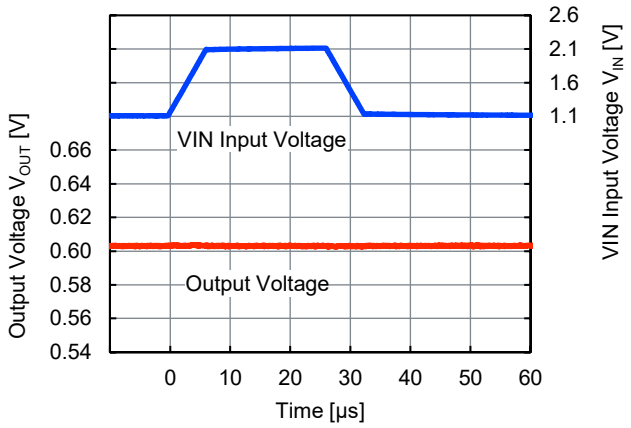
RP120Z201D , V_{IN} = 2.5 V



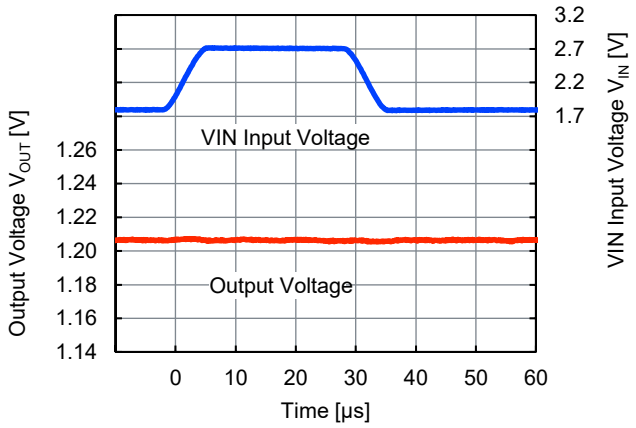
19) VIN Input Transient Response

V_{BIAS} = 3.6 V , CE = V_{BIAS} , I_{OUT} = 10 mA

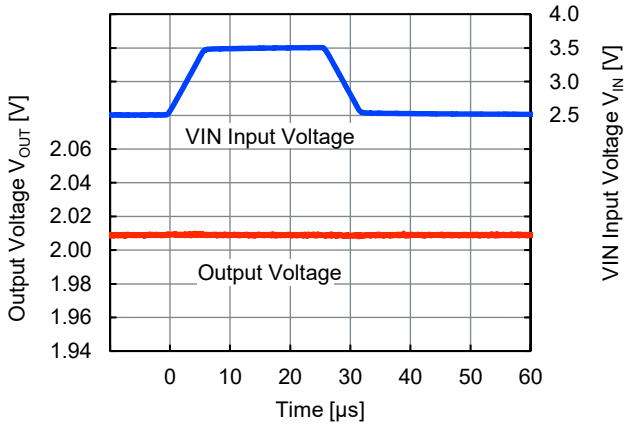
RP120Z061D , V_{IN} = 1.1 ⇔ 2.1 V



RP120Z121D , V_{IN} = 1.7 ⇔ 2.7 V



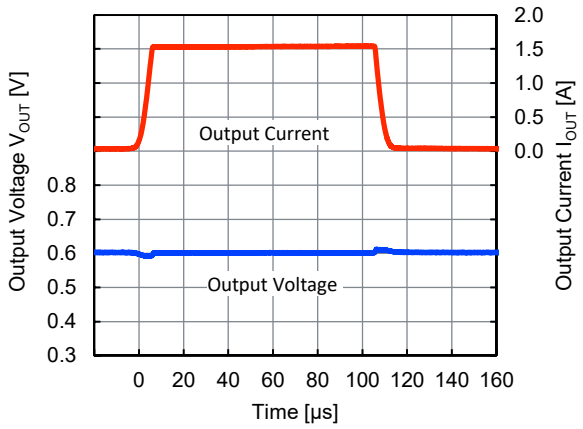
RP120Z201D , V_{IN} = 2.5 ⇔ 3.5 V



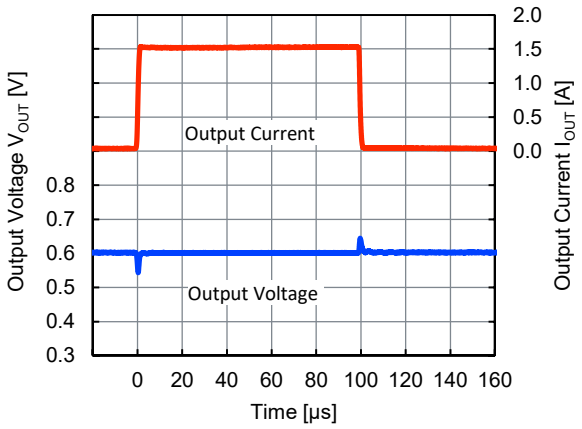
20) Load Transient Response

RP120Z061D , V_{BIAS} = 3.6 V , V_{IN} = 1.1 V , CE = V_{BIAS}

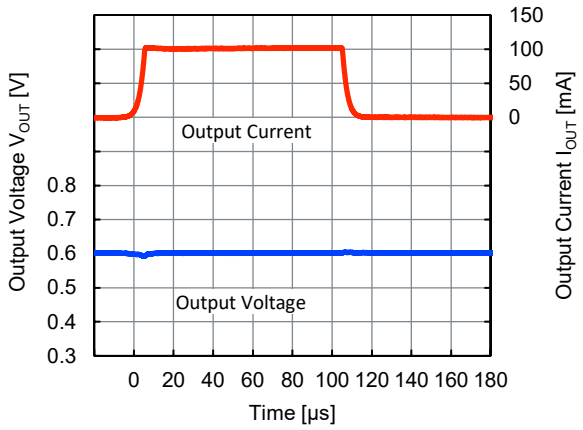
tr = tf = 5.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



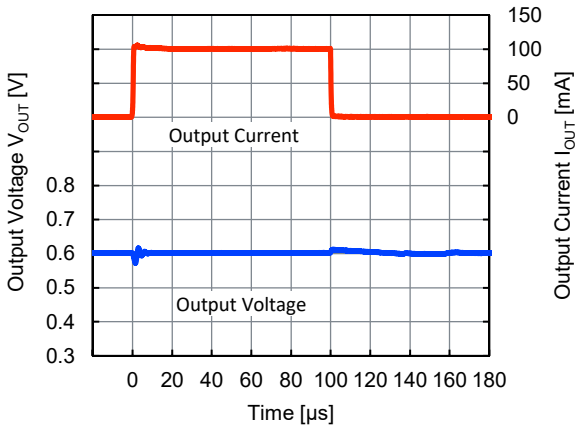
tr = tf = 1.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



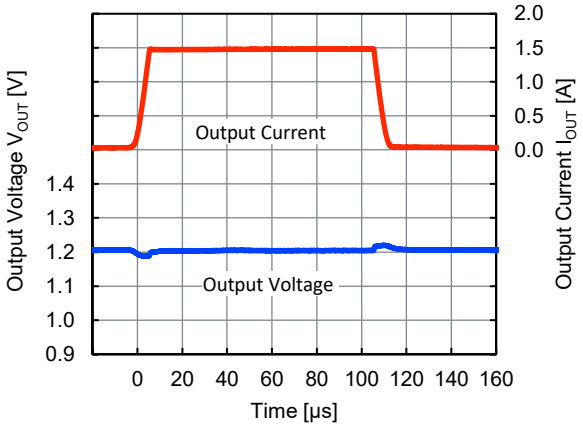
tr = tf = 5.0 µs , I_{OUT} = 1 mA ⇔ 100 mA



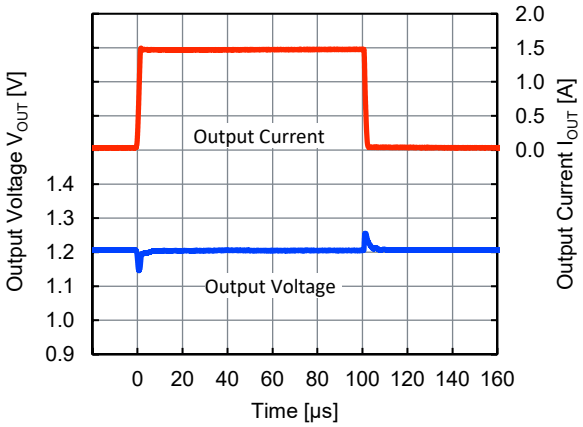
tr = tf = 0.5 µs , I_{OUT} = 1 mA ⇔ 100 mA



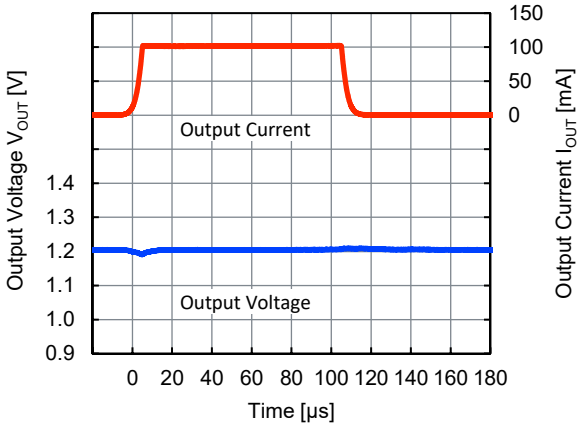
RP120Z121D , V_{BIAS} = 3.6 V , V_{IN} = 1.7 V , CE = V_{BIAS}
tr = tf = 5.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



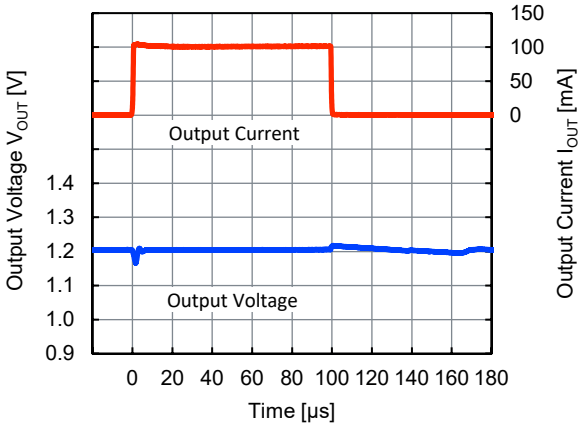
tr = tf = 1.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



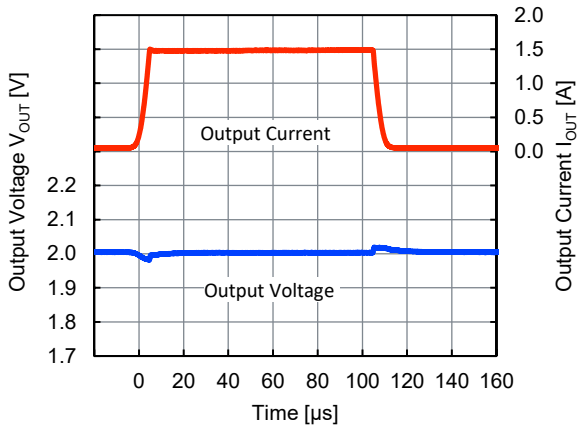
tr = tf = 5.0 µs , I_{OUT} = 1 mA ⇔ 100 mA



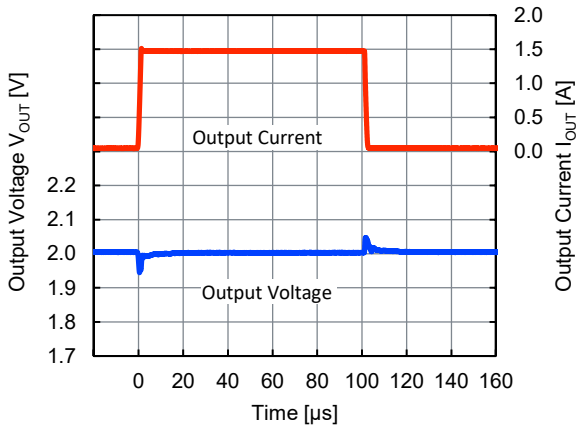
tr = tf = 0.5 µs , I_{OUT} = 1 mA ⇔ 100 mA



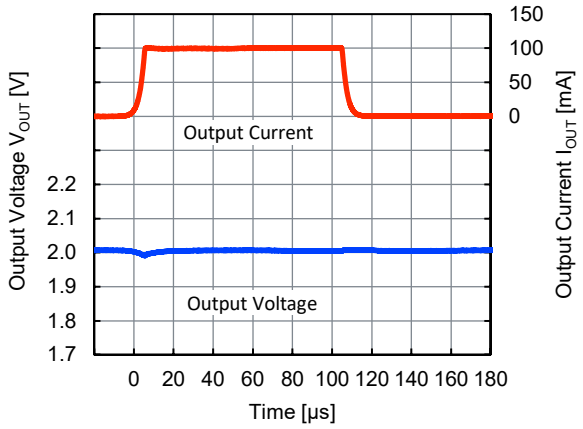
RP120Z201D , V_{BIAS} = 3.6 V , V_{IN} = 2.5 V , CE = V_{BIAS}
tr = tf = 5.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



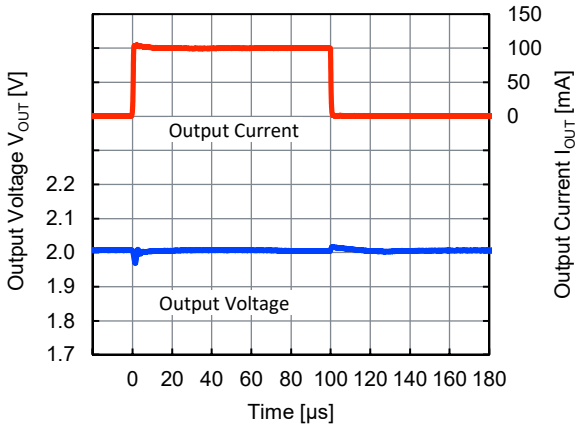
tr = tf = 1.0 µs , I_{OUT} = 30 mA ⇔ 1.5 A



tr = tf = 5.0 µs , I_{OUT} = 1 mA ⇔ 100 mA



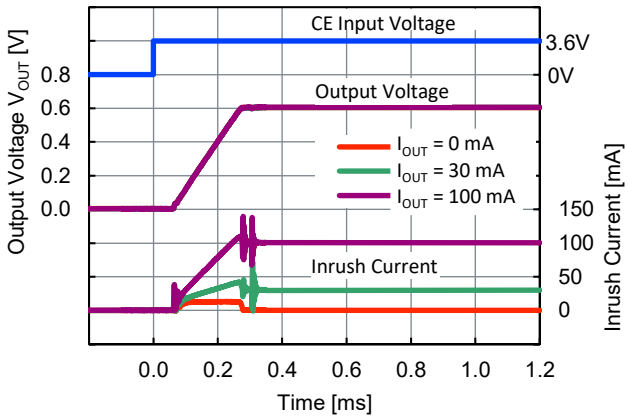
tr = tf = 0.5 µs , I_{OUT} = 1 mA ⇔ 100 mA



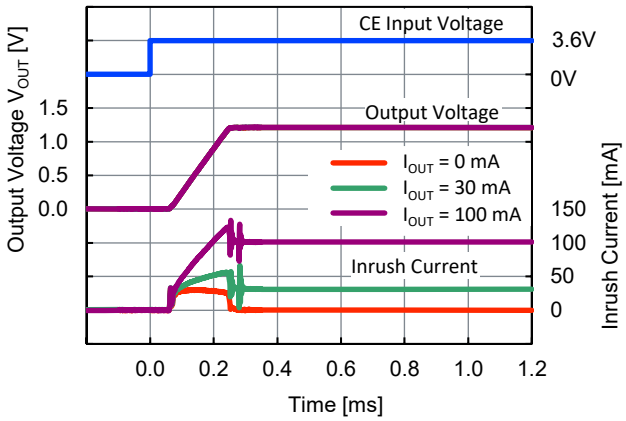
21) Characteristics of Turn On with CE Pin

V_{BIAS} = 3.6 V , CE = 0 V to V_{BIAS} , C_{OUT} = 4.7 µF

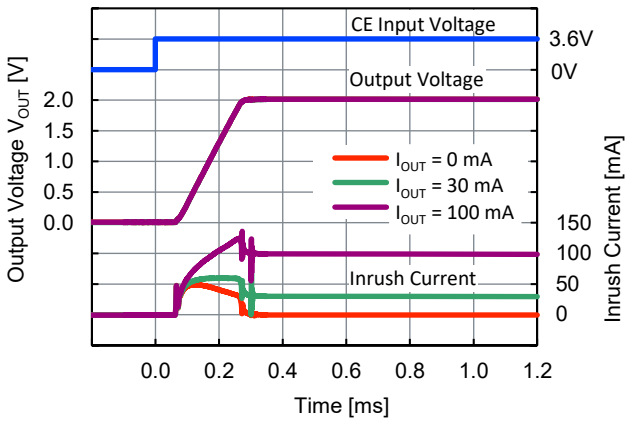
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



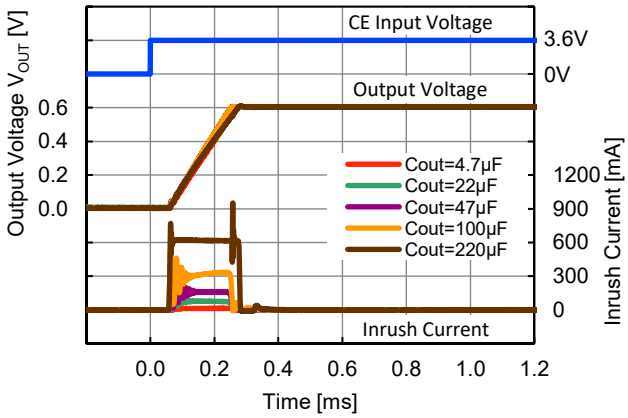
RP120Z201D , V_{IN} = 2.5 V



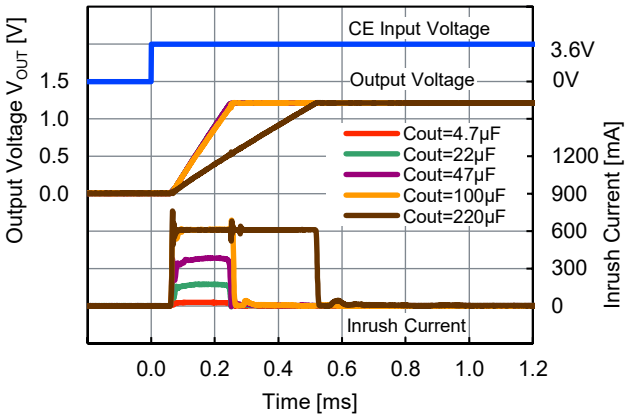
22) Inrush Current

V_{BIAS} = 3.6 V , CE = 0 V to V_{BIAS} , I_{OUT} = 0 mA

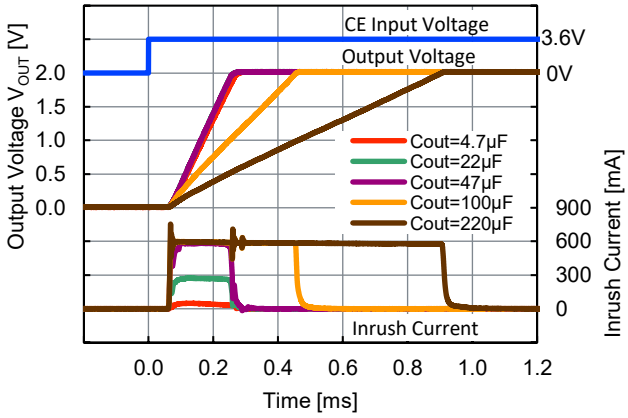
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



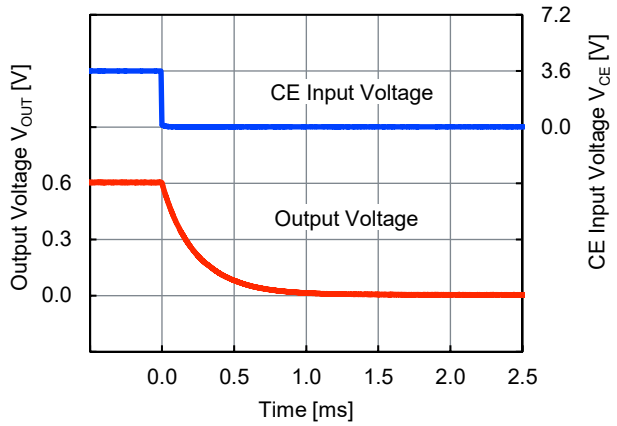
RP120Z201D , V_{IN} = 2.5 V



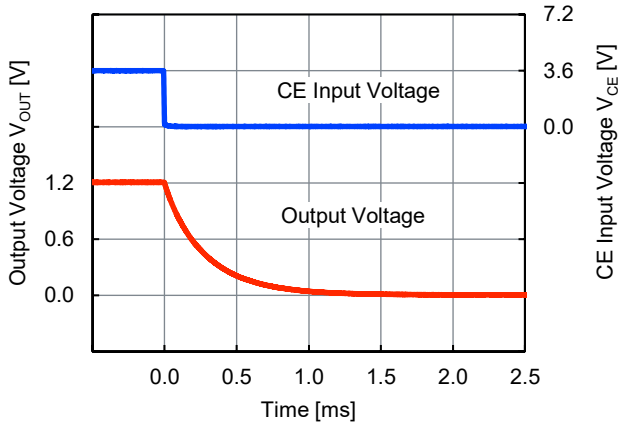
23) Characteristics of Turn Off with CE Pin

V_{BIAS} = 3.6 V , CE = V_{BIAS} to 0 V , I_{OUT} = 0 mA

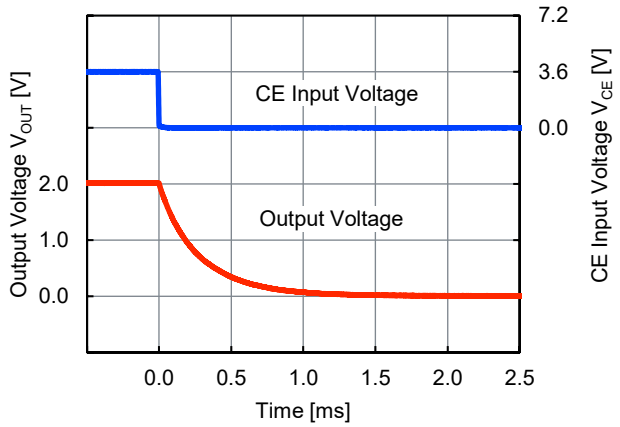
RP120Z061D , V_{IN} = 1.1 V



RP120Z121D , V_{IN} = 1.7 V



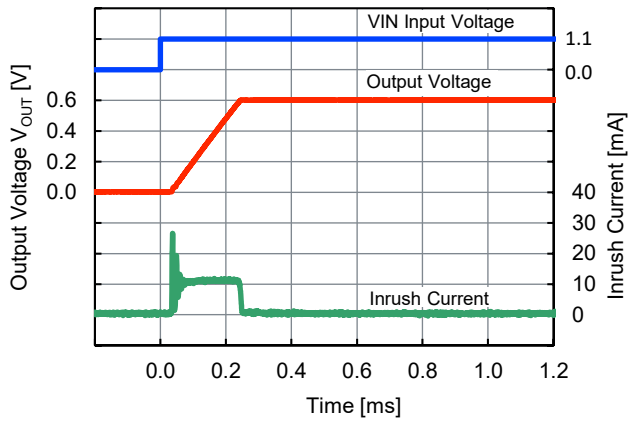
RP120Z201D , V_{IN} = 2.5 V



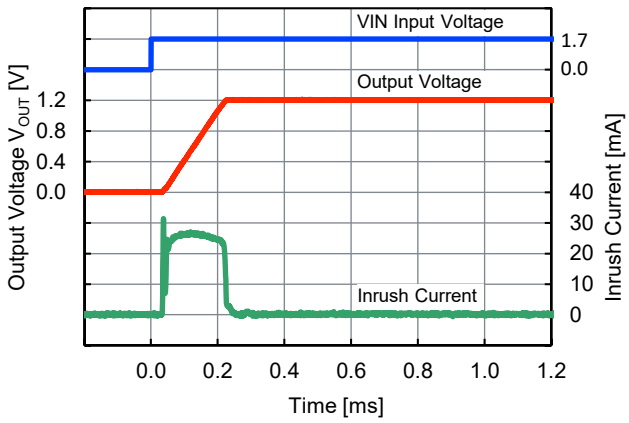
24) VIN Power-on Transient Response

V_{BIAS} = 3.6 V , CE = V_{BIAS} , I_{OUT} = 0 mA

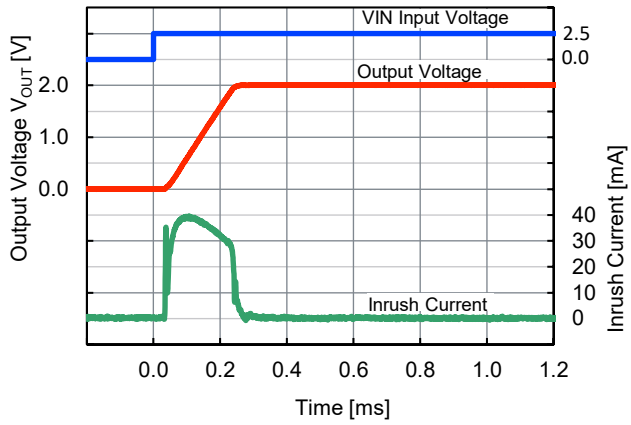
RP120Z061D , V_{IN} = 0 to 1.1 V



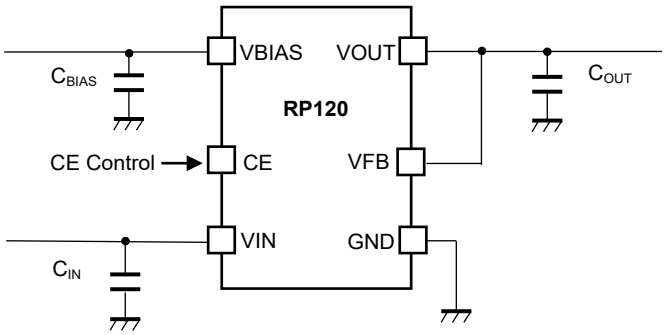
RP120Z121D , V_{IN} = 0 to 1.7 V



RP120Z201D , V_{IN} = 0 to 2.5 V



Test Circuit

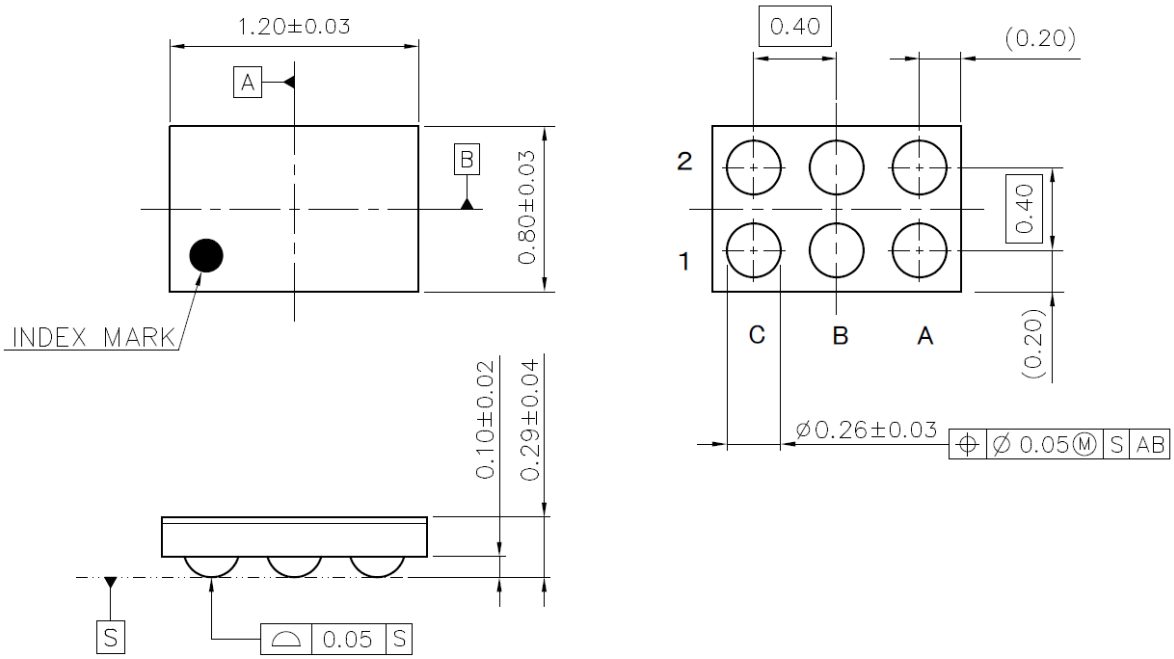


Test **Circuit**

Components List for Our Evaluation

Symbol	Capacitance	Maker	Parts Number
C_{IN}	1 µF	Murata	GRM033R61A105ME15D
C_{BIAS}	1 µF	Murata	GRM033R61A105ME15D
C_{OUT}	4.7 µF	Murata	GRM155R60J475ME47D

DM- WLCSP-6-P11-JE-A

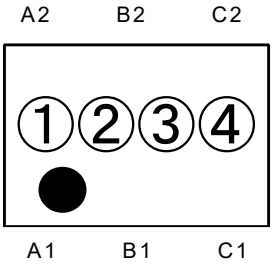


UNIT: mm

WLCSP-6-P11 Package Dimensions

①②: Product Code ⋯ **Refer to the following table**

③④: Lot Number ⋯ Alphanumeric Serial Number

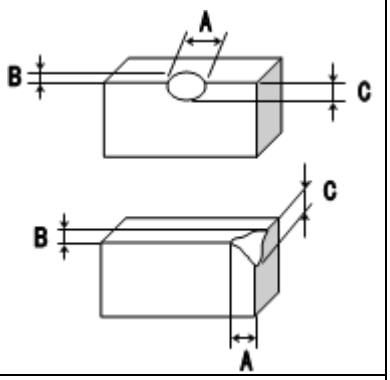


WLCSP-6-P11 Marking Specification

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

RP120Z Marking List

Product Name	① ②
RP120Z001D	A A
RP120Z061D	A C
RP120Z071D	A E
RP120Z071D5	A Y
RP120Z081D	A F
RP120Z081D5	C E
RP120Z091D	A G
RP120Z101D	A H
RP120Z111D	A J
RP120Z121D	A K
RP120Z131D	A L
RP120Z141D	A N
RP120Z151D	A P
RP120Z161D	A R
RP120Z171D	A T
RP120Z181D	A U
RP120Z191D	A V
RP120Z201D	A X

No.	Inspection Items	Inspection Criteria	Figure
1	Package chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A≥0.2mm, B≤0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
3. This product and any technical information relating thereto are subject to complementary export controls (so-called KNOW controls) under the Foreign Exchange and Foreign Trade Law, and related politics ministerial ordinance of the law. (Note that the complementary export controls are inapplicable to any application-specific products, except rockets and pilotless aircraft, that are insusceptible to design or program changes.) Accordingly, when exporting or carrying abroad this product, follow the Foreign Exchange and Foreign Trade Control Law and its related regulations with respect to the complementary export controls.
4. The technical information described in this document shows typical characteristics and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under our or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death should first contact us.
    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

NISSHINBO

Nisshinbo Micro Devices Inc.

Official website
https://www.nisshinbo-microdevices.co.jp/en/

Purchase information
https://www.nisshinbo-microdevices.co.jp/en/buy/