



# Am29861A

## High-Performance Bus Transceiver

### DISTINCTIVE CHARACTERISTICS

- High-speed symmetrical bidirectional transceiver
  - $t_{PD} = 5$  ns typical
- 200-mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down
- $I_{OL}$ : 48 mA commercial
- Higher speed, lower power version of the Am29861

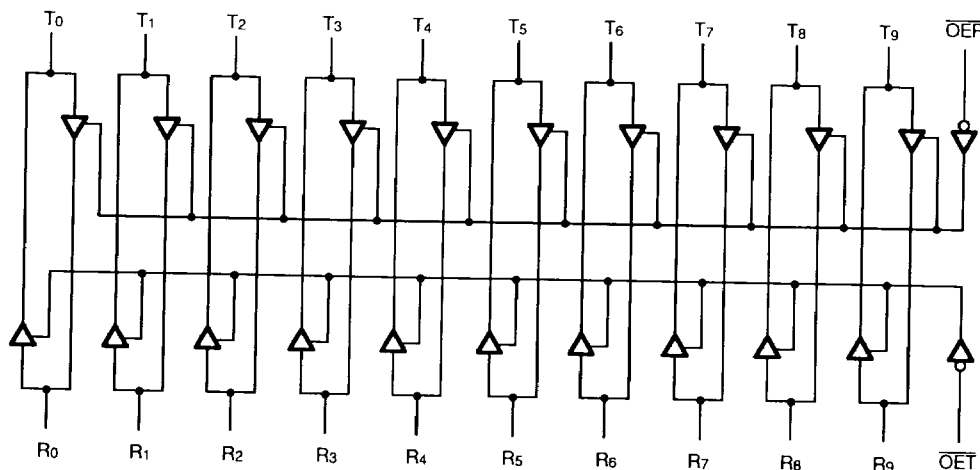
### GENERAL DESCRIPTION

The Am29861A Bus Transceiver provides high-performance bus interface buffering for wide address/data paths or buses carrying parity. The device is a 10-bit bidirectional transceiver. The device features data inputs with 200-mV minimum input hysteresis. The Am29861A is

produced with AMD's proprietary IMOX bipolar process, and features typical propagation delays of 5 ns.

Each member of the Am29800A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both the inputs and outputs.

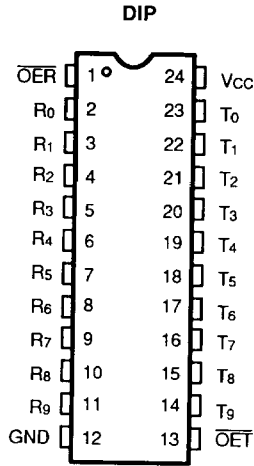
### BLOCK DIAGRAM



07142-001A

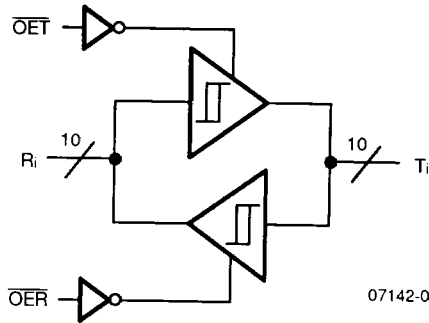
**CONNECTION DIAGRAM**

Top View



07142-002A

**LOGIC SYMBOLS**



07142-003A

**FUNCTION TABLE**

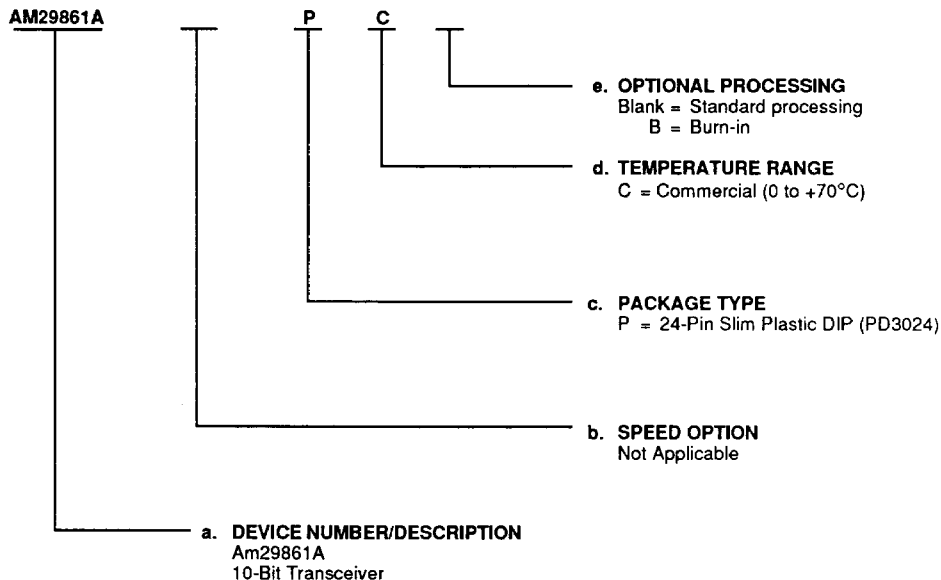
Inputs				Outputs		Function
OET	OER	R <sub>i</sub>	T <sub>i</sub>	R <sub>i</sub>	T <sub>i</sub>	
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

H = HIGH                      L = LOW  
 Z = High Impedance        X = Don't Care  
 N/A = Not Applicable

**ORDERING INFORMATION****Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option (if applicable)**
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM29861A	PC

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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**PIN DESCRIPTION****Am29861A** **$\overline{\text{OER}}$** **Output Enable-Receive (Input, Active LOW)**

When LOW in conjunction with  $\overline{\text{OET}}$  HIGH, the devices are in the Receive mode ( $R_i$  are outputs,  $T_i$  are inputs).

 **$\overline{\text{OET}}$** **Output Enable-Transmit (Input, Active LOW)**

When LOW in conjunction with  $\overline{\text{OER}}$  HIGH, the devices are in the Transmit mode ( $R_i$  are inputs,  $T_i$  are outputs).

 **$R_i$** **Receive Port (Input/Output)**

$R_i$  are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

 **$T_i$** **Transmit Port (Input/Output)**

$T_i$  are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Output For High Output State	-0.5 V to +5.5 V
DC Input Voltage	-1.5 V to +6.0 V
DC Output Current, Into Outputs	100 mA
DC Input Current	-30 mA to +5.0 mA

## OPERATING RANGES

### Commercial (C) Devices

Temperature (T <sub>A</sub> )	0 to +70°C
Supply Voltage (V <sub>CC</sub> )	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -15 mA	2.4	V
			I <sub>OH</sub> = -24 mA	2.0	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 48 mA	0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed input logical LOW voltage for all inputs (Note 1)		0.8	V
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-1.2	V
V <sub>HYST</sub>	Input Hysteresis		200		mV
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V		-0.5	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V		50	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V		100	μA
I <sub>ZL</sub>	I/O Port LOW Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V		-550	μA
I <sub>ZH</sub>	I/O Port HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V		100	μA
I <sub>ZI</sub>	I/O Port HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V		150	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V (Note 2)	-75	-250	mA
I <sub>OFF</sub>	Bus Leakage Current	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 2.9 V		100	μA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 5.5 V Outputs Unloaded	Outputs LOW	140	mA
			Outputs HIGH	115	
			Outputs Hi-Z	130	

### Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of short-circuit test should not exceed one second

**SWITCHING CHARACTERISTICS over operating range unless otherwise specified**

Symbol	Parameter Description	Parameter Test Conditions*	Min	Max	Unit
t <sub>PLH</sub>	Propagation Delay from	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500 Ω R <sub>2</sub> = 500 Ω		8	ns
t <sub>PHL</sub>	R <sub>i</sub> to T <sub>i</sub> or T <sub>i</sub> to R <sub>i</sub>			8	ns
t <sub>ZH</sub>	Output Enable Time $\overline{OET}$ to			11	ns
t <sub>ZL</sub>	T <sub>i</sub> or $\overline{OER}$ to R <sub>i</sub>			12	ns
t <sub>HZ</sub>	Output Disable Time OET to			10	ns
t <sub>LZ</sub>	T <sub>i</sub> or $\overline{OER}$ to R <sub>i</sub>			10	ns

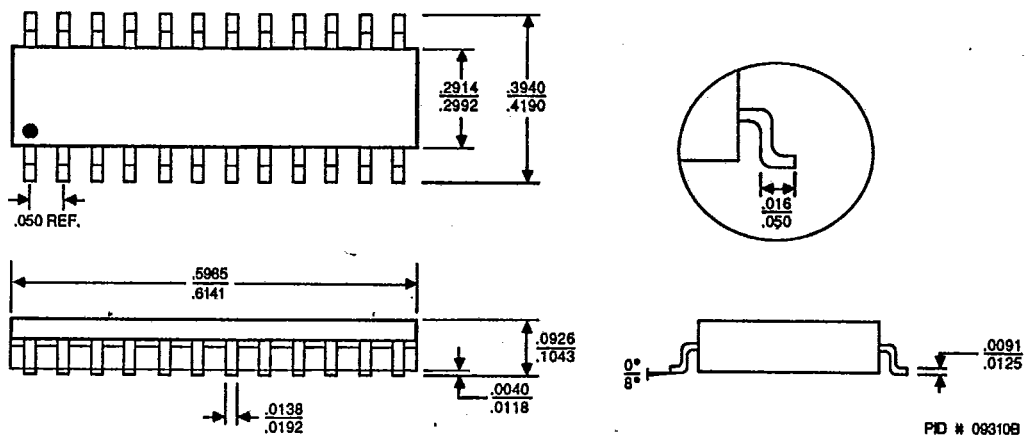
\* See Test Circuit and Waveforms. (Chapter 2)



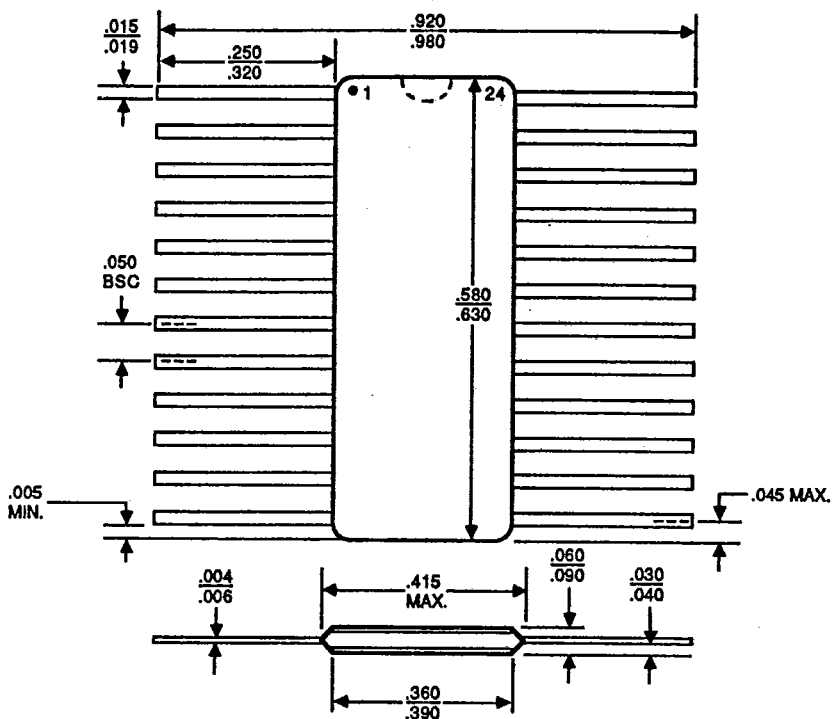
PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



CFM024

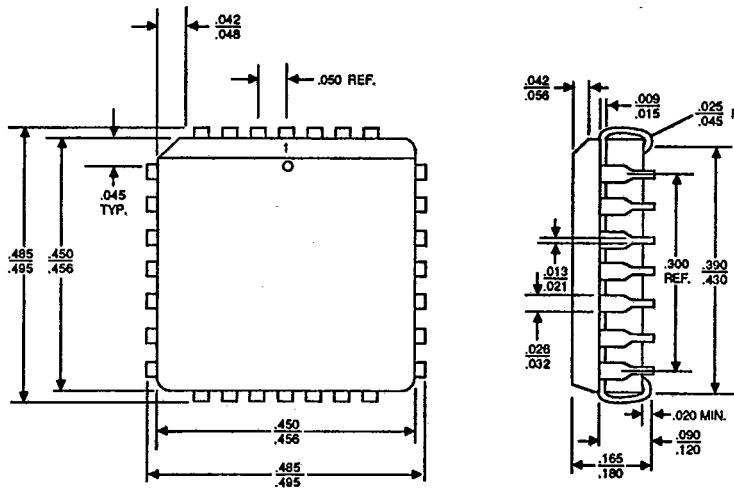




PACKAGE OUTLINES (Cont'd.)

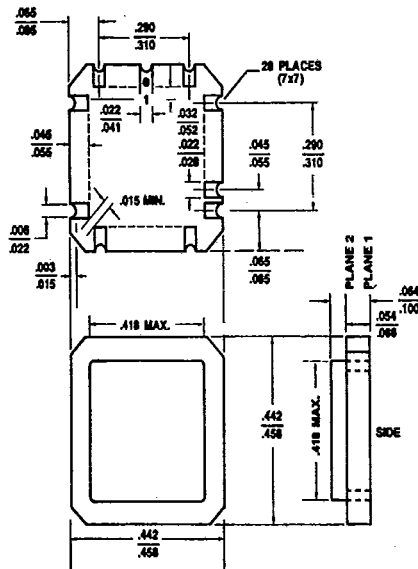
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PL 028



PID # 06751E

CL 028



PID # 06595D

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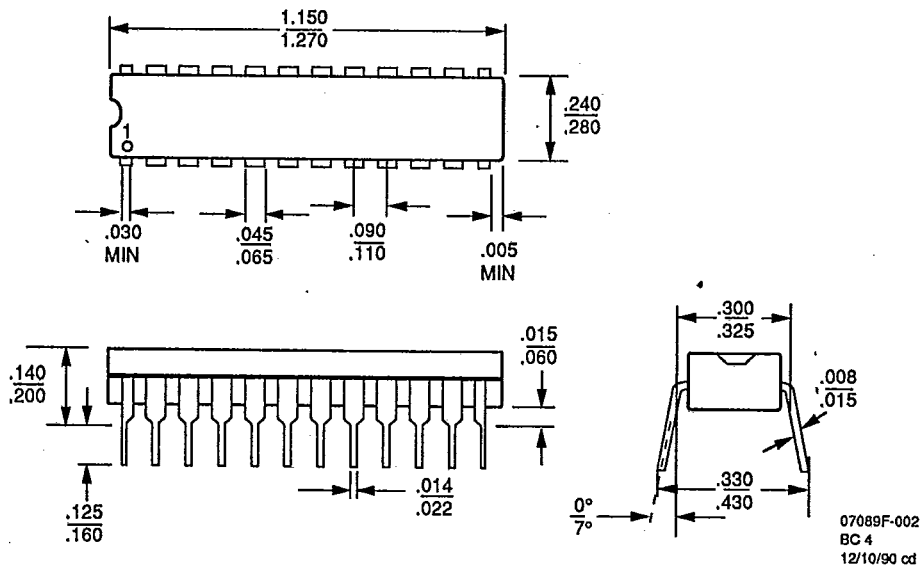


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**PD3024**  
**24-Pin 300-mil Plastic SKINNYDIP**

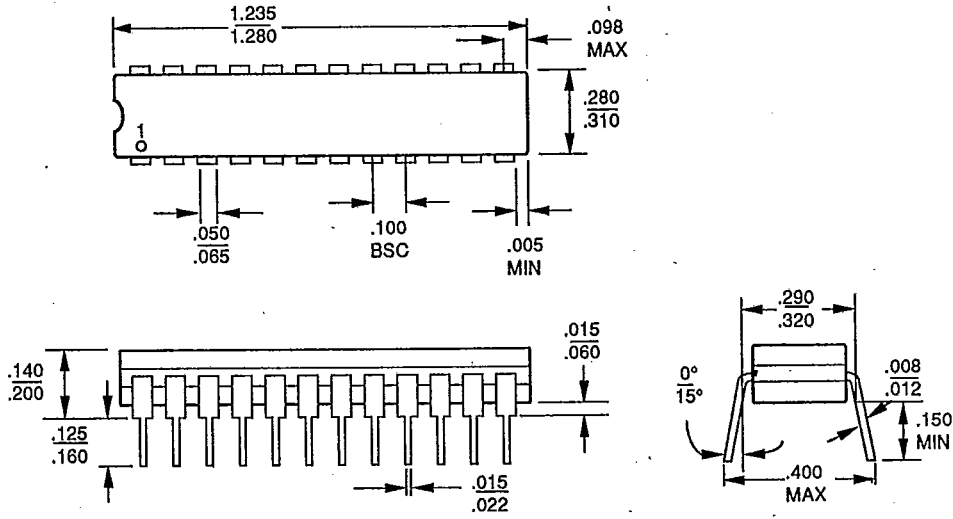
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**Note:**  
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

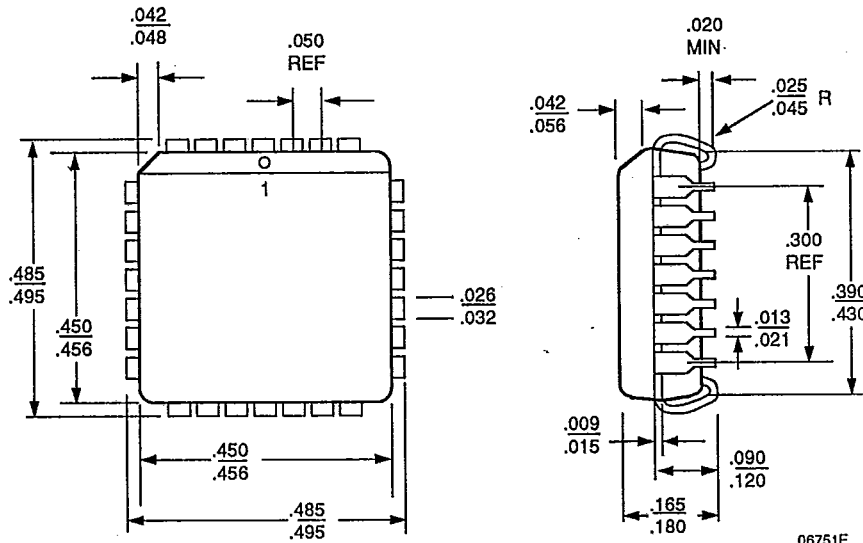
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**CD3024**  
**24-Pin 300-mil Ceramic SKINNYDIP**



06850C

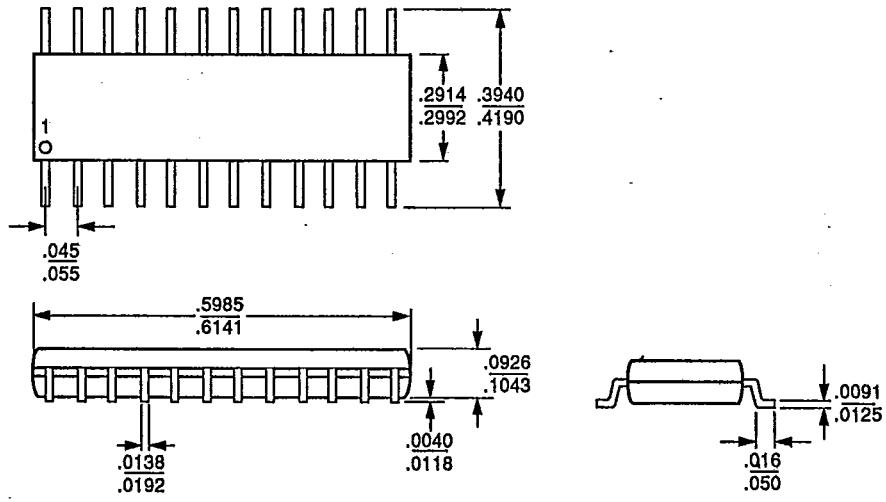
**PL 028**  
**28-Pin Plastic Leaded Chip Carrier**



06751E

**SO 024**  
**24-Pin Plastic Small Outline Package**

T-90-20



09310B