



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT16245T/AT/CT/ET
IDT54/74FCT162245T/AT/CT/ET
IDT54/74FCT166245T/AT/CT
IDT54/74FCT162H245T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
- **Features for FCT16245T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C
- **Features for FCT162245T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

DESCRIPTION:

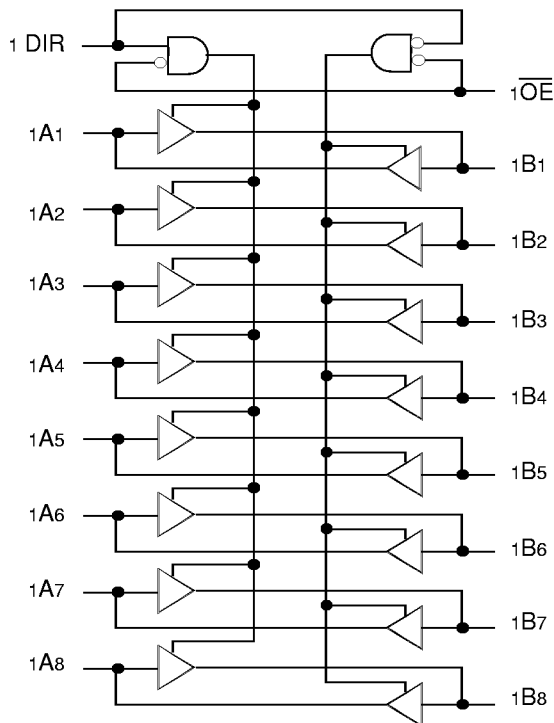
The 16-bit transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin (xOE) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT16245T are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

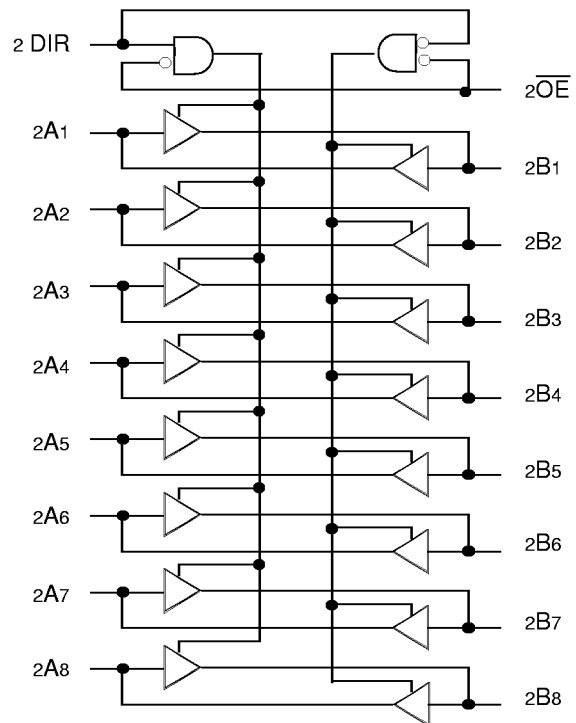
The FCT162245T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162245T are plug-in replacements for the FCT16245T and ABT16245 for on-board interface applications.

The FCT166245T are suited for very low noise, point-to-point driving where there is a single receiver, or a light lumped

FUNCTIONAL BLOCK DIAGRAM



2545 drw 01



2545 drw 02

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MILITARY AND INDUSTRIAL TEMPERATURE RANGES

FEBRUARY 1997

FEATURES: (Cont'd.)

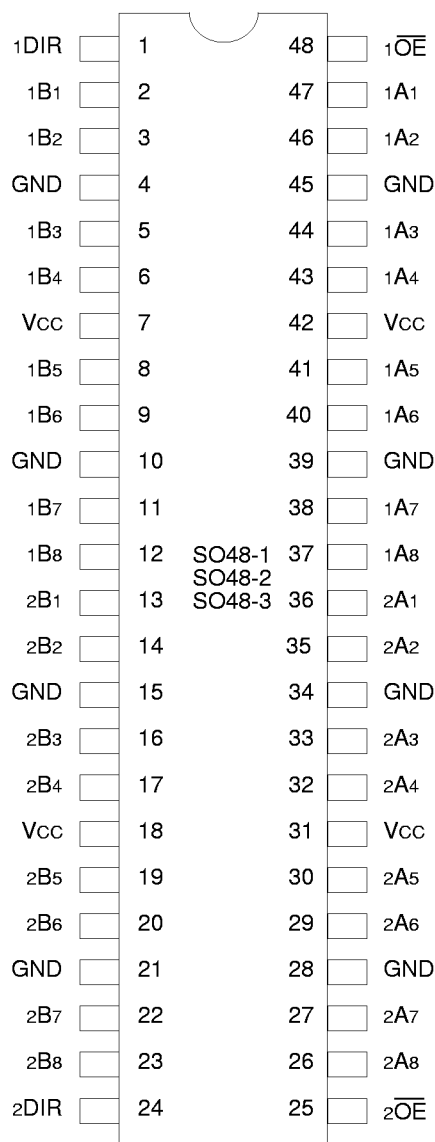
- **Features for FCT166245T/AT/CT:**
 - Light Drive A Port: $\pm 8\text{mA}$ (commercial), $\pm 6\text{mA}$ (military)
 - High Drive B Port: $+64\text{mA}$, -32mA (commercial), $+48\text{mA}$, -24mA (military)
 - Minimal system switching noise
 - Typical VOLP (Output Ground Bounce) $< 0.25\text{V}$ at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$ (A Port Switching)
- **Features for FCT162H245T/AT/CT/ET:**
 - Bus Hold retains last active bus state during 3-state
 - Eliminates the need for external pull up resistors

DESCRIPTION: (Cont'd.)

load ($< 100\text{pF}$). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors. These parts have a $\pm 8\text{mA}$ driver on the "A" Port and a $+64/-32\text{mA}$ driver on the "B" Port, making them ideal for interfacing noisy system busses to noise sensitive interfaces.

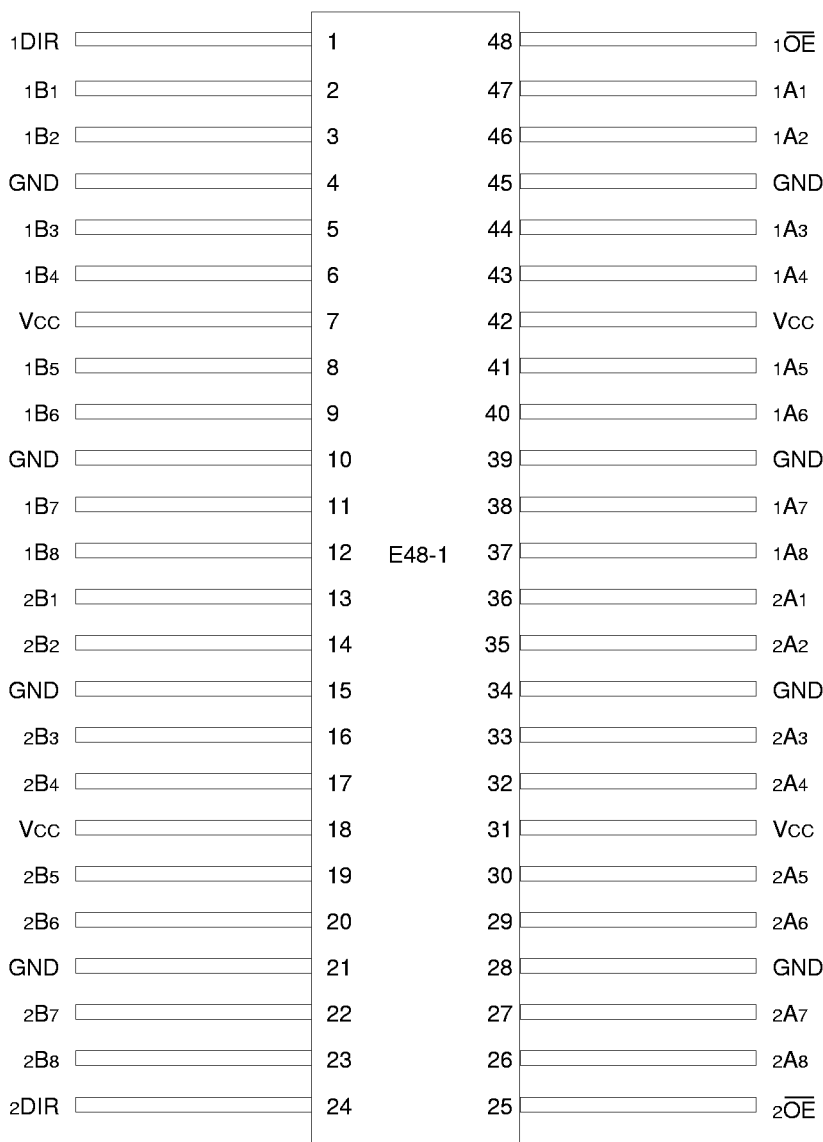
The FCT162H245T have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

PIN CONFIGURATIONS



**SSOP/
TSSOP/TVSOP
TOP VIEW**

2545 drw 03



**CERPACK
TOP VIEW**

2545 drw 04

PIN DESCRIPTION

Pin Names	Description
\overline{xOE}	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs ^(1,2)
xBx	Side B Inputs or 3-State Outputs ^(1,3)

NOTES:

2545 tbl 01

- On FCT162H245T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.
- On FCT166245T this is the ± 8 mA Port.
- On FCT166245T this is the +64/-32mA Port.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

2545 lnk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT and FCT166XXXT (A-Port) Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT and FCT166XXXT (A-Port).

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
\overline{xOE}	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2545 tbl 02

NOTE:

- H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

2545 lnk 04

NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-250	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

2545 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16245T AND FCT166245T (B-PORT)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.5	3.5	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.5	—	V
			I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
			I _{OL} = 48mA MIL. I _{OL} = 64mA COM'L.	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

2545 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162245T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	200	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

2545 Ink 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT166245T (A-PORT ONLY)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		16	48	96	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-16	-48	-96	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 6mA MIL. I _{OL} = 8mA COM'L.	—	0.3	0.55	V

2545 Ink 08

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ±5μA at T_A = -55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
		Standard I/O ⁽⁵⁾			—	—	± 1	
		Bus-hold Input			—	—	± 100	
		Bus-hold I/O			—	—	± 100	
I_{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	
		Standard I/O ⁽⁵⁾			—	—	± 1	
		Bus-hold Input			—	—	± 100	
		Bus-hold I/O			—	—	± 100	
I_{BHH}	Bus Hold Sustain Current ⁽⁴⁾	Bus-hold Input	$V_{CC} = \text{Min.}$	$V_I = 2.0\text{V}$	-50	—	—	μA
I_{BHL}				$V_I = 0.8\text{V}$	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins) ^(5,6)		$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}				$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage		$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current		$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

2545 Ink 09

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Pins with Bus Hold are identified in the pin description.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
- Does not include Bus Hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16245T/162245T ⁽⁵⁾				FCT16245AT/162245AT ⁽⁵⁾				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
tPHL	A to B, B to A										
tPZH	Output Enable Time		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPZL	x $\overline{O}E$ to A or B										
tPHZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
tPLZ	x $\overline{O}E$ to A or B										
tPZH	Output Enable Time		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPZL	xDIR to A or B ⁽⁴⁾										
tPHZ	Output Disable Time	1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns	
tPLZ	xDIR to A or B ⁽⁴⁾										
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

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Symbol	Parameter	Condition ⁽¹⁾	FCT16245CT/162245CT ⁽⁵⁾				FCT16245ET/162245ET ⁽⁵⁾				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	4.1	1.5	4.5	1.5	3.2	—	—	ns
tPHL	A to B, B to A										
tPZH	Output Enable Time		1.5	5.8	1.5	6.2	1.5	4.4	—	—	ns
tPZL	x $\overline{O}E$ to A or B										
tPHZ	Output Disable Time		1.5	4.8	1.5	5.2	1.5	4.0	—	—	ns
tPLZ	x $\overline{O}E$ to A or B										
tPZH	Output Enable Time		1.5	5.8	1.5	6.2	1.5	4.8	—	—	ns
tPZL	xDIR to A or B ⁽⁴⁾										
tPHZ	Output Disable Time	1.5	4.8	1.5	5.2	1.5	4.0	—	—	ns	
tPLZ	xDIR to A or B ⁽⁴⁾										
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

2545 tbl 12

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.
5. Including parts with Bus Hold.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT166245T				FCT166245AT				FCT166245CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay A to B	CL = 50pF RL = 500Ω	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5					ns
tPLH tPHL	Propagation Delay B to A		1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9					ns
tPZH tPZL	Output Enable Time xOE to B		1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2					ns
tPZH tPZL	Output Enable Time xOE to A		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5					ns
tPHZ tPLZ	Output Disable Time xOE to B		1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2					ns
tPHZ tPLZ	Output Disable Time xOE to A		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0					ns
tPZH tPZL	Output Enable Time xDIR to B ⁽⁴⁾		1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2					ns
tPZH tPZL	Output Enable Time xDIR to A ⁽⁴⁾		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5					ns
tPHZ tPLZ	Output Disable Time xDIR to B ⁽⁴⁾		1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2					ns
tPHZ tPLZ	Output Disable Time xDIR to A ⁽⁴⁾		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0					ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5					ns

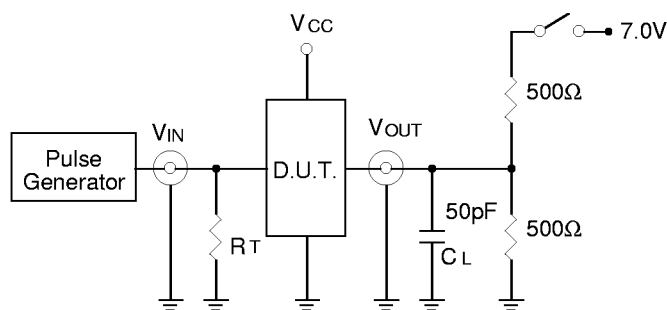
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

2545 tbl 13

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2545 drw 05

SWITCH POSITION

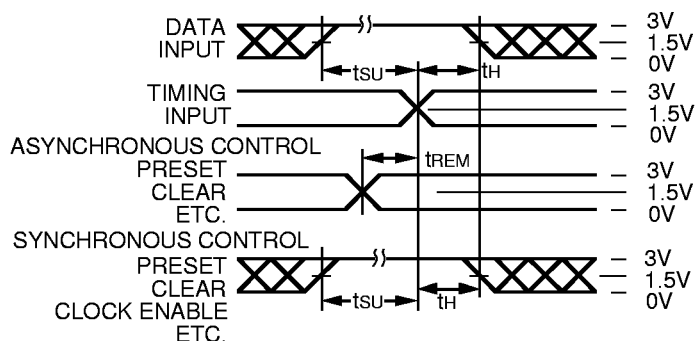
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

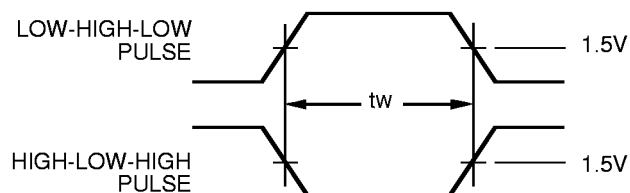
2545 Ink 14

SET-UP, HOLD AND RELEASE TIMES



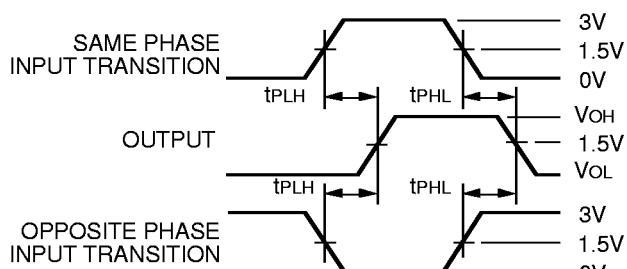
2545 drw 06

PULSE WIDTH



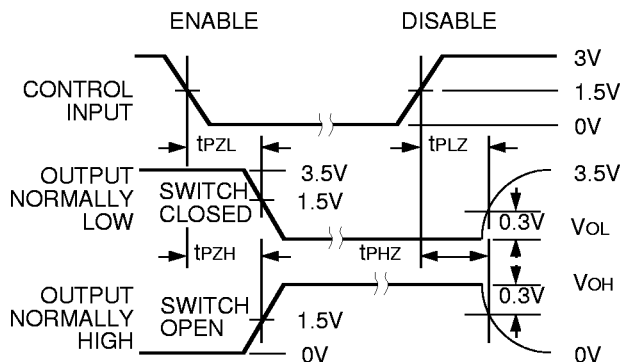
2545 drw 07

PROPAGATION DELAY



2545 drw 08

ENABLE AND DISABLE TIMES



2545 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	X	X	XXXX	X	X	
Temp. Range	Drive	Bus Hold	Device Type	Package	Process			
							Blank B	Commercial MIL-STD-883, Class B
							PV PA PF E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package (SO48-2) Thin Very Small Outline Package (SO48-3) CERPACK (E48-1)
							245T 245AT 245CT 245ET	Non-Inverting 16-Bit Bidirectional Transceiver
							Blank H	Standard Bus Hold
							16 162 166	16-Bit High Drive 16-Bit Balanced Drive 16-Bit Light Drive
							54 74	-55°C to +125°C -40°C to +85°C

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