Am29833A/834A – Am29853A/854A

Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceiver for processor organized devices
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- Buffered direction three-state control
- Output short-circuit protected to V_{CC} limits
- 200-mV minimum input hysteresis on input data ports
- High drive capability:
  - 48 mA Commercial I_{OL}
  - 32 mA Military I_{OL}
- Higher speed, lower power versions of the Am29833/834 & Am29853/854

GENERAL DESCRIPTION

The Am29833A/834A and Am29853A/854A are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator.

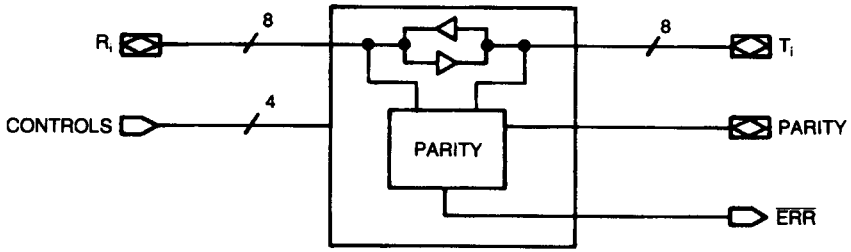
Two options are available: the Am29833A/834A register option, and the Am29853A/854A latch option. With the register option, the error flag can be clocked and stored in a register and read at the open-collector $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

The output enables $\overline{OET}$ and $\overline{OER}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, the $\overline{OER}$ and $\overline{OET}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29833A and Am29853A are noninverting, while the Am29834A and Am29854A present inverting data at the outputs. The devices are specified at 48 mA output sink current over the commercial range and 32 mA over the military range.

SIMPLIFIED BLOCK DIAGRAM

Parity Transceivers



BD005541

PRODUCT SELECTOR GUIDE

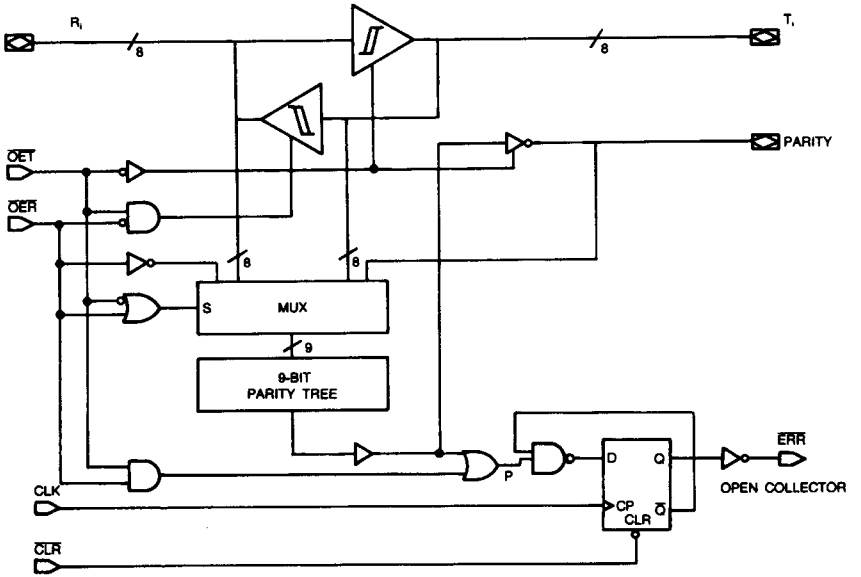
	Error Flag Logic	
	Register	Latch
Noninverting	Am29833A	Am29853A
Inverting	Am29834A	Am29854A

October 1985

Order # 07140A

BLOCK DIAGRAMS*

Am29833A



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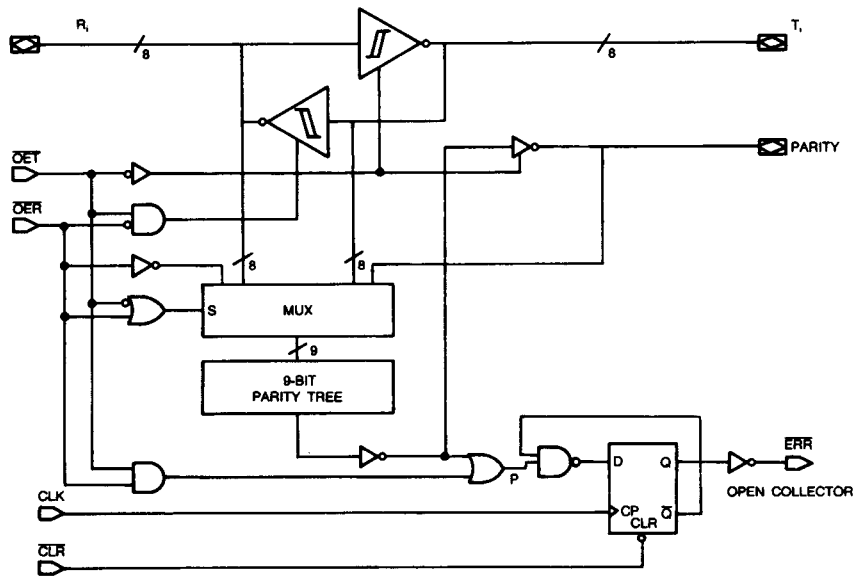
Am29834A



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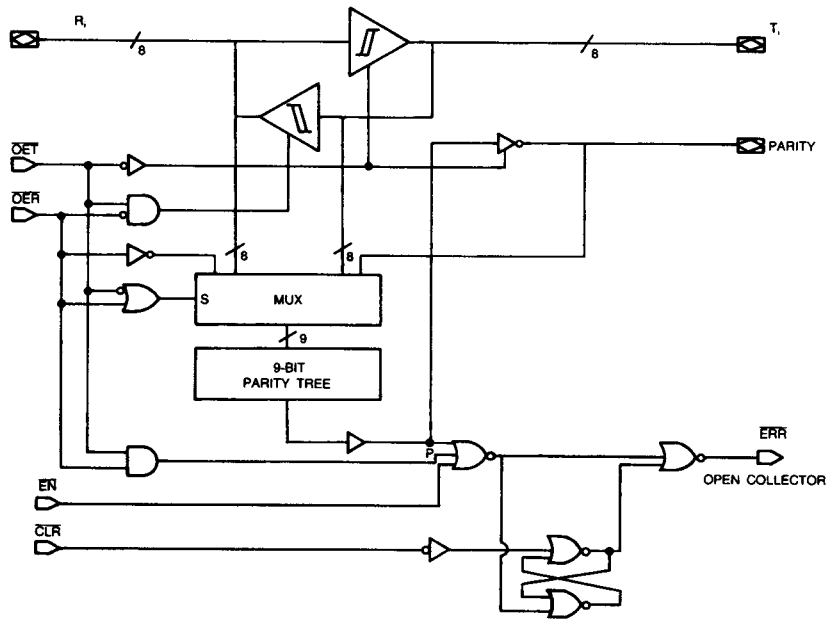
*See following page for additional Block Diagrams.

BLOCK DIAGRAMS (Cont.)

Am29853A



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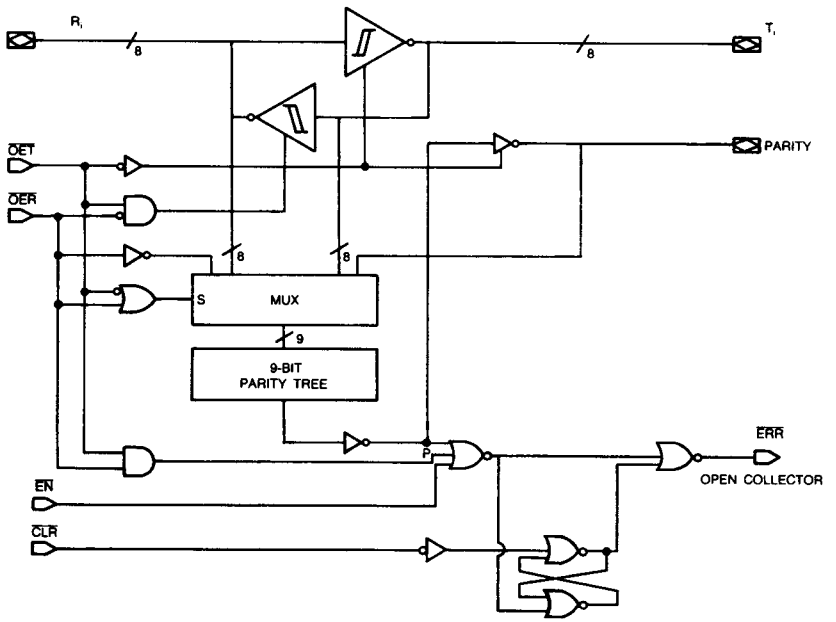
Am29854A



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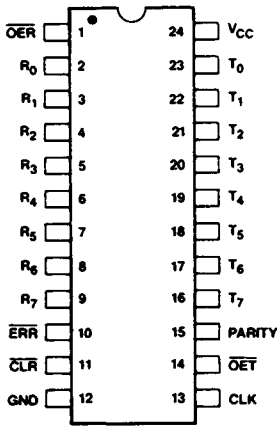
CONNECTION DIAGRAMS
Top View

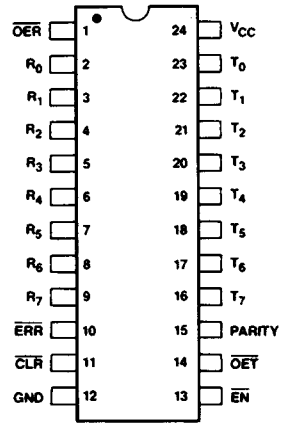
DIPs

Am29833A/834A



CD001120

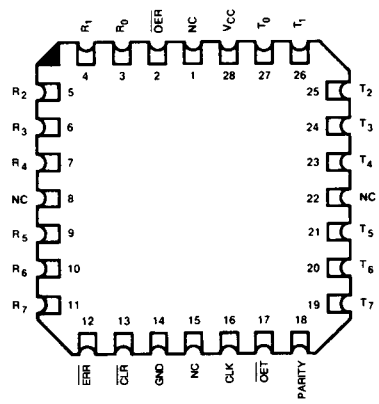
Am29853A/854A



CD001130

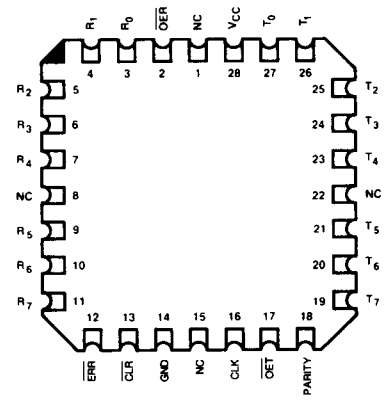
LCC*

Am29833A/834A



CD001395

Am29853A/854A



CD001394

*Same Pinouts apply for PLCC

FUNCTION TABLES

Am29833A (Register Option, Noninverting)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Σ of H's of R_i	T_i	Σ of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled
H	H	L	X	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

Am29834A (Register Option, Inverting)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Σ of H's of R_i	T_i	Σ of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	L	H	*	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	X	X	H	EVEN	NA	NA	NA	L	L	*	
L	H	X	X	L	ODD	NA	NA	NA	H	H	*	
L	H	X	X	L	EVEN	NA	NA	NA	H	L	*	
H	L	H	↑	NA	NA	H	ODD	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	NA	H	EVEN	L	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	H	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	H	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled
H	H	L	X	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	L	L	*	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	L	H	*	
L	L	X	X	L	ODD	NA	NA	NA	H	L	*	
L	L	X	X	L	EVEN	NA	NA	NA	H	H	*	

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
X = Don't Care
Z = High impedance
NA = Not applicable
* = Store the Error state of the last Receive cycle
Odd = Odd number
Even = Even number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE

Error Flag Output

Am29833A/834A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FUNCTION TABLES (Cont.)

Am29853A (Latch Option, Noninverting)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	EN	R_i	Σ of H's of R_i	T_i	Σ of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

Am29854A (Latch Option, Inverting)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Σ of H's of R_i	T_i	Σ of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	L	H	*	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	X	X	H	EVEN	NA	NA	NA	L	L	*	
L	H	X	X	L	ODD	NA	NA	NA	H	H	*	
L	H	X	X	L	EVEN	NA	NA	NA	H	L	*	
H	L	L	L	NA	NA	H	ODD	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	NA	H	EVEN	L	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	H	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	L	NA	NA	*	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	NA	H	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	H	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	H	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	L	L	*	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	L	H	*	
L	L	X	X	L	ODD	NA	NA	NA	H	L	*	
L	L	X	X	L	EVEN	NA	NA	NA	H	H	*	

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
X = Don't Care

Z = High impedance
NA = Not applicable
* = Store the Error state of the last Receive cycle

Odd = Odd number
Even = Even number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE
Error Flag Output

Am29853A/854A

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's Capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
AMD STANDARD PRODUCTS

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

Am29833A — P — C — B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
M = Military* (−55 to +125°C)

C. PACKAGE TYPE
P = 24-Pin (Slim) Plastic DIP (PD3024)
D = 24-Pin (Slim) Ceramic DIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028**)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)
X = Dice

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29833A Parity Bus Transceiver (Noninverting-Register Option)
Am29834A Parity Bus Transceiver (Inverting-Register Option)
Am29853A Parity Bus Transceiver (Noninverting-Latch Option)
Am29854A Parity Bus Transceiver (Inverting-Latch Option)

* Military or Limited Military temperature range products are "NPL" (Non-Compliant Product List), or Non-MIL-STD-883C Compliant products only.

** Preliminary. Subject to Change.

Valid Combinations	
Am29833A/834A and Am29853A/854A	PC, PCB, DC, DCB, DM, DMB, JC**, JCB**, LC, LCB, LM, LMB, XC, XM

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Am29833A/Am29834A, Am29853A/Am29854A

$\overline{OER}$ Output Receive Enable (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$ Output Transmit Enable (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i Receive Port (Input/Output, Three-State)
R_i are the 8-bit data inputs in the Transmit mode, and the inputs in the Receive mode.

T_i Transmit Port (Input/Output, Three-State)
T_i are the 8-bit data outputs in the Transmit mode, and the outputs in the Receive mode.

Parity Parity Flag (Input/Output, Three-State)
In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29833A, Am29834A Only

$\overline{ERR}$ Error Flag (Output, Open Collector)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK Clock (Input, Positive Edge-Triggered)
This pin is the clock input for the Error Flag register.

Am29853A, Am29854A Only

$\overline{ERR}$ Error Flag (Output, Open Collector)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW and $\overline{EN}$ is HIGH, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$ Latch Enable (Input, Active LOW)
This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Output
for High Output State ..... −0.5 V to +5.5 V
DC Input Voltage ..... −0.5 V to +5.5 V
DC Output Current, into Outputs ..... 100 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15 mA	2.4		V
				I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	$\overline{ERR}$	I_{OL} = 48 mA		0.5	V
			All Other Outputs V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32 mA MIL		0.5	
				I_{OL} = 48 mA COM'L		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i	Output Connected to AC Test Load Circuit			200		mV
I_{ZL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V				−550	μA
I_{ZH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				100	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V				150	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)			−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V				100	μA
I_{CC}	Power Supply Current	V_{CC} = Max. (All Outputs Are Open)		Over Temperature Range		180	mA
				+70°C			
				+125°C			

Notes: 1. Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditions*	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		10		14	ns
t_{PHL}					10		14	ns
t_{PLH}	Propagation Delay R_i to Parity				15		20	ns
t_{PHL}					15		20	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i				12		16	ns
t_{ZL}					12		16	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i				12		16	ns
t_{LZ}					12		16	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			12		16		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		0		ns
t_S	Clear ($\overline{CLR}$ ↓) to CLK Setup Time (Note 2)				15		20	ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		7		9.5		ns
t_{PWL}		LOW		7		9.5		ns
t_{PWL}	Clear Pulse Width	LOW		7		9.5		
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				12		16	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				12		16	ns
t_{PLH}	Propagation-Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29853A/854A				20		27	ns
t_{PHL}					15		20	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				15		20	ns
t_{PHL}					15		20	ns

*See test circuit and waveforms.

Notes: 1. For Am29853A/54A, replace CLK with $\overline{EN}$.
2. Not applicable to Am29853A/54A.