

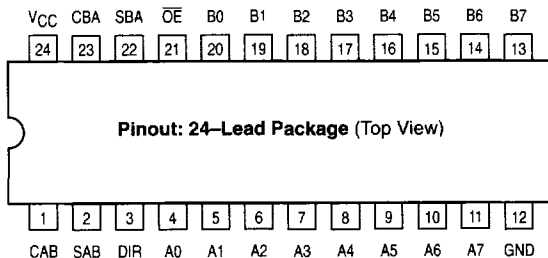
# Low-Voltage CMOS Octal Transceiver/Registered Transceiver

## With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX646 is a high performance, non-inverting octal transceiver/registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX646 inputs to be safely driven from 5V devices. The MC74LCX646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW-to-HIGH logic level. Output Enable ( $\overline{OE}$ ) and DIR pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when the enable  $\overline{OE}$  is active LOW. In the isolation mode ( $\overline{OE}$  HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

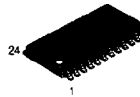
- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



**MC74LCX646**

**LCX**

**LOW-VOLTAGE CMOS  
OCTAL TRANSCEIVER/  
REGISTERED TRANSCEIVER**



**DW SUFFIX**  
PLASTIC SOIC  
CASE 751E-04



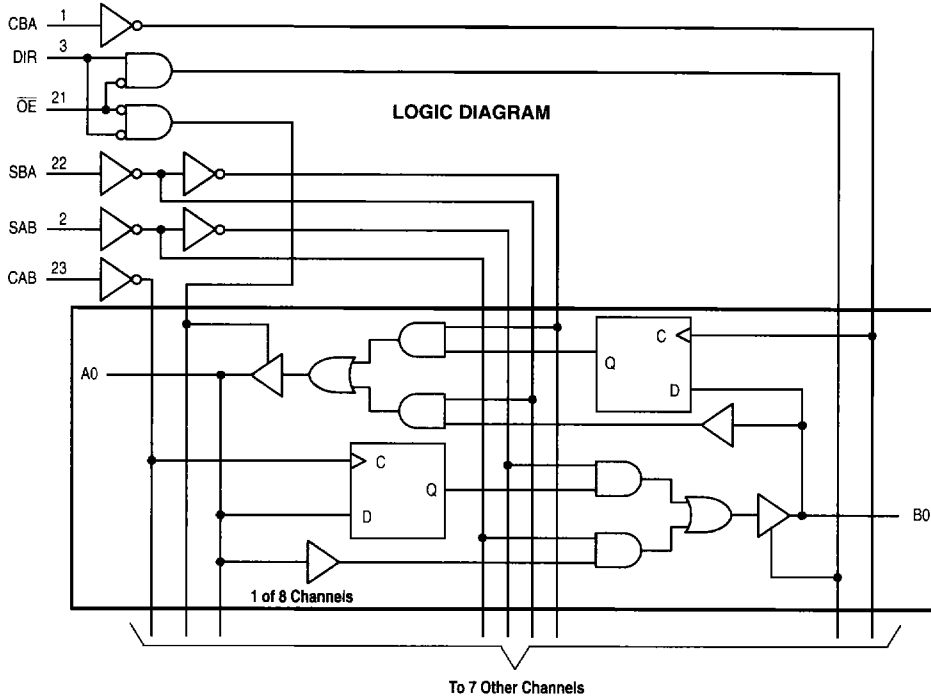
**SD SUFFIX**  
PLASTIC SSOP  
CASE 940D-03



**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948H-01

**PIN NAMES**

Pins	Function
A0-A7	Side A Inputs/Outputs
B0-B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
DIR, $\overline{OE}$	Output Enable Inputs



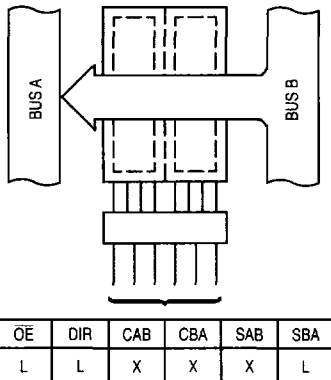
FUNCTION TABLE

		Inputs				Data Ports		Operating Mode
OE	DIR	CAB	CBA	SAB	SBA	An	Bn	
H	X					<b>Input</b>	<b>Input</b>	
		↑	↓	X	X	X	X	Isolation, Hold Storage
		↑	↑	X	X	l h X X	X l h	Store A and/or B Data
L	H					<b>Input</b>	<b>Output</b>	
		↑	X*	L	X	L H	L H	Real Time A Data to B Bus
				H	X	X	QA	Stored A Data to B Bus
		↑	X*	L	X	l h	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	QA QA	Clock A Data to B Bus; Store A Data
L	L					<b>Output</b>	<b>Input</b>	
		X*	↑	X	L	L H	L H	Real Time B Data to A Bus
				X	H	QB	X	Stored B Data to A Bus
		X*	↑	X	L	L H	l h	Real Time B Data to A Bus; Store B Data
				X	H	QB QB	L H	Clock B Data to A Bus; Store B Data

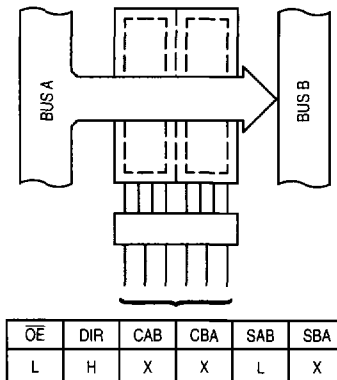
H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; X = Don't Care; ↑ = Low-to-High Clock Transition; ↓ = NOT Low-to-High Clock Transition; QA = A input storage register; QB = B input storage register; \* = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I<sub>CC</sub> reasons, Do Not Float Inputs.

BUS APPLICATIONS

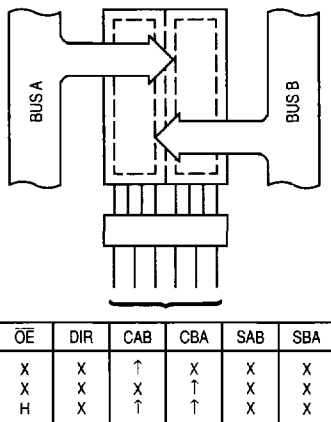
Real Time Transfer – Bus B to Bus A



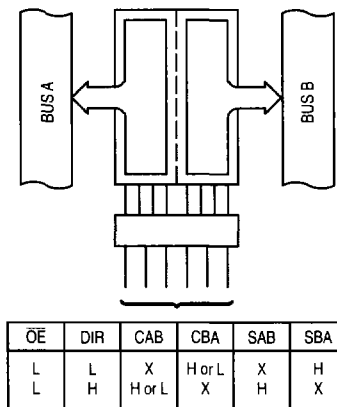
Real Time Transfer – Bus A to Bus B



Store Data from Bus A, Bus B or Busses A and B



Transfer Storage Data to Bus A or Bus B



## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V	
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub>	V	
		0		5.5		
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA	
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA	
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C	
ΔV/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V	

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

# MC74LCX646

## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>O</sub> ≤ 5.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V		±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

## AC CHARACTERISTICS (t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T <sub>A</sub> = -40°C to +85°C				
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.7V		
			Min	Max	Min	Max	
f <sub>max</sub>	Clock Pulse Frequency	3	150				MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 7.0	1.5 7.0	1.5 8.0	1.5 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output	3	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Select to Output	1	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	ns
t <sub>s</sub>	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t <sub>w</sub>	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

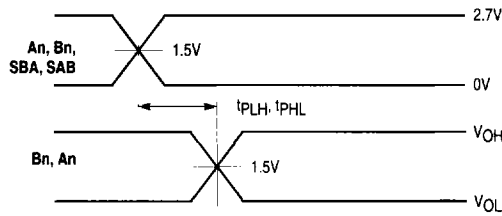
## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4.)	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V		0.8		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4.)	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V		0.8		V

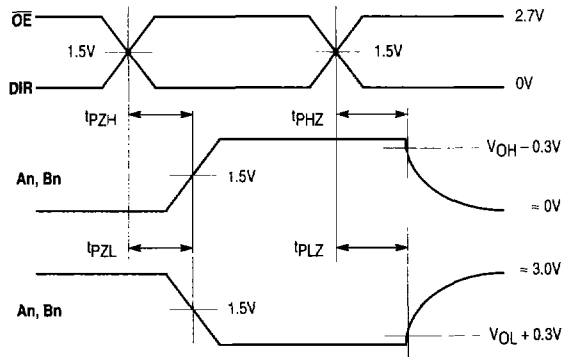
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	25	pF

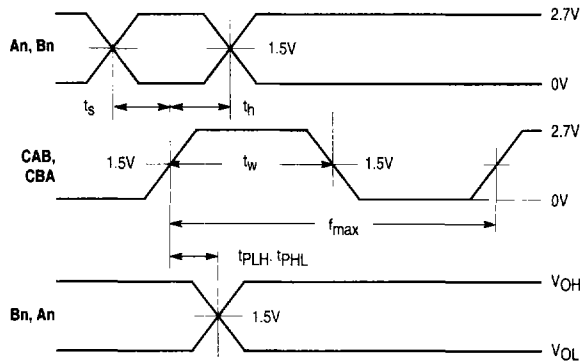


**WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS**  
 $t_p = t_f = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

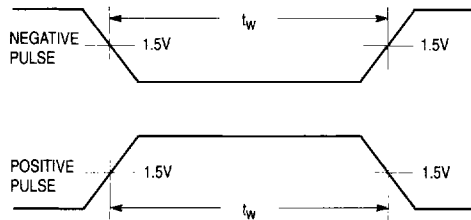


**WAVEFORM 2 – OE/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES**  
 $t_p = t_f = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 1. AC Waveforms**

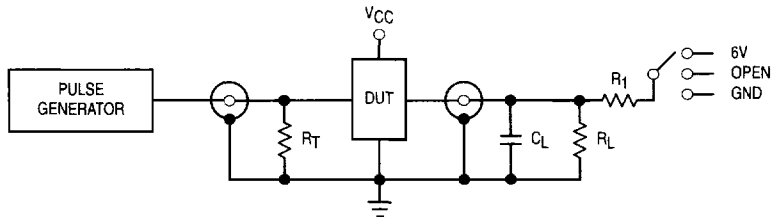


**WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5ns, 10\% \text{ to } 90\%; f = 1MHz; t_W = 500ns \text{ except when noted}$



**WAVEFORM 4 – INPUT PULSE DEFINITION**  
 $t_R = t_F = 2.5ns, 10\% \text{ to } 90\% \text{ of } 0V \text{ to } 2.7V$

**Figure 2. AC Waveforms**



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}, t_{PHZ}$	GND

$C_L = 50pF$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 3. Test Circuit**