Am2917A

Quad Three-State Bus Transceiver with Interface Logic

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- D-type driver register with tri-state bus driver output can sink 48mA at 0.5V max.
- Internal 4-bit odd parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

GENERAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

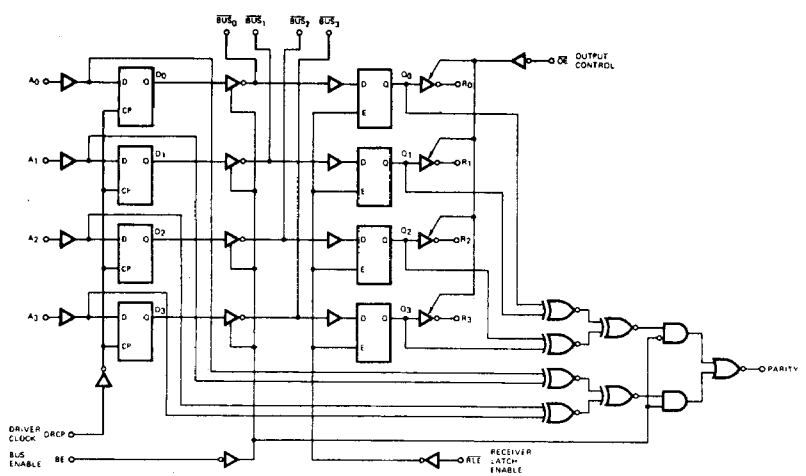
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

BLOCK DIAGRAM



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CONNECTION DIAGRAM
Top View

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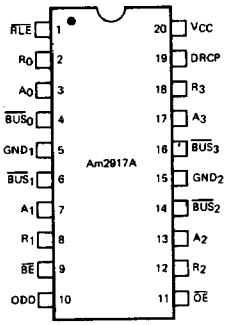

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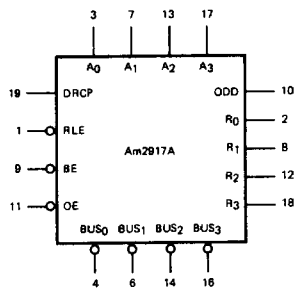
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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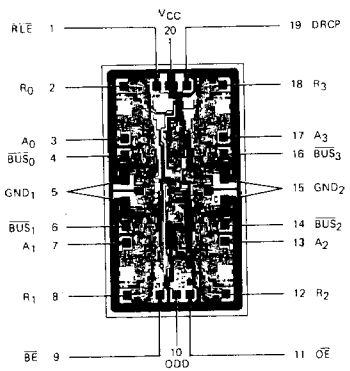
METALLIZATION AND PAD LAYOUT



DIE SIZE .074" x .130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2917A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice
- **Am2917A** — Device type
  - Quad 3-state Bus Transceiver

Valid Combinations	
Am2917A	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7 13, 17	A_0, A_1, A_2, A_3	I	The four driver register inputs.
19	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
9	$\overline{BE}$	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
4, 6, 14, 16	BUS_0, BUS_1, BUS_2, BUS_3	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 8, 12, 18	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.
1	$\overline{RLE}$	I	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
10	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.
11	$\overline{OE}$	I	Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	FUNCTION
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X X	X X	H H	L L	L L	X X	L H	L H	H L	Driver output disable and receive data via Bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L H	↑ ↑	X X	X X	X X	L H	X X	X X	X X	Load driver register
X X	L H	X X	X X	X X	NC NC	X X	X X	X X	No driver clock restrictions
X X	X X	L L	X X	X X	L H	X X	H L	X X	Drive Bus

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

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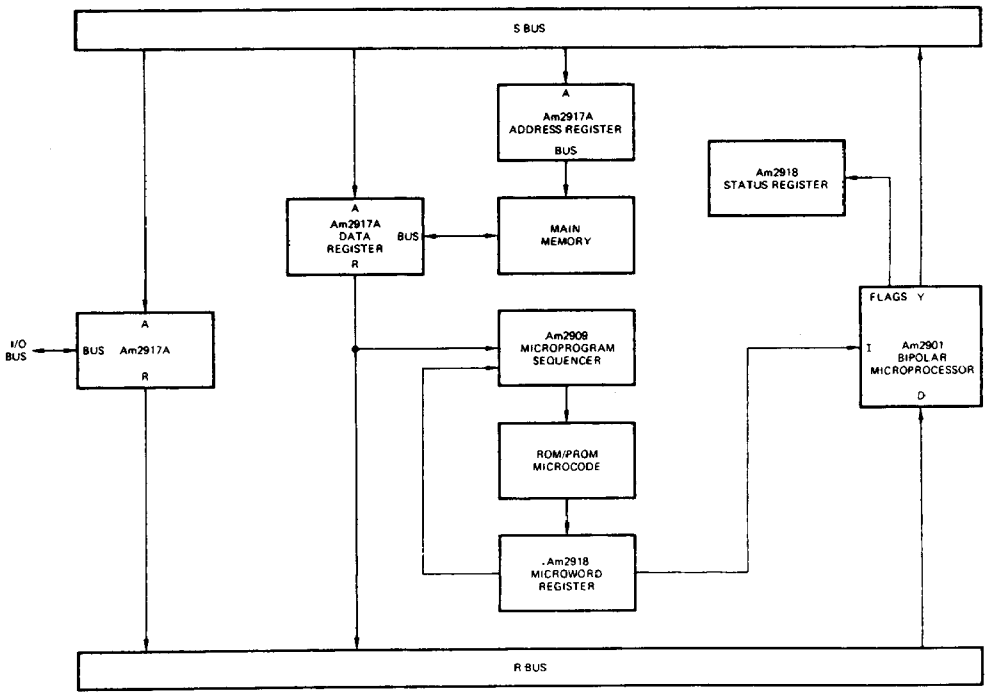
APPLICATIONS



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The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max.
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Bus 100mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100µA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660µA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{BE}$, $\overline{ALE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 7.0V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX	V_O = 2.4V			50	µA
			V_O = 0.4V			−50	

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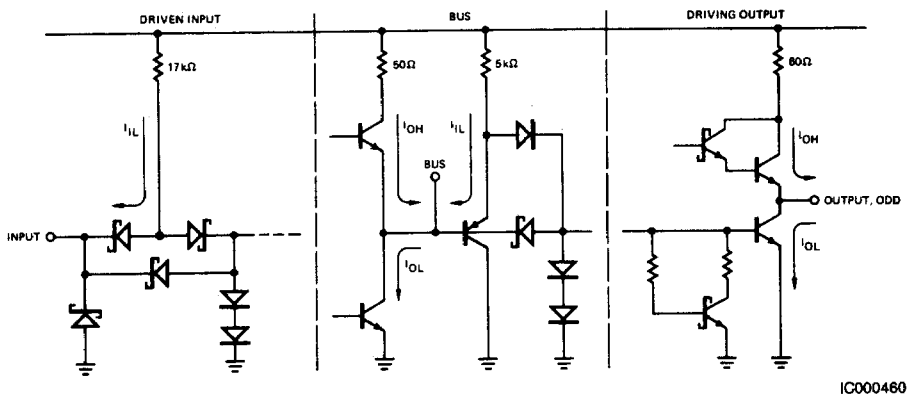
BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)		Min	Typ	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX V_O = 0V		−50	−120	−225	mA

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2917A Min.	COMMERCIAL Am2917A Typ (Note 1)	COMMERCIAL Am2917A Max.	MILITARY Am2917A Min.	MILITARY Am2917A Typ (Note 1)	MILITARY Am2917A Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF R_L (BUS) = 130 Ω		21	32		21	36	ns
t_{PLH}				21	32		21	36	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	23		13	26	ns
t_{HZ}, t_{LZ}				13	18		13	21	
t_s	A Data Inputs	C_L = 15 pF R_L = 2.0 kΩ	12			15			ns
t_h			6.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		17			20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	33	ns
t_{PHL}				18	27		18	30	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	33	ns
t_{PHL}				21	27		21	30	
t_s	Bus to Latch Enable ($\overline{RLE}$)		13			15			ns
t_h			4.0			6.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	42		32	46	ns
t_{PHL}				26	36		26	40	
t_{PLH}	Bus to Odd Party Out (Driver Inhibit)			21	32		21	36	ns
t_{PHL}				21	32		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	32		21	36	ns
t_{PHL}				21	32		21	36	
t_{ZH}, t_{ZL}	Output Control to Output			14	23		14	26	ns
t_{HZ}, t_{LZ}		C_L = 5 pF, R_L = 2.0 kΩ		14	23		14	26	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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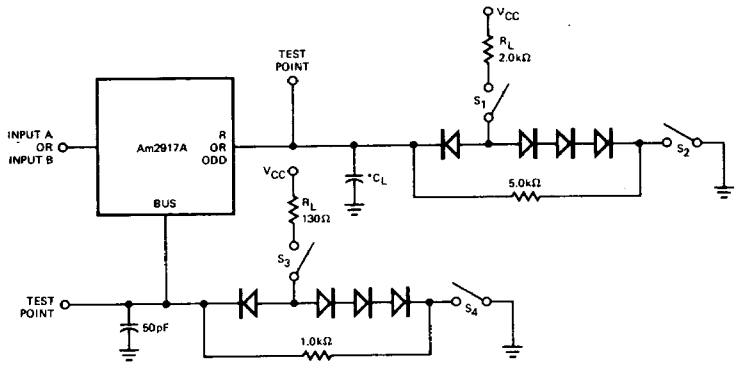
SWITCHING TEST CIRCUIT



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*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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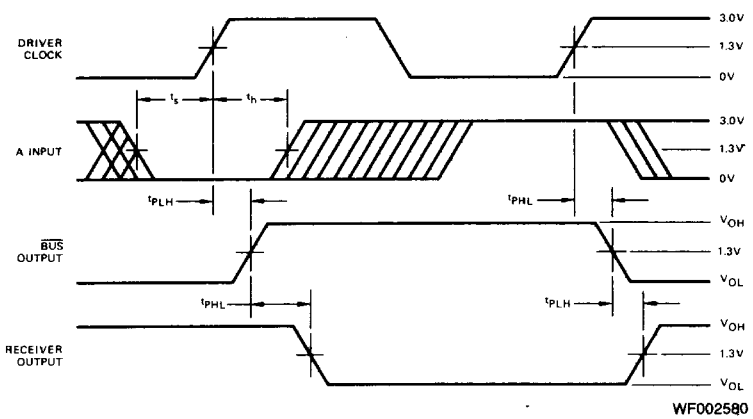
SWITCHING WAVEFORMS



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Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.