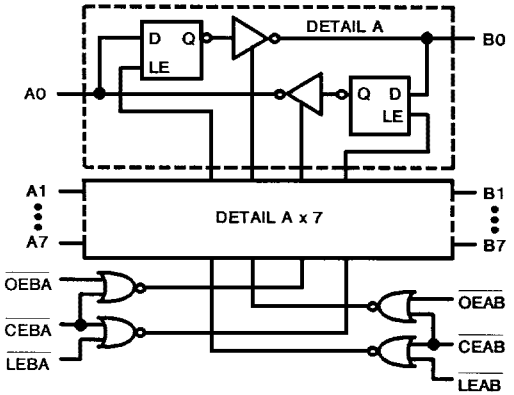
CD54/74FCT543, CD54/74FCT543AT
CD54/74FCT544, CD54/74FCT544AT

July 1990



CD54/74FCT543, 543AT FUNCTIONAL DIAGRAM

Octal Register-Transceivers, 3-State

CD54/74FCT543, CD54/74FCT543AT - Non-Inverting
CD54/74FCT544, CD54/74FCT544AT - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 4.1ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT543AT)*

The CD54/74FCT543, 543AT, 544, and 544AT 3-State octal register-transceviers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the outut of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

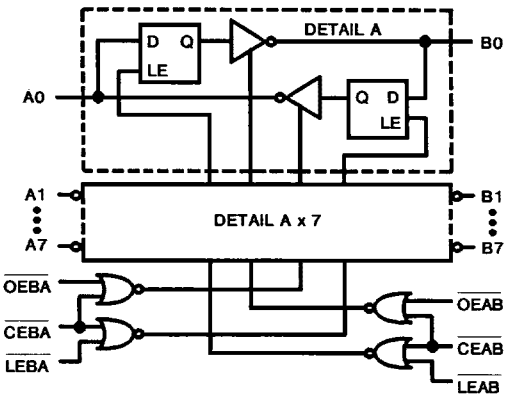
The CD54/74FCT543, 543AT, 544, and 544AT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT543 and 544 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX Types - Speed of bipolar FAST*/AS/S; FCTXXXAT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.



CD54/74FCT544, 544AT FUNCTIONAL DIAGRAM

File Number **2399**

TRUTH TABLE For A-to-B (Symmetric with B-to-A)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0-B7
H	X	X	Storing	High Z
X	H	-	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	V_{CC}	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

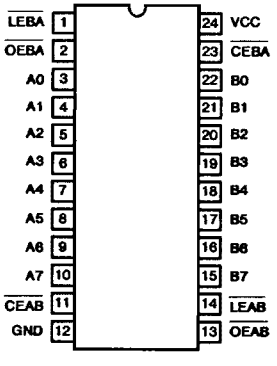
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-15	MIN	2.4	-	2.4	-	-	-	V
		VIL	-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

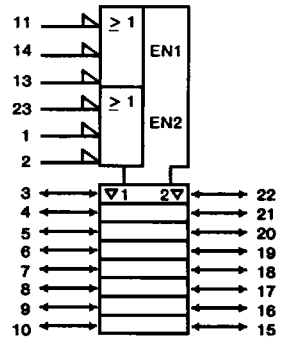
* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT543, CD54/74FCT543AT TYPES

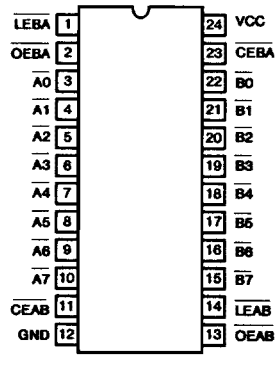


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT544, CD54/74FCT544AT TYPES



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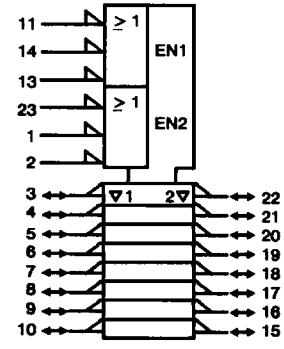


IEC LOGIC SYMBOL

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	VCC (V)	CD54/74FCT543, 544					CD54/74FCT543AT, 544AT*					UNITS
				AMBIENT TEMPERATURE (T_A)										
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
				TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Latch Enable Pulse Width	FCT543/AT	tW	5†		9	–	9	–		6	–	7	–	ns
	FCT544/AT	tW	5		7.5	–	9	–						ns
Data to Latch Enable Setup Time		tSU	5		3	–	3	–		2	–	2	–	ns
Data to Latch Enable Hold Time		tH	5		2	–	2	–		2	–	2	–	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL – See Figure 4

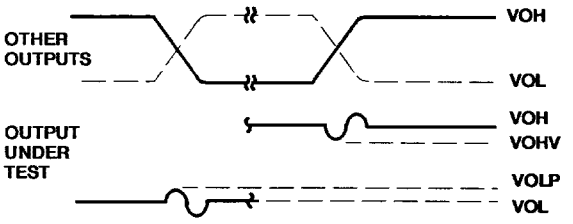
CHARACTERISTICS		SYMBOL	VCC (V)	CD54/74FCT543, 544					CD54/74FCT543AT, 544AT*					UNITS
				AMBIENT TEMPERATURE (T_A)										
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
				TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays: An ⟷ Bn	FCT543/AT	tPLH, tPHL	5†	6.4	2.5	8.5	2.5	10	4.1	2.5	6.5	2.5	7.5	ns
	FCT544/AT	tPLH, tPHL	5	7.9	3	10.5	3	12						ns
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	FCT543/AT	tPLH, tPHL	5	9.4	2.5	12.5	2.5	14	6.1	2.5	8	2.5	10.5	ns
	FCT544/AT	tPLH, tPHL	5	10.9	3	14.5	3	17						ns
$\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		tPLZ, tPHZ	5	6.8	2	9	2	13	4.8	2	7.5	2	8.5	ns
		tPZL, tPZH	5	9	2	12	2	14	5.9	2	9	2	10	ns
Power Dissipation Capacitance	FCT543/AT	CPD§	–	49 Typical					49 Typical					pF
	FCT544/AT	CPD§	–	58 Typical					58 Typical					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C										V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C										V
Input Capacitance		CI	–	–	–	10	–	10	–	–	10	–	10	pF
Input/Output Capacitance		$C_{I/O}$	–	–	–	15	–	15	–	–	15	–	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ is @ 5V

* Contact local Sales Office for availability

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

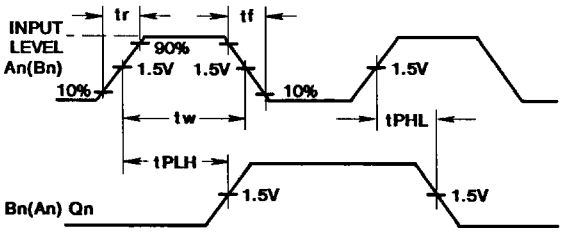


Figure 2 - CD54/74FCT543, 543AT propagation delay times.

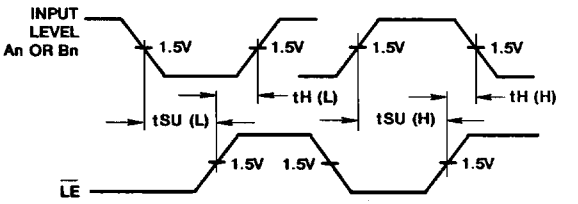
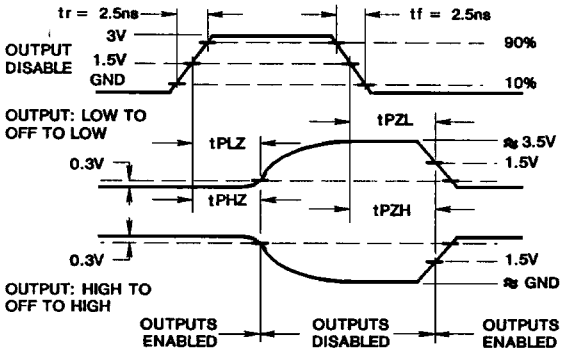
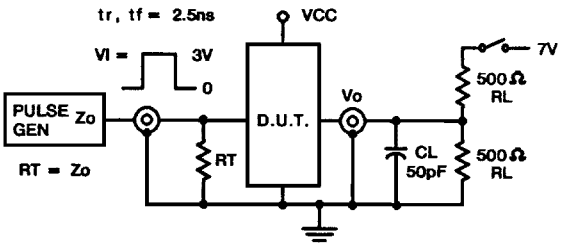


Figure 3 - CD54/74FCT543, 543AT setup and hold times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.