Am29C833/Am29C853/Am29C855
Am29C933/Am29C953/Am29C955

High-Performance CMOS Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 6 ns typical
  - R-Parity delay = 9 ns typical
- Error flag with open-drain output
- Generates odd parity for all-zero protection
- Low standby power
- Am29C855 adds new functionality
- 200-mV typical input hysteresis on input data ports
- I_{OL} = 24 mA, Commercial and Military
- JEDEC FCT-compatible specs
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

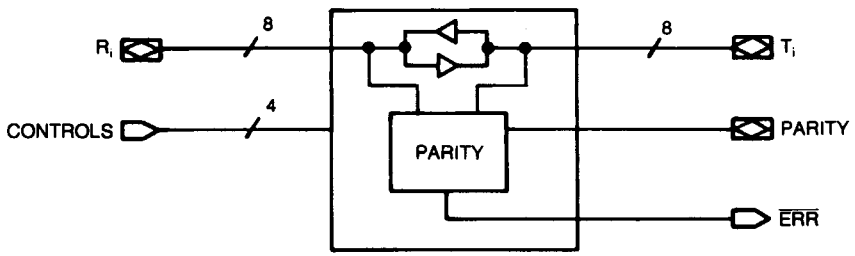
The Am29C833, Am29C853, and Am29C855 are high-performance CMOS parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with the $\overline{ERR}$ flag showing the results of the parity test. Each of these devices is produced with AMD's exclusive CS-11 CMOS process, and features a typical propagation delay of 6 ns, as well as an output current drive of 24 mA.

In the Am29C833, the error flag is clocked and stored in a register which is read at the open-drain $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29C853, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29C853 and Am29C833, parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port. The Am29C855, a variation of the Am29C853, is designed so that when both output enables are HIGH, the $\overline{ERR}$ pin retains its current state.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29C833, Am29C853, and Am29C855 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS parity transceivers with this pinout are the Am29C933, Am29C953, and Am29C955; their pinouts are shown later in this data sheet.

SIMPLIFIED BLOCK DIAGRAM



BD005541

Publication # 07323 | Rev. B | Amendment /0
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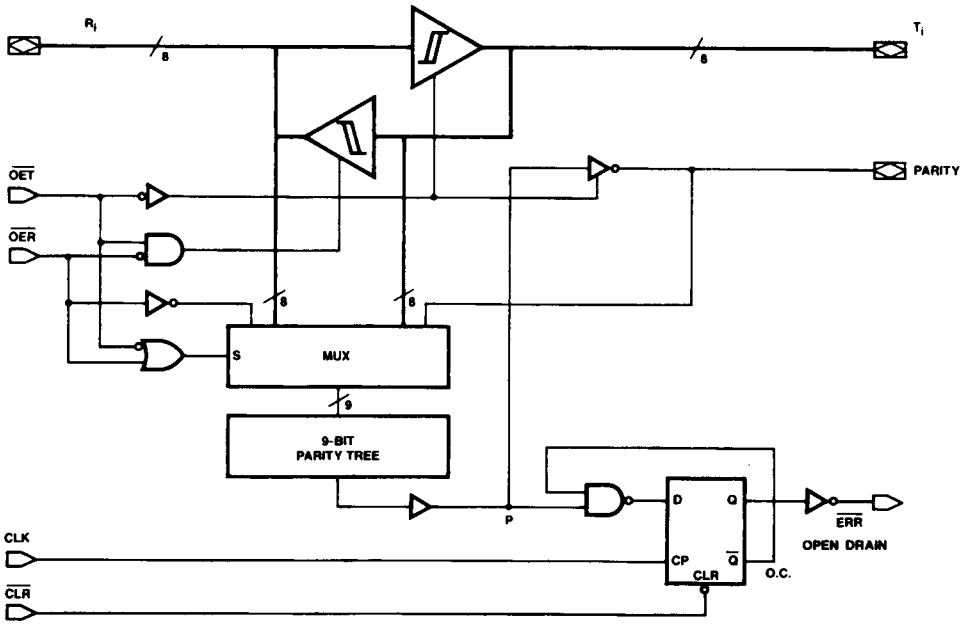
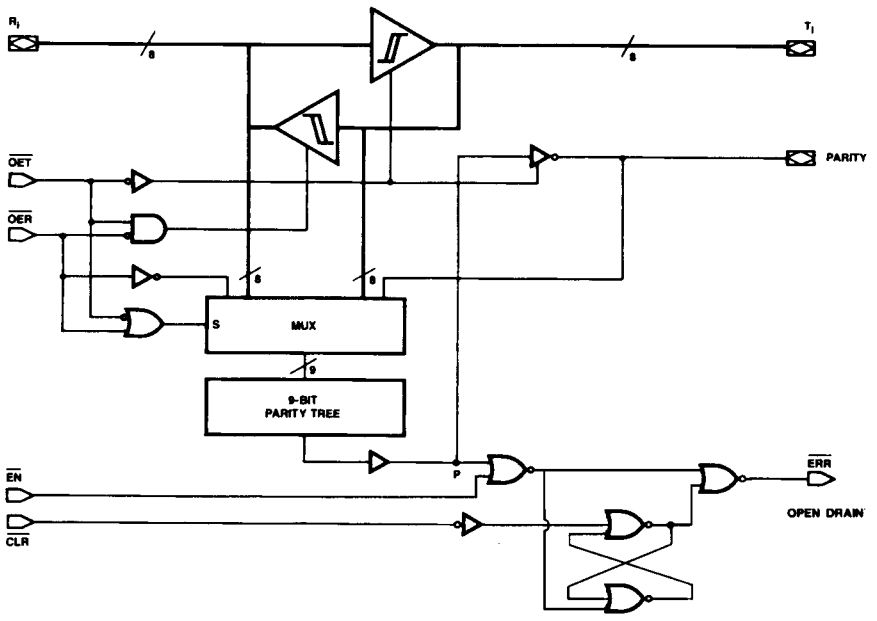
BLOCK DIAGRAMS*

Am29C833



BD001044

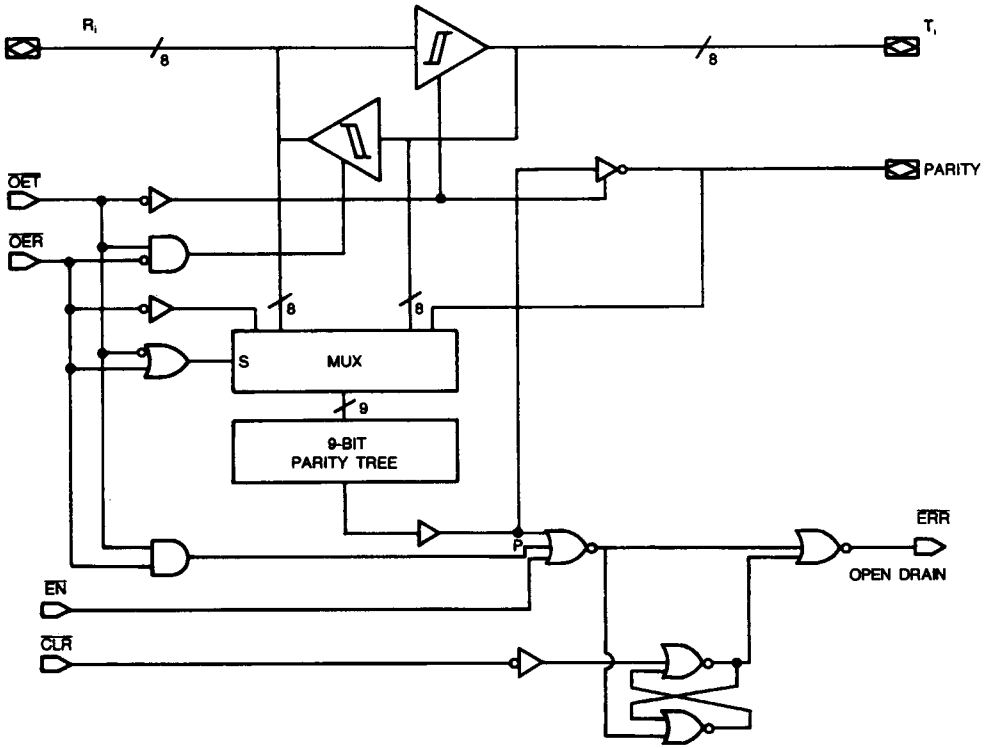
Am29C853



BD001035

BLOCK DIAGRAMS (Cont'd.)

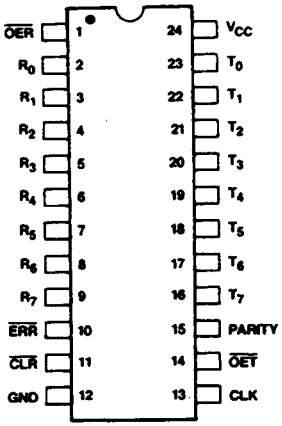
Am29C855



CONNECTION DIAGRAMS
Top View

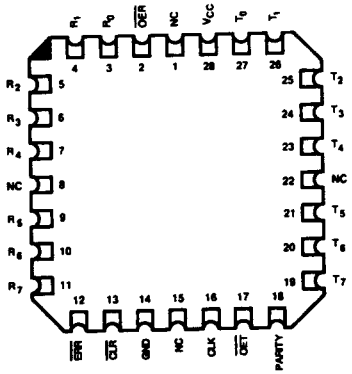
Am29C833

DIPs*



CD001120

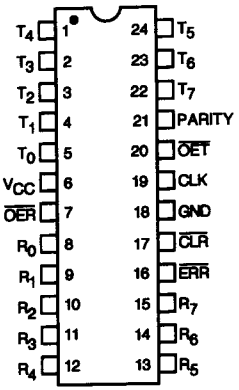
LCC**



CD001398

Am29C933

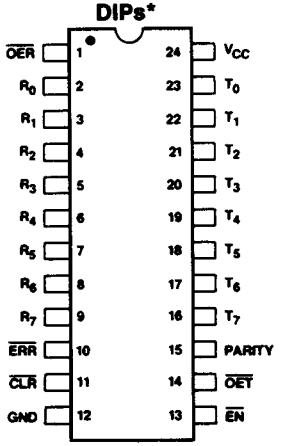
DIPs



CD010714

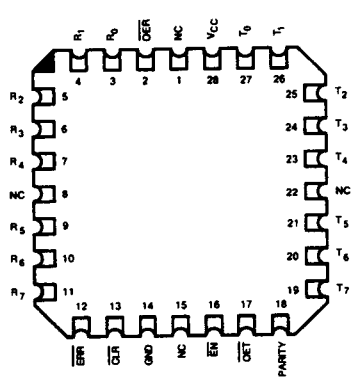
Am29C853/Am29C855

DIPs*



CD001130

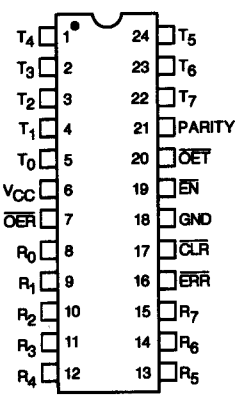
LCC**



CD001399

Am29C953/Am29C955

DIPs



CD010715

*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

FUNCTION TABLES

Am29C833 (Register Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_I	Sum of H's of R_I	T_I	Sum of H's (T_I + Parity)	R_I	T_I	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition of Clock
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE

Error Flag Output

Am29C833

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

FUNCTION TABLES (Cont'd.)

Am29C853 (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

Am29C855 (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of L's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	*	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	*	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = HIGH
L = LOW
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLE
Error Flag Output

Am29C853/Am29C855

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's Capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29C833 P C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (–55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C833 CMOS Parity Bus Transceiver — Register Option
Am29C853 CMOS Parity Bus Transceiver — Latch Option
Am29C855 CMOS Parity Bus Transceiver — Latch Option
Am29C933 CMOS Parity Bus Transceiver — Register Option (Center-V_{CC}-and-GND Pinout)
Am29C953 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)
Am29C955 CMOS Parity Bus Transceiver — Latch Option (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C833	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C853	
AM29C855	
AM29C933	PC, PCB, DC, DCB, DE
AM29C953	
AM29C955	

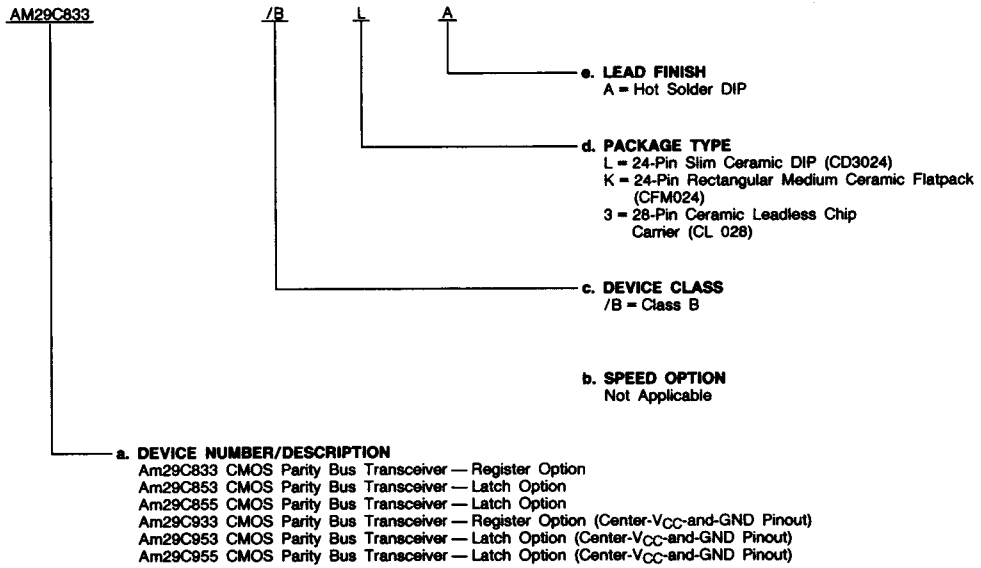
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C833	/BLA, /BKA, /B3A
AM29C853	
AM29C855	
AM29C933	/BLA
AM29C953	
AM29C955	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C833/Am29C853/Am29C855

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i Receive Port (Input/Output, Three-State)
R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output, Three-State)
T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity Parity Flag (Input/Output, Three-State)
In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29C833 Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK Clock (Input, Positive Edge-Triggered)
This pin is the clock input for the Error Flag register.

Am29C853/Am29C855 Only

$\overline{ERR}$ Error Flag (Output, Open Drain)
In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared. In the Am29C855, the error flag will retain its previous state when $\overline{OET}$ and $\overline{OER}$ are HIGH.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ goes LOW and $\overline{EN}$ is HIGH, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$ Latch Enable (Input, Active LOW)
This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +48 mA (2 x I_{OL})
I_{SOURCE} ..... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions				Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA				0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage (Note 2)		Am29C853, Am29C855	All Inputs	2.0		V
				Am29C833	$\overline{CLR}$	3.0		V
					Remaining Inputs	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V	V_{IN} = 0.0 V				−10	μA
		Input Only	V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V	V_{IN} = 2.7 V				5	μA
		Input Only	V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V				15	μA
			V_{OUT} = 5.5 V				20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V				−15	μA
			V_{OUT} = 0.0 V				−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)				−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL			160	μA
				COM'L			120	
I_{CCT}			V_{IN} = 3.4 V	R_i, T_j, Parity			3.0	mA/Bit
				$\overline{CLR}$, $\overline{EN}$, $\overline{OET}$, $\overline{OER}$			1.5	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)					400	μA/Bit/MHz

Notes: 1. n = number outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		15		18	ns
t_{PHL}					15		18	ns
t_{PLH}	Propagation Delay R_i to Parity				19		23	ns
t_{PHL}					19		23	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity				15		18	ns
t_{ZL}					15		18	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity				15		18	ns
t_{LZ}					15		18	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			18		21		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		2		ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to CLK Setup Time (Note 2)			15		18		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		6		9		ns
t_{PWL}		LOW		6		9		ns
t_{PWL}	Clear Pulse Width	LOW		6		9		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				15		18	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				20		23	ns
t_{PLH}	Propagation-Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29C853/854				29		33	ns
t_{PHL}					25		28	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				22		25	ns
t_{PHL}					22		25	ns

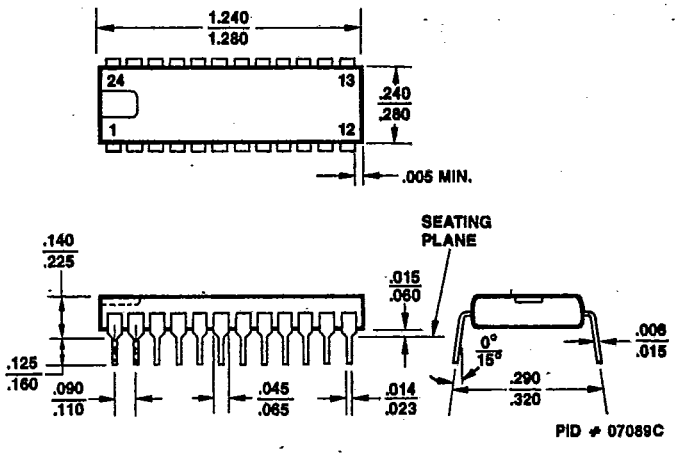
*See test circuit and waveforms.

Notes: 1. For Am29C853/Am29C855, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833.

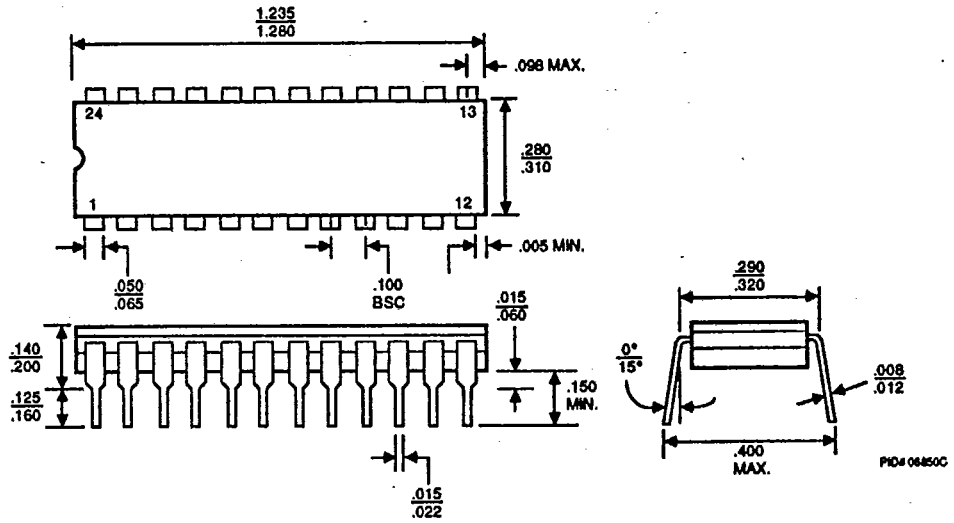
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

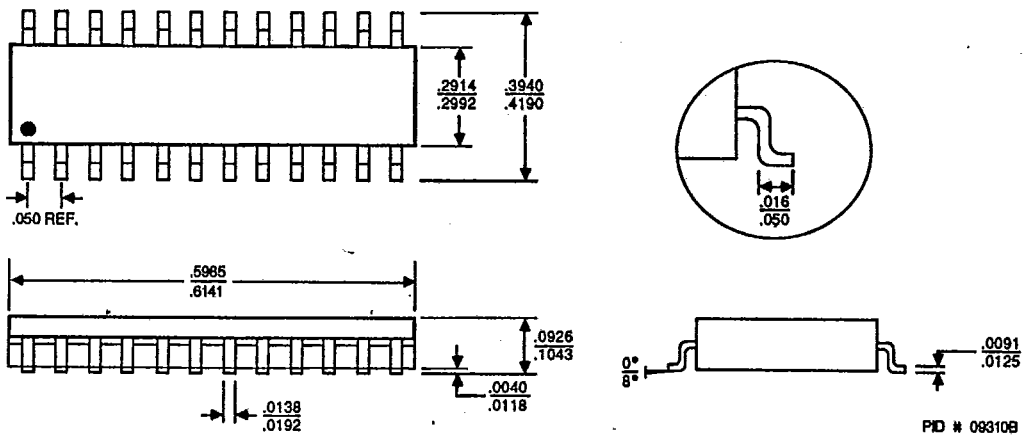


*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



PID # 09310B

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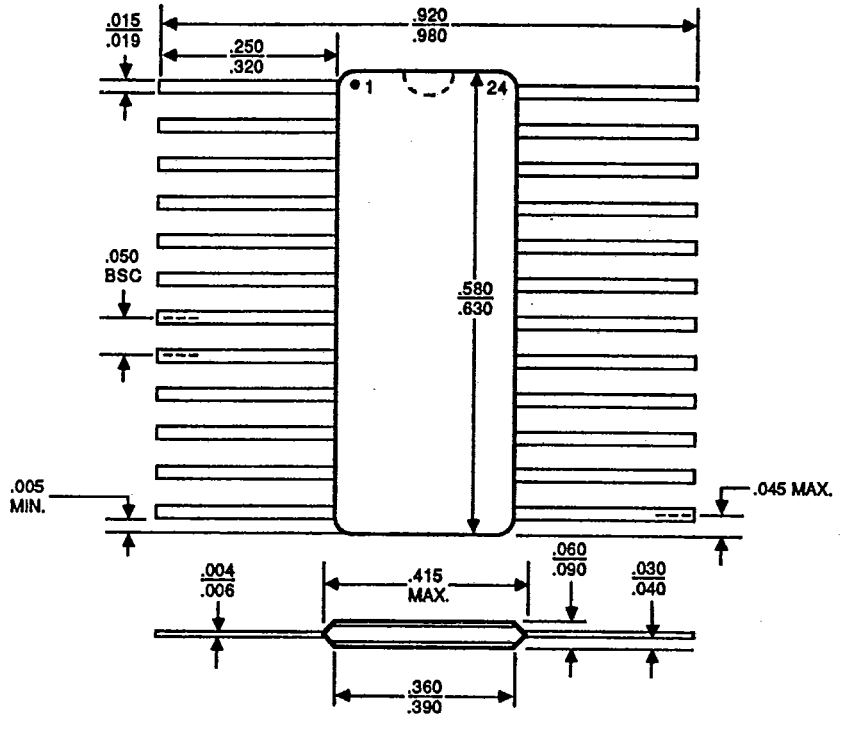
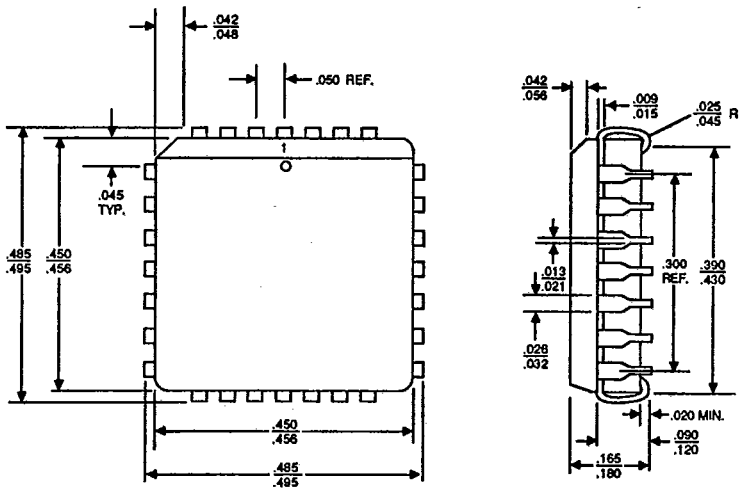


PID # 07371C

PACKAGE OUTLINES (Cont'd.)

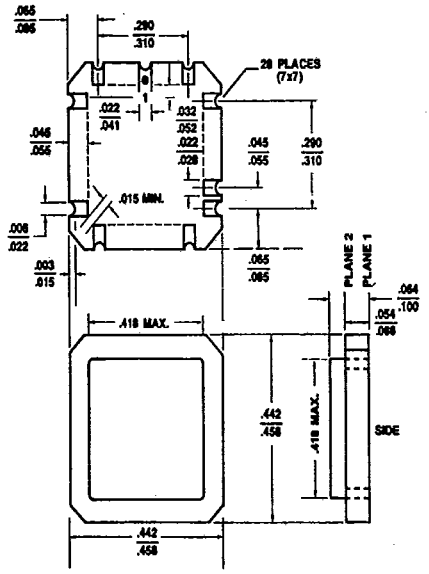
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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