

Product Preview

**8-Bit Serial or Parallel-Input/
Serial-Output Shift Register
with Input Latch**
High-Performance Silicon-Gate CMOS

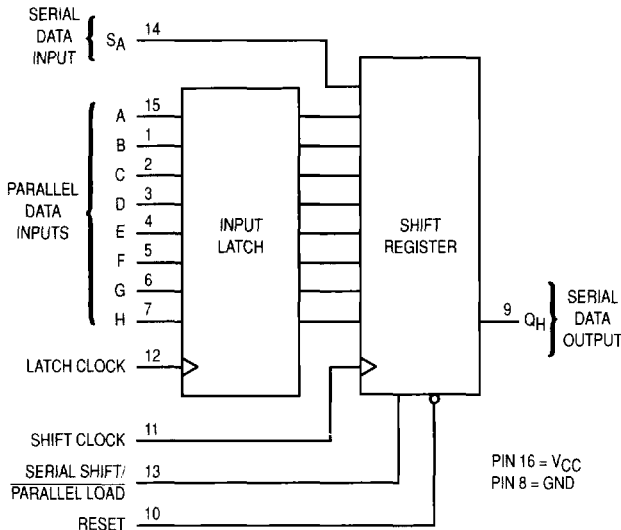
The MC54/74HC597A is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

The HC597A is similar in function to the HC589A, which is a 3-state device.

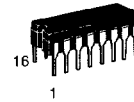
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates

LOGIC DIAGRAM

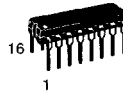


PIN 16 = VCC
PIN 8 = GND

MC54/74HC597A



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05



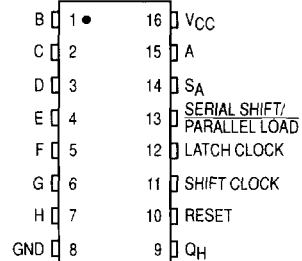
DT SUFFIX
TSSOP PACKAGE
CASE 948F-01

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

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PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
 Ceramic DIP: - 10 mW/°C from 100° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C
 TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 3.0 V	0	600	
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	10	9	8	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 1 and 8)	2.0	175	225	275	ns
		3.0	100	110	125	
		4.5	40	50	60	
		6.0	30	40	50	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 8)	2.0	160	200	240	ns
		3.0	90	130	160	
		4.5	30	40	48	
		6.0	25	30	40	
t _{PHL}	Maximum Propagation Delay, Reset to Q _H (Figures 3 and 8)	2.0	160	200	240	ns
		3.0	90	130	160	
		4.5	30	40	48	
		6.0	25	30	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 4 and 8)	2.0	160	200	240	ns
		3.0	90	130	160	
		4.5	30	40	48	
		6.0	25	30	40	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2.
- Information on typical parametric values can be found in Chapter 2.

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2.**3**

PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

SA (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

Serial Shift/Parallel Load (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

Reset (Pin 10)

Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

Shift Clock (Pin 11)

Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q_H , being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

OUTPUT

 Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register.

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data inputs A–H to Latch Clock (Figure 5)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 6)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_h	Minimum Hold Time, Latch Clock to Parallel Data Inputs A–H (Figure 5)	2.0	15	20	30	ns
		3.0	10	15	25	
		4.5	2	3	5	
		6.0	2	3	4	
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 6)	2.0	2	2	2	ns
		3.0	2	2	2	
		4.5	2	2	2	
		6.0	2	2	2	
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t_w	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 1 and 2)	2.0	60	70	80	ns
		3.0	35	40	45	
		4.5	12	15	19	
		6.0	10	13	16	
t_w	Minimum Pulse Width, Reset (Figure 3)	2.0	60	70	80	ns
		3.0	35	40	45	
		4.5	12	15	19	
		6.0	10	13	16	
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0	60	70	80	ns
		3.0	35	40	45	
		4.5	12	15	19	
		6.0	10	13	16	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2.

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FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S _A	Parallel Inputs A–H	Latch Contents	Shift Register Contents	Output Q _H
Reset shift register	L	X	L, H, $\bar{\text{L}}$	X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X	$\bar{\text{L}}$	X	X	a–h	a–h	L	L
Load parallel data into data latch	H	H	$\bar{\text{L}}$	L, H, $\bar{\text{L}}$	X	a–h	a–h	U	U
Transfer latch contents to shift register	H	L	L, H, $\bar{\text{L}}$	X	X	X	U	LR _N → SR _N	LR _H
Contents of data latch and shift register are unchanged	H	H	L, H, $\bar{\text{L}}$	L, H, $\bar{\text{L}}$	X	X	U	U	U
Load parallel data into data latch and shift register	H	L	$\bar{\text{L}}$	X	X	a–h	a–h	a–h	h
Shift serial data into shift register	H	H	X	$\bar{\text{L}}$	D	X	*	SR _A = D; SR _N → SR _{N+1}	SR _G → SR _H
Load parallel data into data latch and shift serial data into shift register	H	H	$\bar{\text{L}}$	$\bar{\text{L}}$	D	a–h	a–h	SR _A = D; SR _N → SR _{N+1}	SR _G → SR _H

LR = latch register contents

SR = shift register contents

* = depends on latch clock input

a–h = data at parallel data inputs A–H

D = data (L, H) at serial data input S_A

U = remains unchanged

X = don't care

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SWITCHING WAVEFORMS

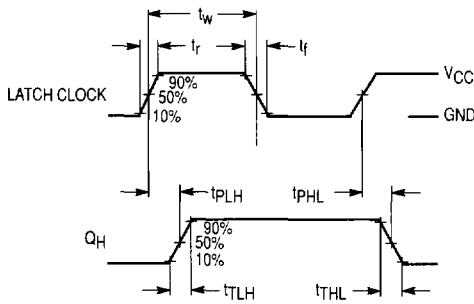


Figure 1. (Serial Shift/Parallel Load = L)

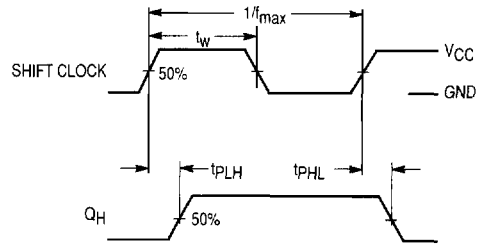


Figure 2. (Serial Shift/Parallel Load = H)

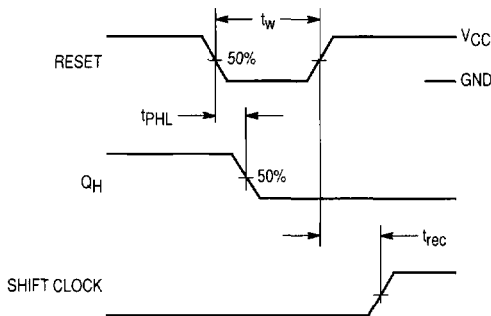


Figure 3.

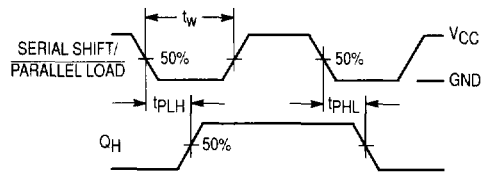


Figure 4.

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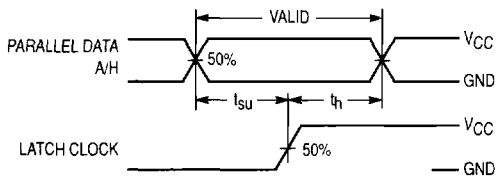


Figure 5.

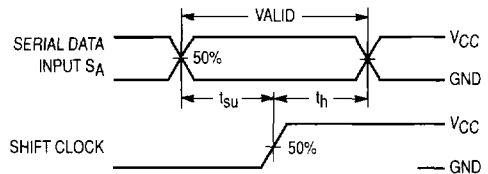


Figure 6.

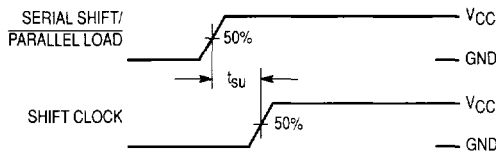
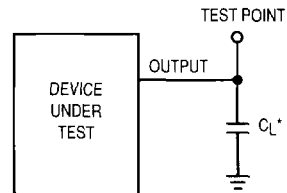


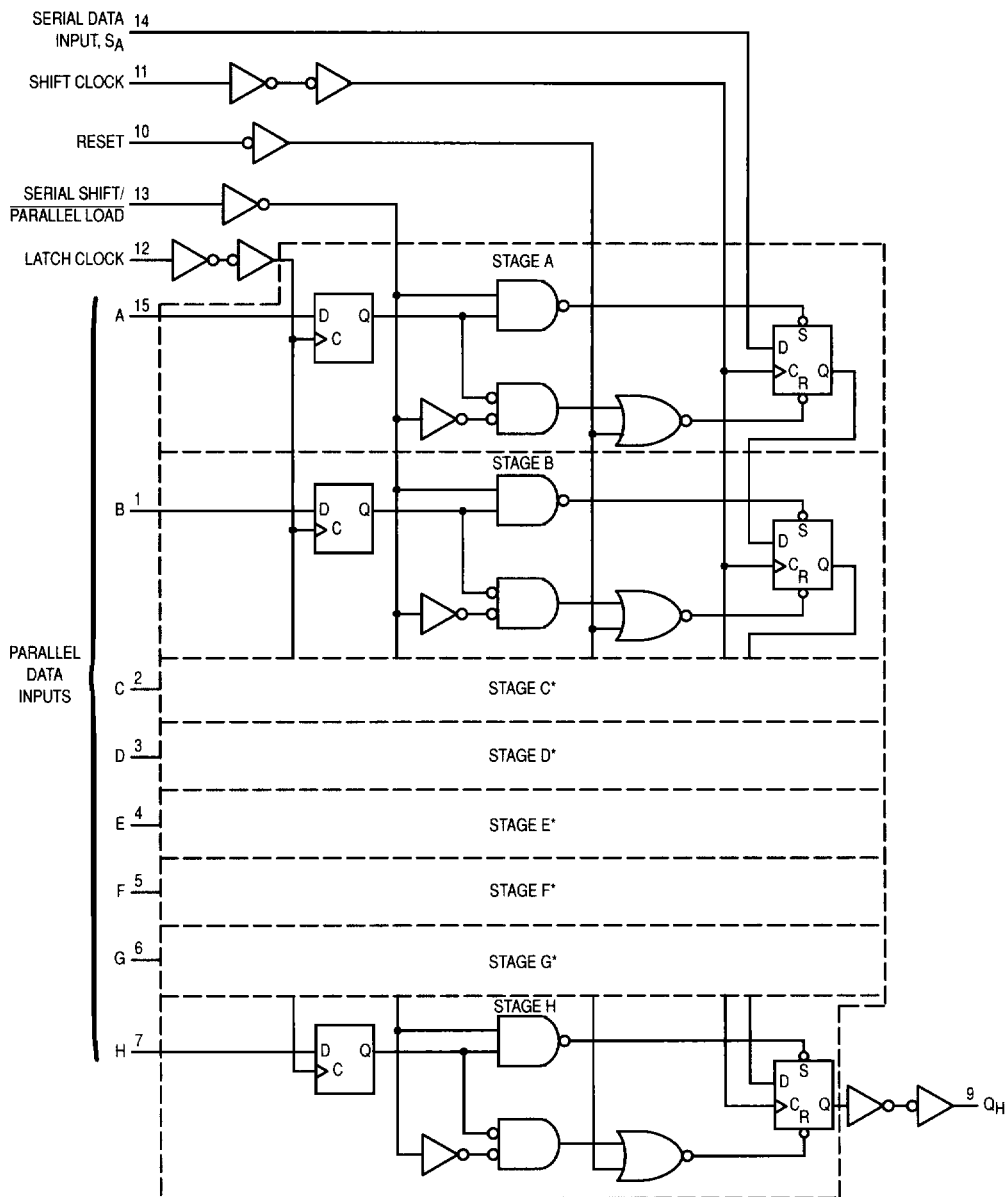
Figure 7.



* Includes all probe and jig capacitance

Figure 8. Test Circuit

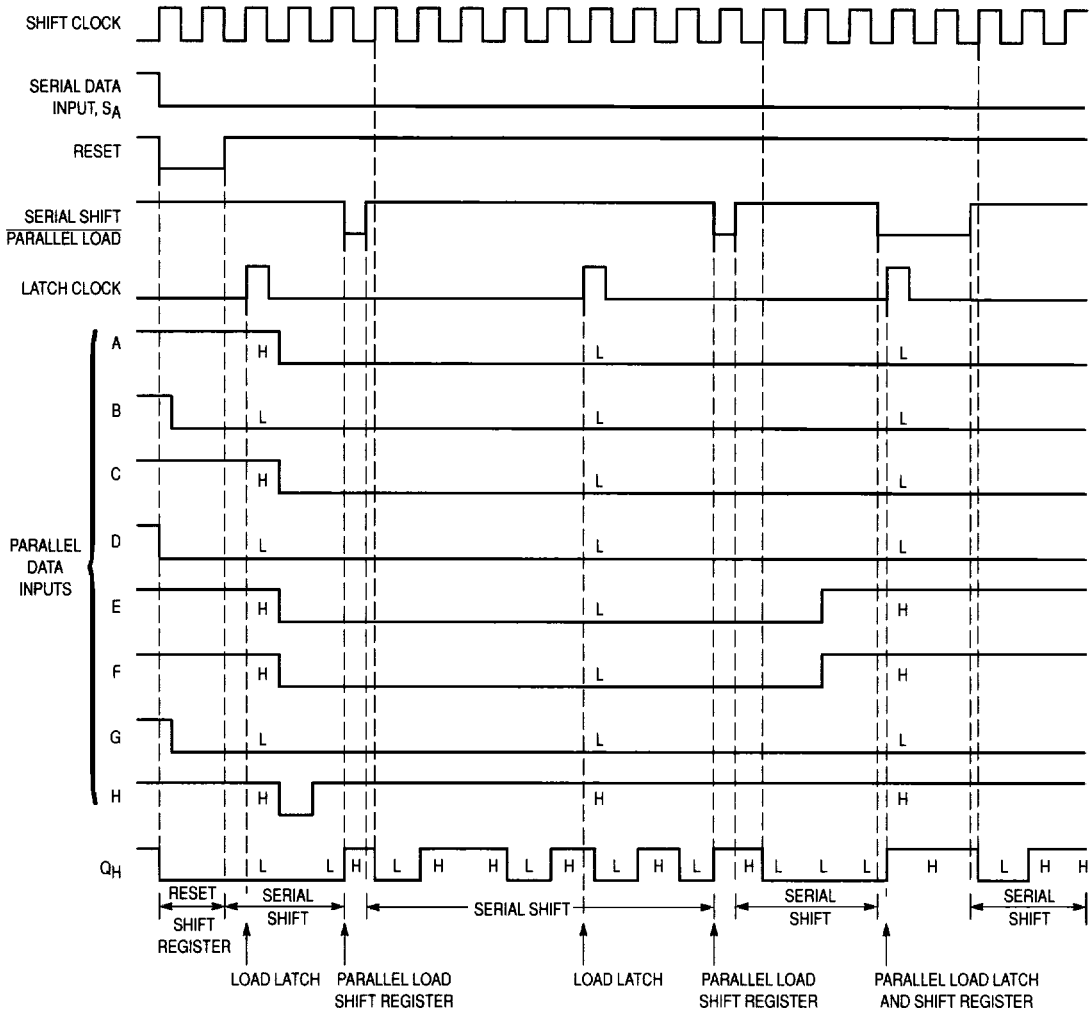
EXPANDED LOGIC DIAGRAM



*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

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TIMING DIAGRAM



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