

CMOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,
Synchronous Serial Input/Serial Output

The RCA-CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL DATA input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

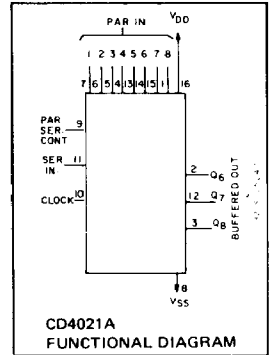
When the PARALLEL/SERIAL CONTROL input is low, data are serially shifted into the 8-stage register synchronously with the positive-going transition of the CLOCK pulse.

Features:

- Asynchronous parallel or synchronous serial operation under control of parallel/serial control input
- Individual JAM inputs to each register stage
- Master-slave flip-flop register stages
- Fully static operation. DC to 5 MHz
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

When the PARALLEL/SERIAL CONTROL input is high, data are jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using addi-



tional CD4021A packages.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, K, H PACKAGES				E PACKAGE				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current I _L Max.	-	-	5	5	0.5	5	300	50	0.5	50	700	μ A
	-	-	10	10	1	10	600	100	1	100	1400	
	-	-	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V _{OL} High Level, V _{OH}	-	5	5	0 Typ.; 0.05 Max.								V
	-	10	10	0 Typ.; 0.05 Max.								
	-	0	5	4.95 Min.; 5 typ.								
Noise Immunity: Inputs Low, V _{NL} Inputs High, V _{NH}	4.2	-	5	1.5 Min.; 2.25 Typ.								V
	9	-	10	3 Min.; 4.5 Typ.								
	0.8	-	5	1.5 Min.; 2.25 Typ.								
Noise Margin: Inputs Low, V _{NML} Inputs High, V _{NMH}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
	0.5	-	5	1 Min.								
Output Drive Current: N-Channel (Sink), I _D N Min. P-Channel (Source), I _D P Min.	0.5	-	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	-	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
	4.5	-	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
Input Leakage Current, I _{IL} , I _{IH}	-	-	15	$\pm 10^{-5}$ Typ., ± 1 Max.								

Applications:

- Parallel to serial data conversion
- Asynchronous parallel input/serial output data queueing
- General purpose register

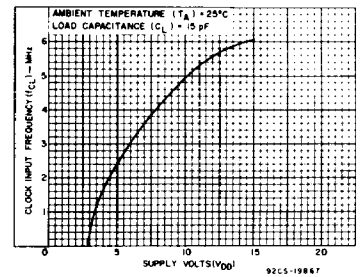


Fig. 1 - Typical clock input frequency vs. supply voltage.

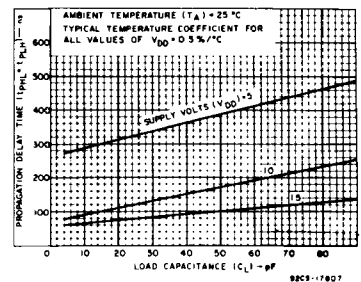


Fig. 2 - Typical propagation delay time vs. load capacitance.

CD4021A Types

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-85 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

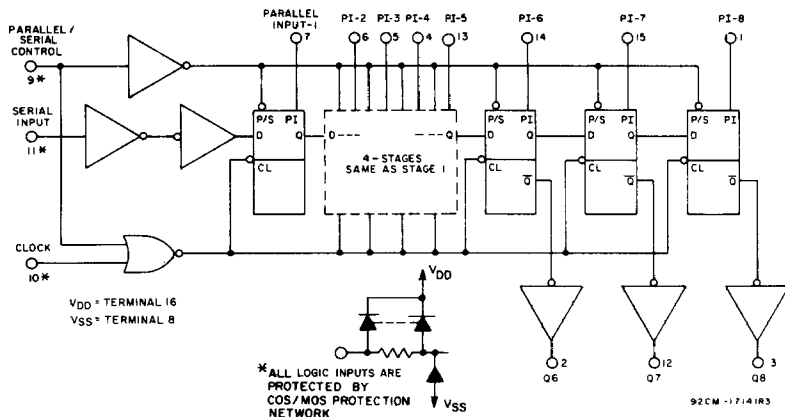


Fig. 5 - Logic diagram.

TRUTH TABLE

CL ^Δ	Serial Input	Parallel/Serial Control	PI-1	PI-n	Q ₁ (Internal)	Q _n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
	0	0	X	X	0	Q _{n-1}
	1	0	X	X	1	Q _{n-1}
	X	0	X	X	Q ₁	Q _n

Δ = LEVEL CHANGE X = DON'T CARE CASE
NO CHANGE

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Fig. 6 - Truth table.

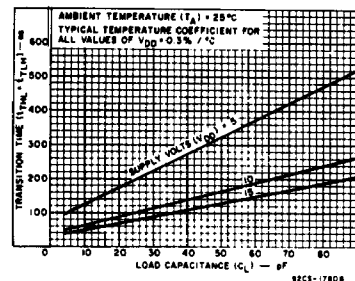


Fig. 3 - Typical transition time vs. load capacitance.

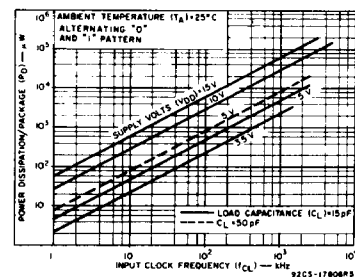


Fig. 4 - Typical dissipation characteristics.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	- -	500 100	- -	ns
Clock Pulse Width, t_{Wp}	5 10	500 175	- -	830 200	- -	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_{rCL} , t_{fCL}	5 10	- -	15 5	- -	15 5	μs

* If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

CD4021A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS	
		VDD (V)	D, F, K, H PACKAGES			E PACKAGE			
			MIN.	TYP.	MAX.	MIN.	TYP.		MAX.
Propagation Delay Time, ** t_{PLH}, t_{PHL}	5	-	300	750	-	300	1000	ns	
	10	-	100	225	-	300	300		
Transition Time; t_{THL}, t_{TLH}	5	-	150	300	-	150	400	ns	
	10	-	75	125	-	75	150		
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	-	0.6	2.5	-	MHz	
	10	3	5	-	2.5	5	-		
Minimum Clock Pulse Width, t_W	5	-	200	500	-	200	830	ns	
	10	-	100	175	-	100	200		
Clock Rise & Fall Time; t_{rCL} & t_{fCL} *	5	-	-	15	-	-	15	μs	
	10	-	-	5	-	-	5		
Minimum Data Set Up Time, t_S	5	-	100	350	-	100	500	ns	
	10	-	50	80	-	50	100		
Minimum High-Level Parallel/Serial Control Pulse Width t_W	5	-	200	500	-	200	830	ns	
	10	-	100	175	-	100	200		
Input Capacitance C_i	Any Input	-	5	-	-	5	-	pF	

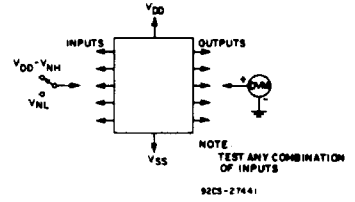


Fig. 7 - Noise-immunity test circuit.

Test performed with the following sequence of "One's" and "Zero's".

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S1 S2 S3 S4 S5
0 0 1 0 0
1 0 1 1 1
1 0 1 0 1
0 1 1 1 1
0 1 0 0 0
    
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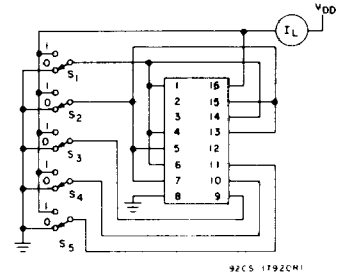


Fig. 8 - Quiescent device current test circuit.

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

**From Clock or Parallel/Serial Control Input

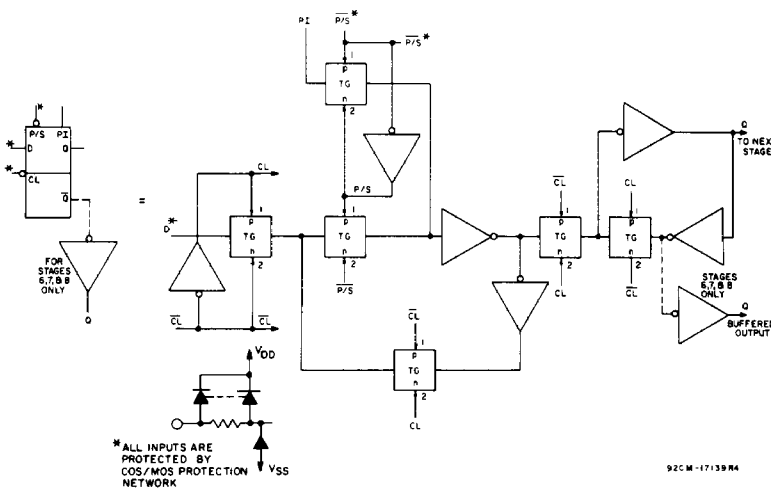


Fig. 10 - One typical stage and its equivalent detailed circuit.

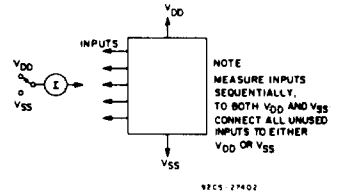


Fig. 9 - Input-leakage-current test circuit.