

Am29524/Am29525

Dual 7-/8-Deep Pipeline Registers

PRELIMINARY

ECL/TTL

DISTINCTIVE CHARACTERISTICS

- Provides temporary address or data storage
- Am29524 — Dual 7-deep or single 14-deep (with feed-through and 0) registers
- Am29525 — Dual 8-deep or single 16-deep registers
- Hold, or shift and load instructions
- High-speed ECL-internal technology, TTL-compatible I/O, packaged in 28-pin 0.4-inch (400 Mil) sidebraced DIPs
- All registers available at three-state output

GENERAL DESCRIPTION

The Am29524/Am29525 are 8-bit wide, 14- and 16-word deep pipeline registers. The registers are organized as two 7- or 8-byte shift registers. By microinstruction, data may be entered into either shift register.

Am29525, the shift registers are 8 deep and any of the sixteen registers may be output. In both devices, the two shift-register stacks may be cascaded to form a single 14- or 16-byte-long pipeline register.

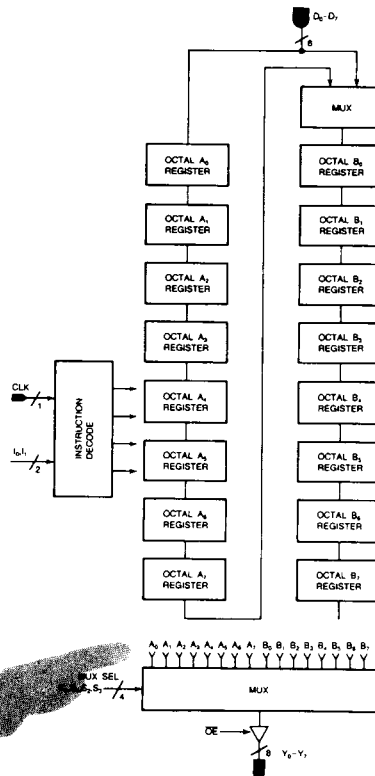
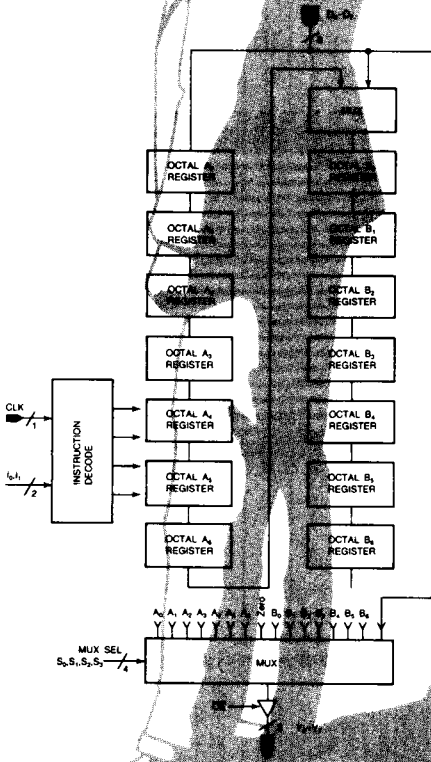
In the Am29524, the shift registers are 7 deep. All fourteen registers are available at the output, as well as the input data fed directly to the output, or an 8-bit byte. In the

A single clock is provided and operation of the shift registers is under microprogram control. The device has three-state outputs.

BLOCK DIAGRAMS

Am29524

Am29525



Bl 5-31

0000798

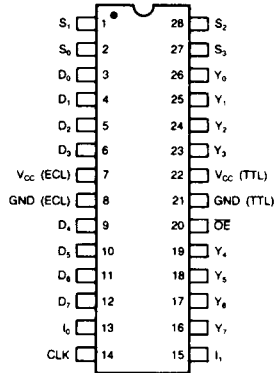
Oneq

3D006020

AM29



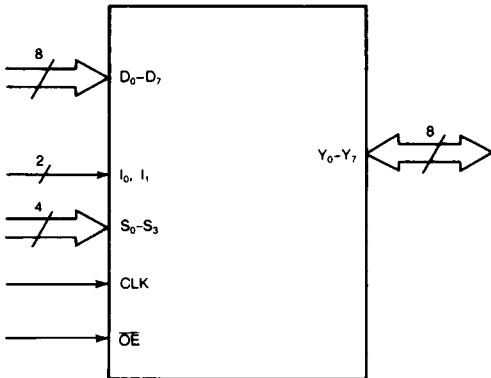
CONNECTION DIAGRAM Top View



CD009330

Note: Pin 1 is marked for orientation.

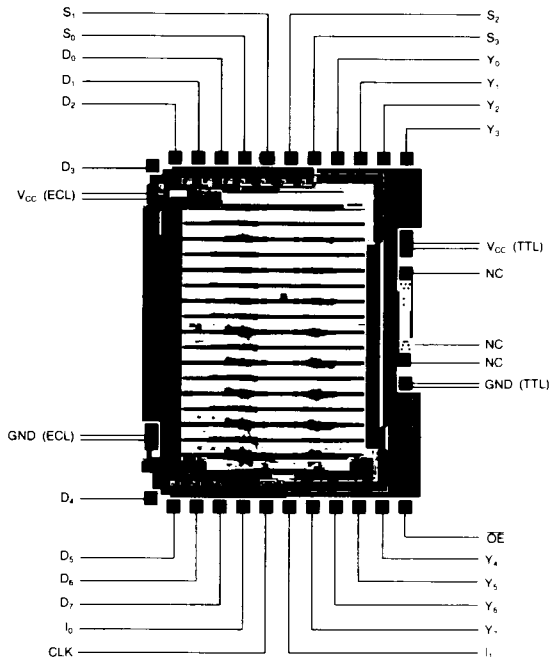
LOGIC SYMBOL



LS002300

V_{CC} (ECL) = ECL Power Supply
 V_{CC} (TTL) = TTL Power Supply
 GND (ECL) = ECL Ground
 GND (TTL) = TTL Ground

METALLIZATION AND PAD LAYOUT



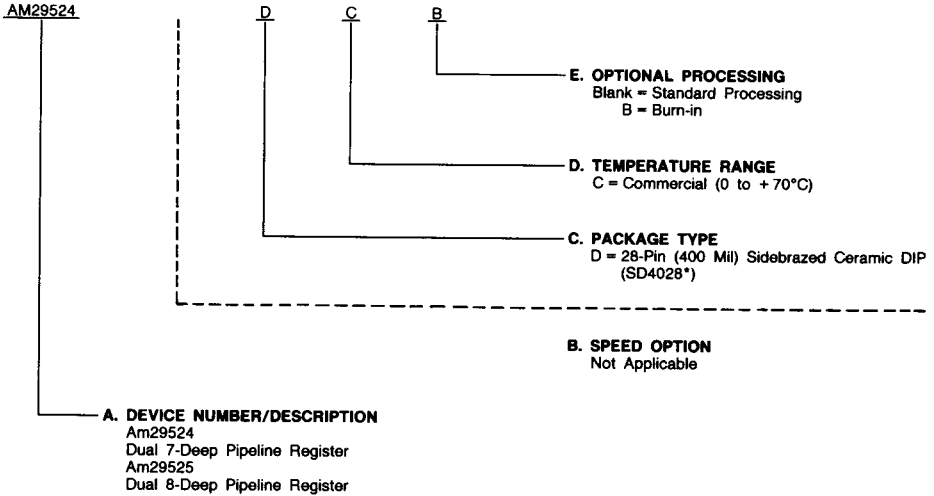
Die Size: .114" x .150"

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option (if applicable)**
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM29524, AM29525	DC, DCB

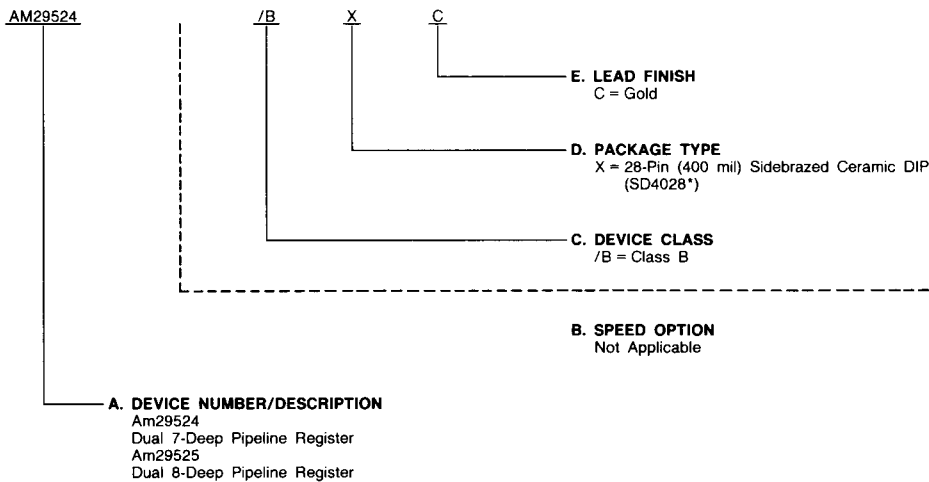
*Preliminary. Subject to Change.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



Valid Combinations	
AM29524, AM29525	/BXC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

*Preliminary. Subject to Change.

PIN DESCRIPTION

D₀ – D₇ Register Input Port (Input, Active HIGH)

Data to be written to any of the internal registers is input via this port.

Y₀ – Y₇ Register Output Port (Output, Three-State)

Data to be read out of any of the internal registers is output via this three-state port.

I₀, I₁ Instruction Inputs (Input, Active HIGH)

Operational control of the device is determined by these inputs. See Tables 1 through 3 for details.

S₀ – S₃ Register Output Select (Input, Active HIGH)

These inputs select which register appears on the Register Output Port. See Table 3 for details.

CLK Clock (Input)

The rising edge of the clock loads data into the appropriate registers as determined by the Instruction Inputs.

OE Output Enable (Input, Active LOW)

When LOW, the register selected by the Register Output Select Inputs appears on the Register Output Port. When HIGH, the Register Output Port is three-stated.

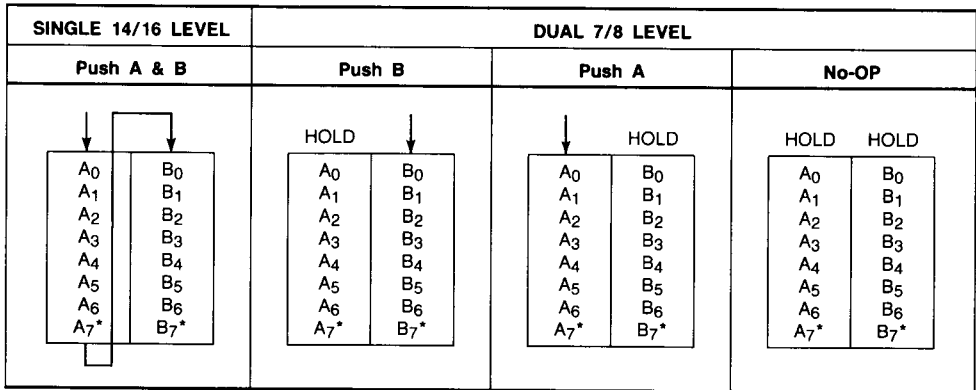
FUNCTIONAL DESCRIPTION

The following tables describe operation of the Am29524/29525. Table 1 illustrates register operation in response to instruction inputs I_0 and I_1 . Note that in the 7-deep device (Am29524), registers A₇ and B₇ do not exist. Table 2 gives the

operand values corresponding to the operations illustrated in Table 1. Table 3 gives the Register Output Select codes required to access a specific register, which then appears at the Register Output Port.

TABLE 1. REGISTER LOAD OPERATIONS

(See Table 2 for instruction codes.)



* A₇ and B₇ registers apply only to Am29525.

TABLE 2. INSTRUCTION SET DESCRIPTIONS

Mnemonic	Inputs		Description
	I_1	I_0	
Shift	0	0	Push A & B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	No-OP

TABLE 3. SELECT OPERATION DESCRIPTIONS

S ₃	S ₂	S ₁	S ₀	Y ₀ - Y ₇
0	0	0	0	A ₀
0	0	0	1	A ₁
0	0	1	0	A ₂
0	0	1	1	A ₃
0	1	0	0	A ₄
0	1	0	1	A ₅
0	1	1	0	A ₆
0	1	1	1	0 (Am29524)
				A ₇ (Am29525)
1	0	0	0	B ₀
				B ₁
1	0	1	0	B ₂
				B ₃
1	0	1	1	B ₄
				B ₅
1	1	0	0	B ₆
				B ₇
1	1	1	0	D ₀ - D ₇ (Am29524)
				B ₇ (Am29525)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Case Temperature under Bias (T_C) -55 to +125°C
 DC Supply Voltage
 to Ground Potential Continuous -0.5 to +7.0 V
 DC Voltage Applied to Outputs for
 HIGH Output State -0.5 to + V_{CC} Max.
 DC Input Voltage -0.5 to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
 Temperature (T_A) 0 to +70°C
 Supply Voltage (V_{CC}) +4.75 to +5.25 V
 Military (M) Devices
 Temperature (T_C) -55 to +125°C
 Supply Voltage (V_{CC}) +4.5 to +5.5 V

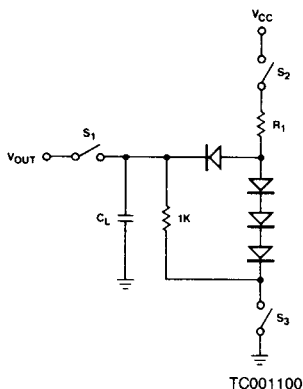
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Units
V_{OH}	Output HIGH Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{CC} = \text{Min.}$	$I_{OH} = -0.3 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.},$ $V_{IN} = V_{IH}$ or V_{IL}	Com: $I_{OL} = 24 \text{ mA}$ Mil: $I_{OL} = 16 \text{ mA}$		0	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Input		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Input			0.8	V
V_I	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{I} = -1 \text{ mA}$			-1.5	V
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0 \text{ V}$ for inputs			-0.5	mA
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.4 \text{ V}$			50.0	μA
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 5.5 \text{ V}$			1.0	mA
$I_{OZH},$ I_{OZL}	Off-State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.4 \text{ V}$		50.0	μA
			$V_O = 0.4 \text{ V}$		-50.0	
I_{SC}	Output Short-Circuit Current (Note 2)	$V_{CC} = \text{Max.} + 0.5 \text{ V}$ $V_O = 0.5 \text{ V}$		-20.0	-100.0	mA
I_{CC}	Power Supply Current (Note 3)	Com. Only	$T_A = 0 \text{ to } +70^\circ\text{C}$			mA
		$V_{CC} = \text{Max.}$	$T_A = +70^\circ\text{C}$		345	
		Mil. Only	$T_C = -55 \text{ to } +125^\circ\text{C}$		400	
		$V_{CC} = \text{Max.}$	$T_C = +125^\circ\text{C}$			

- Notes: 1. For conditions shown as Min. or Max., use appropriate values specified under Operating Ranges for applicable device type.
 2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
 3. All inputs LOW.

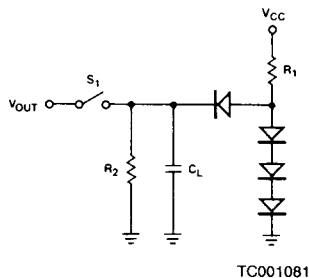
SWITCHING TEST CIRCUITS



A. Three-State Outputs

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

- Notes:
1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
 2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
 3. S_1 and S_3 are closed while S_2 is open for tp_{ZH} test.
 4. S_1 and S_2 are closed while S_3 is open for tp_{ZL} test.
 5. $C_L = 5.0$ pF for output disable tests.



B. Normal Outputs

$$R_2 = \frac{2.4 V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

Test Philosophy and Methods

The following points give the general philosophy which we apply to tests which must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data-sheet reconciliation which follow.

Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance which varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays in to and out of the high-impedance state and are usually the test is performed at the higher load capacitance the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data-sheet loads, may be used during production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels.

AC Testing

AC parameters are specified which cannot be measured accurately on automatic testers because of tester limitations. Data-input hold times fall into this category. In these cases, the parameter in question is tested by correlating the tester to bench data or oscilloscope measurements made on the tester by engineering (supporting data on file).

Certain AC tests are redundant since they can be shown to be predicted by other tests which have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

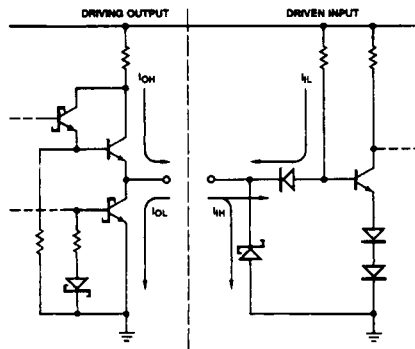
When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) which is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0, V_{CC} = \text{Max. case}$.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

No.	Parameter Symbol		Parameter Description	Test Conditions	Commercial		Military		Units	
					Min.	Max.	Min.	Max.		
1	t _{PDCO}	t _{PLH}	CLK to Y ₀ -Y ₇	R _L = 150 Ω C _L = 50 pF				21	ns	
		t _{PHL}								
2	t _{PDSO}	t _{PLH}	S ₀ -S ₃ to Y ₀ -Y ₇					21	ns	
		t _{PHL}								
3	t _{PDDO}	t _{PLH}	D ₀ -D ₇ to Y ₀ -Y ₇ (Note 1)					20	ns	
		t _{PHL}								
4	t _{SD}		D ₀ -D ₇ to CLK Setup					9	ns	
5	t _{HD}		CLK to D ₀ -D ₇ Hold					0	ns	
6	t _{SI}		I _{0,1} to CLK Setup					11	ns	
7	t _{HI}		CLK to I _{0,1} Hold					0	ns	
8	t _{PHZ}	OE to Output Enable/Disable Times			C _L = 5 pF				15	ns
9	t _{PLZ}									
10	t _{PZH}				C _L = 50 pF					20
11	t _{PZL}									
12	t _{PWH}		Clock Pulse Width HIGH				12	ns		
13	t _{PWL}		Clock Pulse Width LOW					ns		

Notes: 1. Am29524 only.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

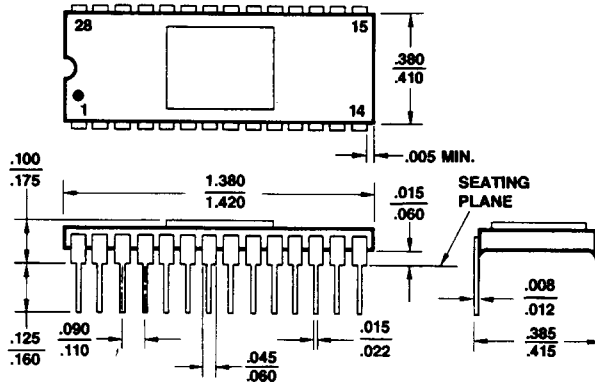


ICR00501

PHYSICAL DIMENSIONS

SD4028*

H21.5



PID # 07930A

*Preliminary. Subject to Change.

The International Standard of
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electrical parameters, AC and DC,
over the entire operating range.

INT·STD·500

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