

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

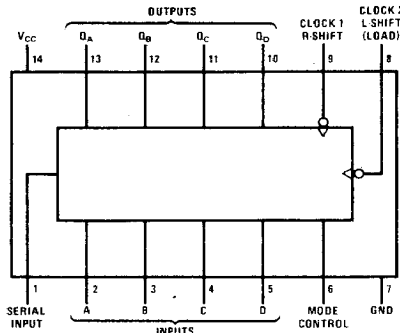
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2

when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

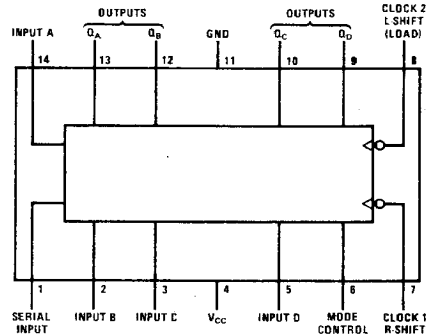
Features

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
95	36 MHz	250 mW
L95	14 MHz	24 mW
LS95B	36 MHz	65 mW

Connection Diagrams

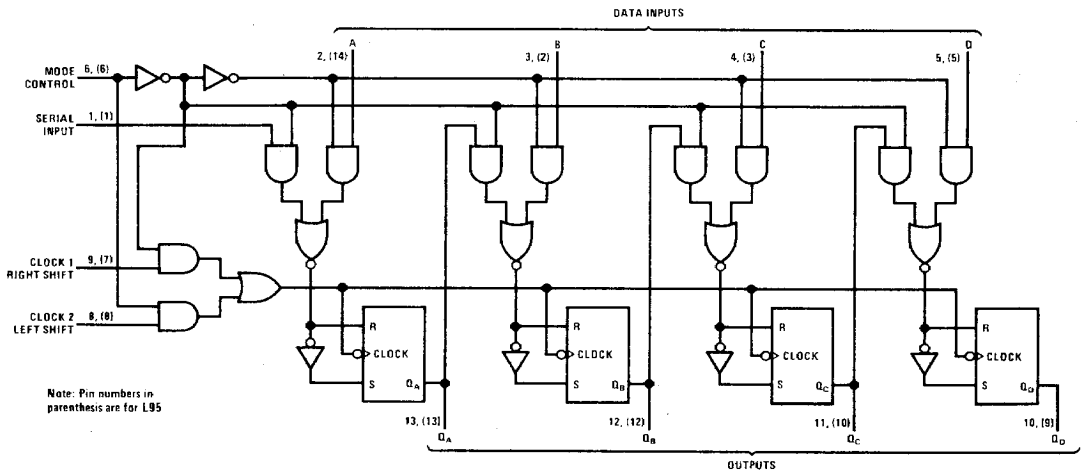


5495(J), (W); 7495(J), (N), (W);
54LS95B/74LS95B(J), (N), (W)



54L95/74L95(J), (N), (W)

Logic Diagram



Note: Pin numbers in parenthesis are for L95

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	DM54/74		DM54L/74L		DM54LS/74LS		UNITS
		MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage		0.8		0.7		0.7	V
V _I	Input Clamp Voltage		0.8		0.7		0.8	V
I _{OH}	High Level Output Current		-1.5		N/A		-1.5	V
V _{OH}	High Level Output Voltage			-800			-400	μA
I _{OL}	Low Level Output Current		2.4	3.4	2.4	3.1	2.5	3.4
V _{OL}	Low Level Output Voltage		2.4	3.4	2.4	3.1	2.7	3.4
I _I	Input Current at Maximum Input Voltage		16		2		4	mA
I _{IH}	High Level Input Current		16		3.6		8	mA
I _{IL}	Low Level Input Current		0.2	0.4	0.13	0.3	0.25	0.4
I _{OS}	Short Circuit Output Current		0.2	0.4	0.2	0.4	0.35	0.5
I _{CC}	Supply Current		1		0.2		0.25	0.4

Notes

- (1) All typical values are at V_{CC} = 5V, T_A = 25°C.
- (2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.
- (3) I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics $V_{CC} = 5V, T_A = 25^{\circ}C$

PARAMETER	DM54/74			DM54L/74L			DM54LS/74LS			UNITS		
	95			L95			LS95B					
	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX				
t_{max}		25	36			6	14		25	36	MHz	
t_{PLH}	Maximum Clock Frequency											
	Propagation Delay Time, Low-to-High Level Output From Clock	$C_L = 15\text{ pF}$ $R_L = 400\Omega$	25	35	$C_L = 50\text{ pF}$ $R_L = 4\text{ k}\Omega$		42	90	$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$	18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock						48	90		21	32	ns
$t_{W(CLOCK)}$	Width of Clock Pulse		15			90				25		ns
t_{SETUP}	Setup Time, High-Level Data		20	10		50				20		ns
t_{SETUP}	Setup Time, Low-Level Data		20	10		50				20		ns
t_{HOLD}	Hold Time, High-Level or Low-Level Data		0	-10		0				10		ns
$t_{ENABLE1}$	Time to Enable Clock 1		20			120				20		ns
$t_{ENABLE2}$	Time to Enable Clock 2		15			100				20		ns
$t_{INHIBIT1}$	Time to Inhibit Clock 1		10			0				20		ns
$t_{INHIBIT2}$	Time to Inhibit Clock 2		10			0				20		ns

1 Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)
↑ = Transition from high to low level, ↓ = Transition from low to high level
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = The level of Q_A, Q_B, Q_C, Q_D , respectively, before the indicated steady state input conditions were established.
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = The level of Q_A, Q_B, Q_C, Q_D , respectively, before the most recent transition of the clock.

Truth Table

MODE CONTROL	INPUTS				OUTPUTS							
	CLOCKS Z (L) 1 (R)	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D		
			A	B	C	D						
H	H	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
H	↑	X	X	X	X	a	b	c	d			
H	↓	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	d			
L	L	H	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
L	X	↑	X	X	X	H	Q_{Bn}	Q_{Cn}	Q_{Dn}			
L	X	↓	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}			
↑	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
↓	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
↑	L	H	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
↓	L	H	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
↑	H	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			
↓	H	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}			