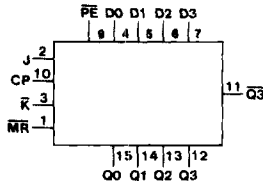


# High-Speed CMOS Logic

## 4-Bit Parallel Access Register



**FUNCTIONAL DIAGRAM**

**Type Features:**

- Asynchronous Master Reset
- J,  $\bar{K}$ , (D) inputs to first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complementary output from last stage
- Buffered inputs
- Typical  $f_{MAX}=50$  MHz @  $V_{CC}=5$  V,  $C_L=15$  pF,  $T_A=25^\circ$  C

**Family Features:**

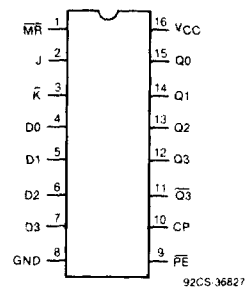
- Fanout (Over Temperature Range):  
Standard Outputs - 10 LSTTL Loads  
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:  
CD74HC/HCT:  $-40$  to  $+85^\circ$  C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:  
2 to 6 V Operation  
High Noise Immunity:  $N_{IL}=30\%$ ,  $N_{IH}=30\%$  of  $V_{CC}$   
@  $V_{CC}=5$  V
- CD54HCT/CD74HCT Types:  
4.5 to 5.5 V Operation  
Direct LSTTL Input Logic Compatibility  
 $V_{IL}=0.8$  V Max.,  $V_{IH}=2$  V Min.  
CMOS Input Compatibility  
 $I_i \leq 1 \mu A$  @  $V_{OL}$ ,  $V_{OH}$

The functional characteristics of the RCA-CD54/74HC195 and CD54/74HCT195 4-Bit Parallel Access Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The two modes of operation, shift right (Q0-Q1) and parallel load, are controlled by the state of the Parallel Enable (PE) input. Serial data enters the first flip-flop (Q0) via the J and  $\bar{K}$  inputs when the PE input is high, and is shifted one bit in the direction Q0-Q1-Q2-Q3 following each LOW-to-HIGH clock transition. The J and  $\bar{K}$  inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the PE input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D0-D3) is transferred to the respective Q0-Q3 outputs. Shift left operation (Q3-Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the PE input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The HC/HCT195 series utilizes edge-triggering; therefore, there is no restriction on the activity of the J,  $\bar{K}$ , Pn and PE inputs for logic operations, other than the set-up and hold time requirements. A LOW on the asynchronous Master Reset ( $\bar{MR}$ ) input sets all Q outputs LOW, independent of any other input condition.

The CD54HC195 and CD54HCT195 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC195 and CD74HCT195 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).



**TERMINAL ASSIGNMENT**

# CD54/74HC195 CD54/74HCT195

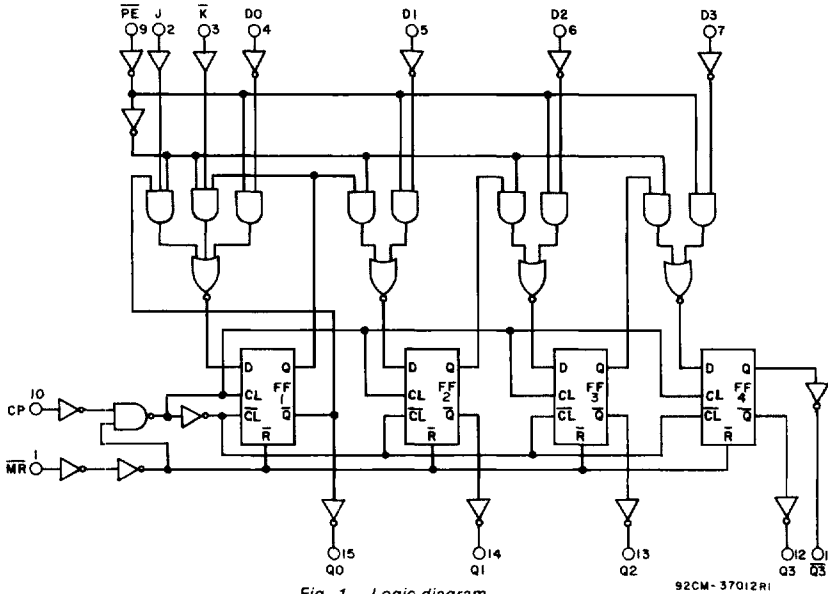


Fig. 1 - Logic diagram.

**Function Table**

Operating Modes	INPUTS						OUTPUTS				
	MR	CP	PE	J	K	D <sub>n</sub>	Q0	Q1	Q2	Q3	Q3̄
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set first stage	H	↗	h	h	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Reset first stage	H	↗	h	l	l	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Toggle first stage	H	↗	h	h	l	X	q̄ <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Retain first stage	H	↗	h	l	h	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Parallel Load	H	↗	l	X	X	d <sub>n</sub>	d <sub>0</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>	d̄ <sub>3</sub>

H=HIGH voltage level.

L=LOW voltage level.

X=Don't care.

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

d<sub>n</sub> (q<sub>n</sub>)=Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

↗=LOW-to-HIGH clock transition.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE, (V<sub>CC</sub>):

(Voltages referenced to ground) ..... -0.5 to + 7 V

DC INPUT DIODE CURRENT, I<sub>IK</sub> (FOR V<sub>i</sub> < -0.5 V OR V<sub>i</sub> > V<sub>CC</sub> + 0.5 V) ..... ±20mA

DC OUTPUT DIODE CURRENT, I<sub>OK</sub> (FOR V<sub>o</sub> < -0.5 V OR V<sub>o</sub> > V<sub>CC</sub> + 0.5 V) ..... ±20mA

DC DRAIN CURRENT, PER OUTPUT (I<sub>O</sub>) (FOR -0.5 V < V<sub>o</sub> < V<sub>CC</sub> + 0.5 V) ..... ±25mA

DC V<sub>CC</sub> OR GROUND CURRENT (I<sub>CC</sub>) ..... ±50mA

POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW

For T<sub>A</sub> = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW

For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW

For T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW

For T<sub>A</sub> = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW

For T<sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE F, H ..... -55 to +125°C

PACKAGE TYPE E, M ..... -40 to +85°C

STORAGE TEMPERATURE (T<sub>stg</sub>) ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)

with solder contacting lead tips only ..... +300°C

# CD54/74HC195 CD54/74HCT195

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC195/CD54HC195									CD74HCT195/CD54HCT195									UNITS						
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES			54HC TYPES			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES			54HCT TYPES				
	V <sub>I</sub> V	I <sub>O</sub> mA	V <sub>CC</sub> V	+25°C			-40/ +85°C			-55/ +125°C			V <sub>I</sub> V	V <sub>CC</sub> V	+25°C			-40/ +85°C			-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Typ	Max	Min		Max	Min	Max			
High-Level Input Voltage V <sub>IH</sub>			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5			2	—	—	2	—	2	—	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	to			2	—	—	2	—	2	—	—	V	
			6	4.2	—	—	4.2	—	4.2	—	—	—	5.5											V	
Low-Level Input Voltage V <sub>IL</sub>			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5											V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	to			0.8	—	0.8	—	0.8	—	0.8	—	—	V
			6	—	—	1.8	—	1.8	—	1.8	—	—	5.5											V	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IL</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	—	V <sub>IL</sub>												V	
or CMOS Loads	V <sub>IH</sub>		4.5	4.4	—	—	4.4	—	4.4	—	—	or	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	—	V	
	V <sub>IH</sub>		6	5.9	—	—	5.9	—	5.9	—	—	V <sub>IH</sub>												V	
TTL Loads	V <sub>IL</sub>										V <sub>IL</sub>													V	
or		-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	—	—	—	V		
V <sub>IH</sub>		-5.2	6	5.48	—	—	5.34	—	5.2	—	V <sub>IH</sub>												V		
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IL</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V <sub>IL</sub>												V	
or CMOS Loads	V <sub>IH</sub>		4.5	—	—	0.1	—	0.1	—	0.1	—	or	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	—	V	
	V <sub>IH</sub>		6	—	—	0.1	—	0.1	—	0.1	—	V <sub>IH</sub>												V	
TTL Loads	V <sub>IL</sub>										V <sub>IL</sub>													V	
or		4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	—	V		
V <sub>IH</sub>		5.2	6	—	—	0.26	—	0.33	—	0.4	V <sub>IH</sub>												V		
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub>		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V <sub>CC</sub> & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	—	μA	
or Gnd																									μA
																									μA
Quiescent Device Current I <sub>CC</sub>	V <sub>CC</sub>	0	6	—	—	8	—	80	—	160	—	V <sub>CC</sub>	5.5	—	—	8	—	80	—	160	—	160	—	μA	
or												or												μA	
Gnd												Gnd												μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI <sub>CC</sub> *												4.5												μA	
												V <sub>CC</sub> -2.1	to	—	100	360	—	450	—	490	—	—	—	μA	
												5.5												μA	

\*For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0-D3	0.3
PE	0.65
MR	0.3
CP	0.3
J, K	0.3

\*Unit Load is ΔI<sub>CC</sub> limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC195 CD54/74HCT195

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> =Full Package Temperature Range) V <sub>CC</sub> *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V <sub>in</sub> , V <sub>out</sub>	0	V <sub>CC</sub>	V
Operating Temperature T <sub>A</sub> :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t <sub>r</sub> , t <sub>f</sub>			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

\*Unless otherwise specified, all voltages are referenced to Ground.

**SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns)**

CHARACTERISTIC	SYMBOL	C <sub>L</sub> pF	Typical		Units
			HC	HCT	
CP to Qn Propagation Delay	t <sub>PHL</sub> t <sub>PLH</sub>	15	14	14	ns
MR to Qn	t <sub>PHL</sub>	15	13	14	ns
Maximum Clock Frequency	f <sub>MAX</sub>	15	50	50	MHz
Power Dissipation Capacitance*	C <sub>PD</sub>	—	45	50	pF

\*C<sub>PD</sub> is used to determine the dynamic power consumption, per register.

$$PD = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o \text{ where}$$

f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

**CD54/74HC195**  
**CD54/74HCT195**

**Pre-requisite for Switching Function**

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency (Figure 3)	f <sub>MAX</sub>	2	6	—	—	5	—	—	—	4	—	—	—	ns	
		4.5	30	—	25	—	25	—	20	—	20	—	16		
		6	35	—	—	—	29	—	—	—	23	—	—		
MR Pulse Width (Figure 3)	t <sub>w</sub>	2	80	—	—	100	—	—	—	120	—	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		
		6	14	—	—	—	17	—	—	—	20	—	—		
Clock Pulse Width (Figure 3)	t <sub>w</sub>	2	80	—	—	100	—	—	—	120	—	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		
		6	14	—	—	—	17	—	—	—	20	—	—		
Set-up Time J, $\overline{K}$ , $\overline{PE}$ to Clock (Figure 5)	t <sub>SU</sub>	2	100	—	—	125	—	—	—	150	—	—	—	ns	
		4.5	20	—	20	—	25	—	25	—	30	—	30		
		6	17	—	—	—	21	—	—	—	26	—	—		
Hold Time J, $\overline{K}$ , $\overline{PE}$ to Clock (Figure 5)	t <sub>H</sub>	2	3	—	—	3	—	—	—	3	—	—	—	ns	
		4.5	3	—	3	—	3	—	3	—	3	—	3		
		6	3	—	—	—	3	—	—	—	3	—	—		
Removal Time MR to Clock (Figure 3)	t <sub>REM</sub>	2	80	—	—	100	—	—	—	120	—	—	—	ns	
		4.5	16	—	16	—	20	—	20	—	24	—	24		
		6	14	—	—	—	17	—	—	—	20	—	—		

**SWITCHING CHARACTERISTICS (C<sub>L</sub>=50 pF, Input t<sub>r</sub>,t<sub>f</sub>=6 ns)**

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay CP to Output (Figure 3)	t <sub>PLH</sub>	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay MR to Output (Figure 3)	t <sub>PLH</sub>	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C <sub>i</sub>		—	10	—	10	—	10	—	10	—	10	—	pF	

# CD54/74HC195 CD54/74HCT195

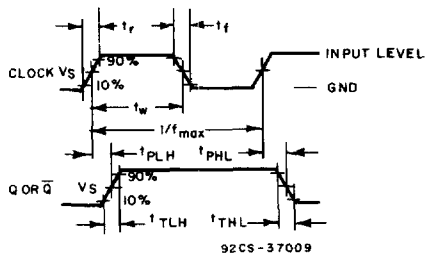


Fig. 3 - Clock pre-requisite and propagation delays and output transition times.

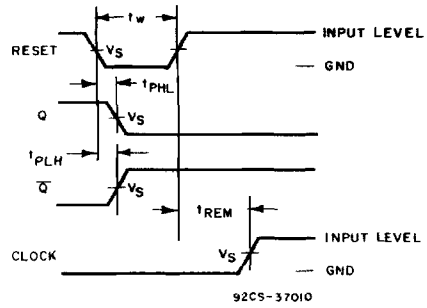


Fig. 4 - Master Reset pre-requisite and propagation delays.

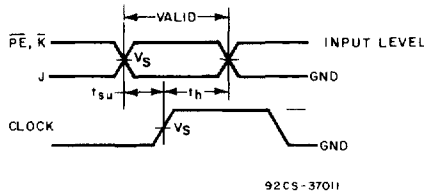


Fig. 5 - J,  $\bar{K}$  or Parallel Enable pre-requisite times.

	HC	HCT
INPUT LEVEL	$V_{CC}$	3V
$V_S$	50%	1.3V