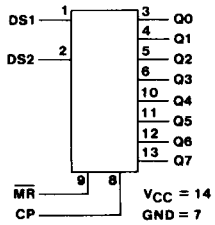
Recent Additions
CD54AC164/3A
CD54ACT164/3A

8-Bit Serial-In/Parallel-Out Shift Register

The RCA CD54AC164 and CD54ACT164 are 8-bit serial-in/parallel-out shift registers with asynchronous reset that utilize the new RCA ADVANCED CMOS LOGIC technology. Data are shifted on the positive edge of the clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided; either one can be used as a Data Enable control.

The CD54AC/ACT164 are supplied in 14-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

Package Specifications
(See Section 11, Fig. 10)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
DS1, DS2	0.5
$\overline{MR}$	0.74
CP	0.71

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections
Identical to CD54HC/HCT164/3A, page 5-71.

Recent Additions
CD54AC164/3A
CD54ACT164/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH}	1.5	—	157	ns
	t_{PHL}	3.3*	3.2	17.5	
		5†	2.1	12.5•	
$\overline{MR}$ to Qn	t_{PLH}	1.5	—	174	ns
	t_{PHL}	3.3	3.7	19.5	
		5	2.4	13.9•	
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH}	5†	2.6	14.9•	ns
$\overline{MR}$ to Qn	t_{PHL}	5	2.7	15.8•	
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per device.
For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

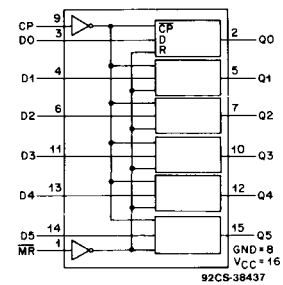
(Limits with black dots (•) are tested 100%.)

CD54AC174/3A
CD54ACT174/3A

Hex D Flip-Flop with Reset

The RCA CD54AC174 and CD54ACT174 are hex D flip-flops with reset that utilize the new RCA ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All six flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low-voltage level independent of the clock.

The CD54AC174 and CD54ACT174 are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

Package Specifications
(See Section 11, Fig. 11)