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April 1st, 2010
Renesas Electronics Corporation

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HD74HC670

4-by-4 Register File (with 3-state outputs)

REJ03D0639-0200
 (Previous ADE-205-521)
 Rev.2.00
 Mar 30, 2006

Description

The HD74HC670, 16-bit register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data.

This permits simultaneous writing into one location and reading from another word location. Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, (G_W) is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, (G_R) is high, the data outputs are inhibited and go into the high-impedance state. The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

Features

- High Speed Operation: t_{pd} (Read Select to Q) = 21 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC670P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC670FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Write Inputs			Word			
W _B	W _A	G _W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

Read Inputs			Outputs			
R _B	R _A	G _R	Q ₁	Q ₂	Q ₃	Q ₄
L	L	L	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃	W ₀ B ₄
L	H	L	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃	W ₁ B ₄
H	L	L	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃	W ₂ B ₄
H	H	L	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃	W ₃ B ₄
X	X	H	Z	Z	Z	Z

H : high level

L : low level

X : irrelevant

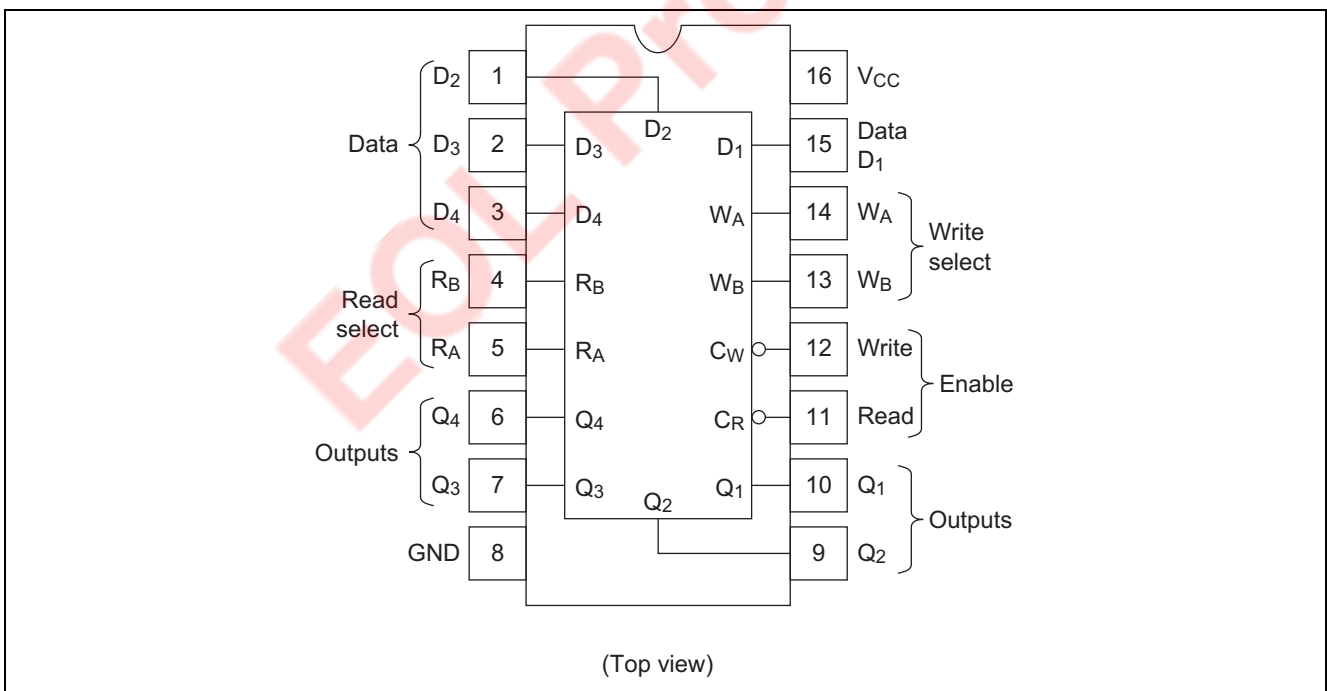
Z : high impedance (off)

(Q = D): The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

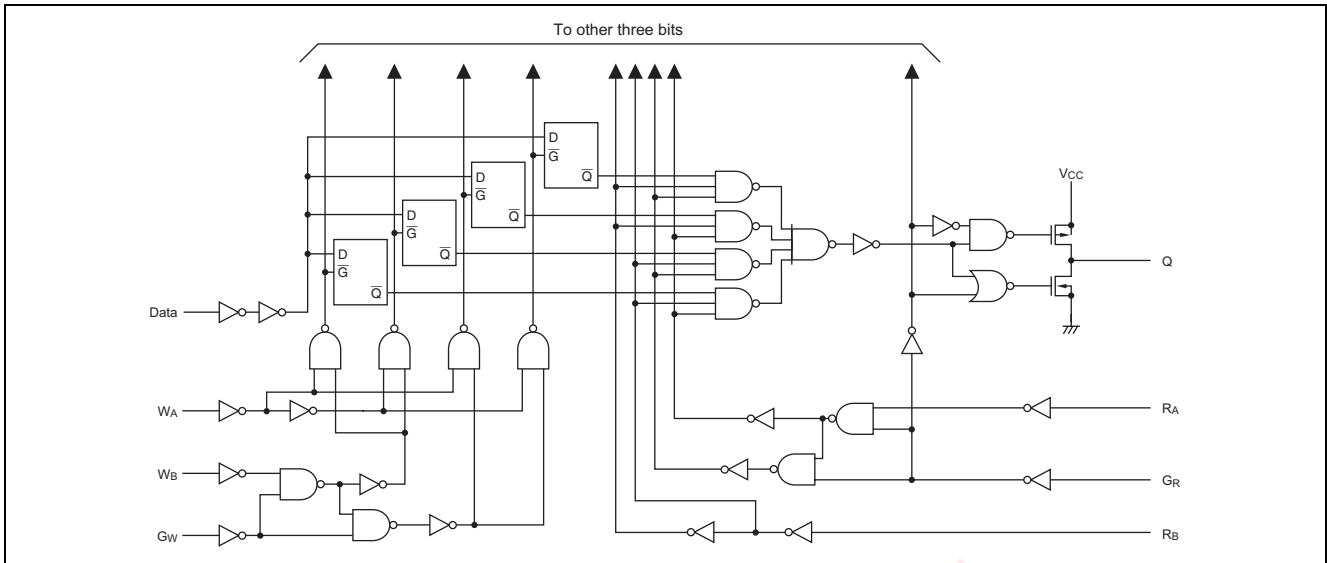
Q₀ : The level of Q before the indicated input conditions were established.

W₀ B₁ : The first bit of word 0, etc.

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	$^{\circ}C$	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0 V$
		0 to 500		$V_{CC} = 4.5 V$
		0 to 400		$V_{CC} = 6.0 V$

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

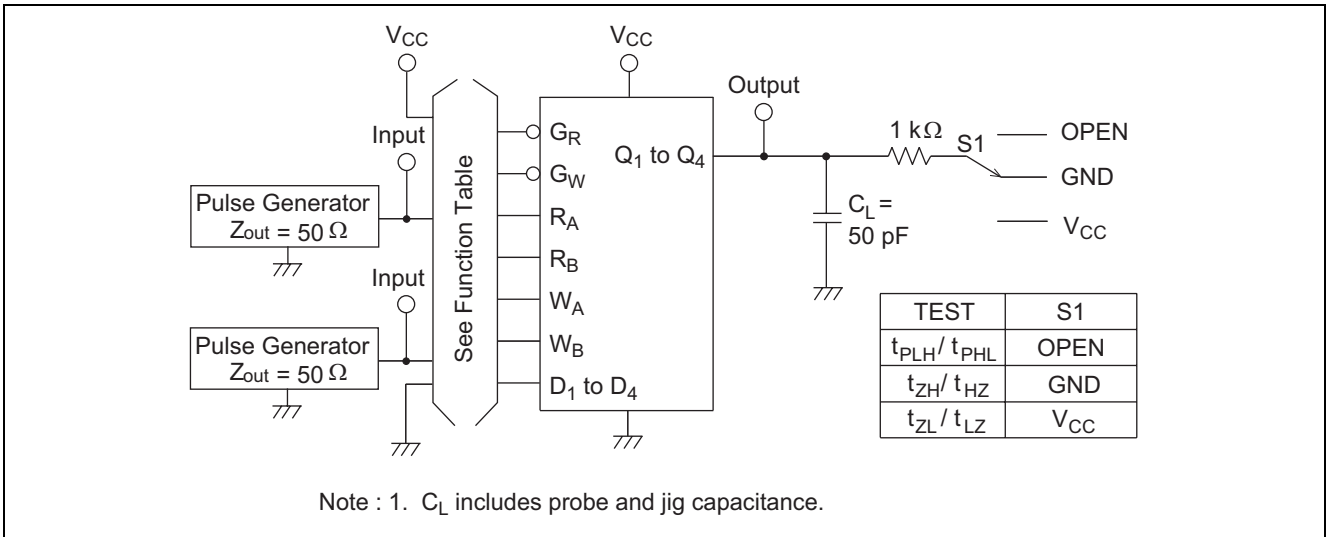
Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V _{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	V _{in} = V _{IH} or V _{IL}	I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -6 mA	
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -7.8 mA	
		4.5	4.18	—	—	4.13	—				
		6.0	5.68	—	—	5.63	—				
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	V _{in} = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33				I _{OL} = 6 mA
		6.0	—	—	0.26	—	0.33				I _{OL} = 7.8 mA
Off-state output current	I _{oz}	6.0	—	—	±0.5	—	±5.0	μA	V _{in} = V _{IN} or V _{IL} , V _{out} = V _{CC} or GND		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	V _{in} = V _{CC} or GND		
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	V _{in} = V _{CC} or GND, I _{out} = 0 μA		

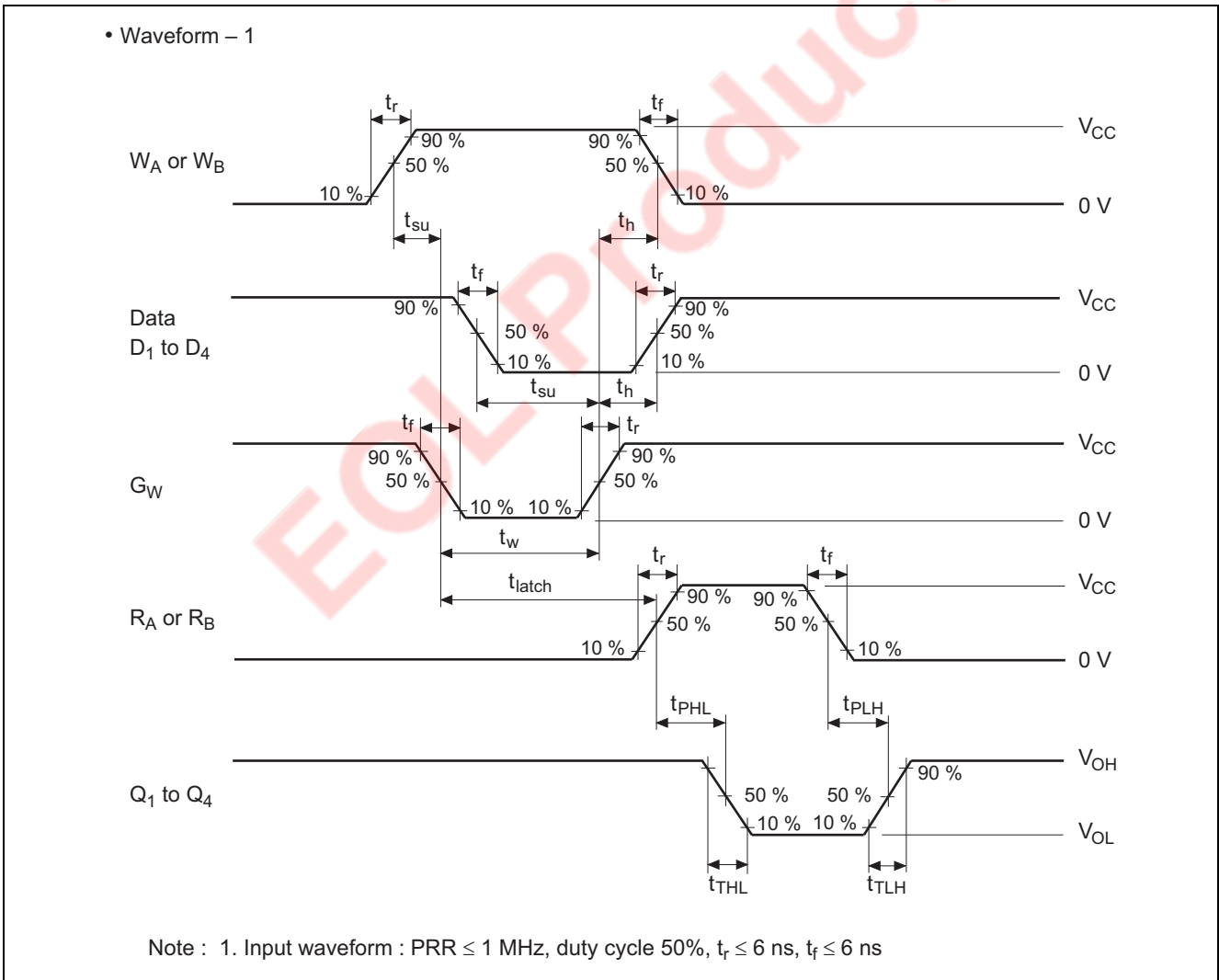
Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t_{PLH}	2.0	—	—	160	—	200	ns	Read select to Q
		4.5	—	21	32	—	40		
		6.0	—	—	27	—	34		
	t_{PHL}	2.0	—	—	200	—	250	ns	Write enable to Q
		4.5	—	24	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	150	—	190	ns	Data to Q
		4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
		4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	60	—	—	75	—	ns	Data to Write enable
		4.5	12	4	—	15	—		
		6.0	10	—	—	13	—		
		2.0	60	—	—	75	—	ns	Write select to Write enable
		4.5	12	—	—	15	—		
		6.0	10	—	—	13	—		
Hold time	t_h	2.0	50	—	—	63	—	ns	Write enable to Data
		4.5	10	6	—	13	—		
		6.0	9	—	—	11	—		
		2.0	50	—	—	63	—	ns	Write enable to Write select
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		
Latch time for new data	t_{latch}	2.5	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

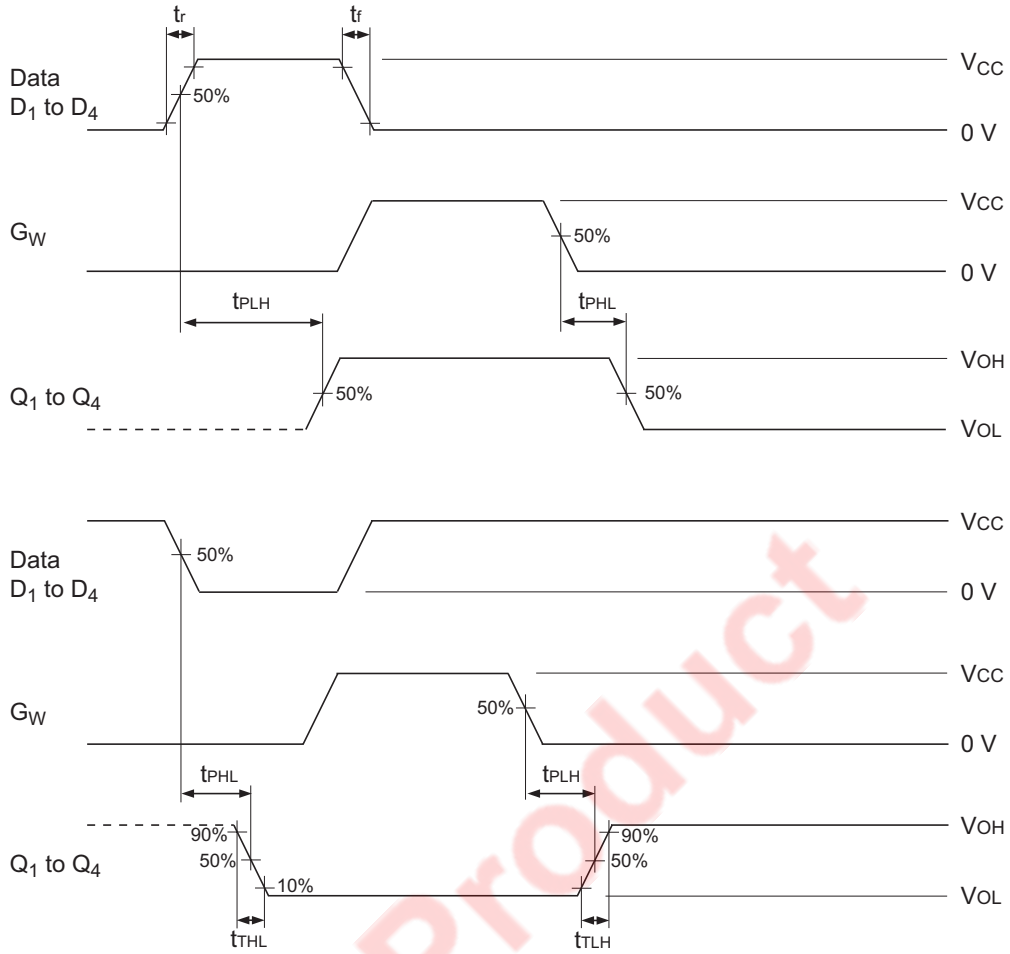
Test Circuit



Waveforms

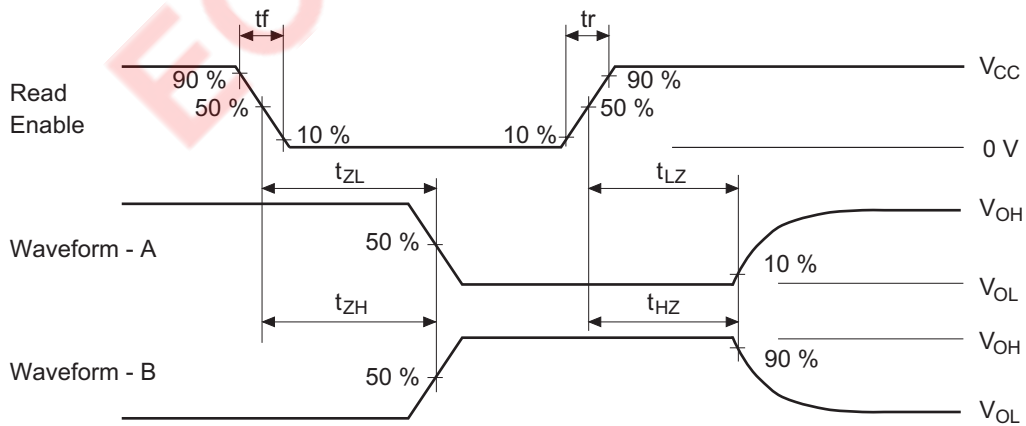


• Waveform – 2



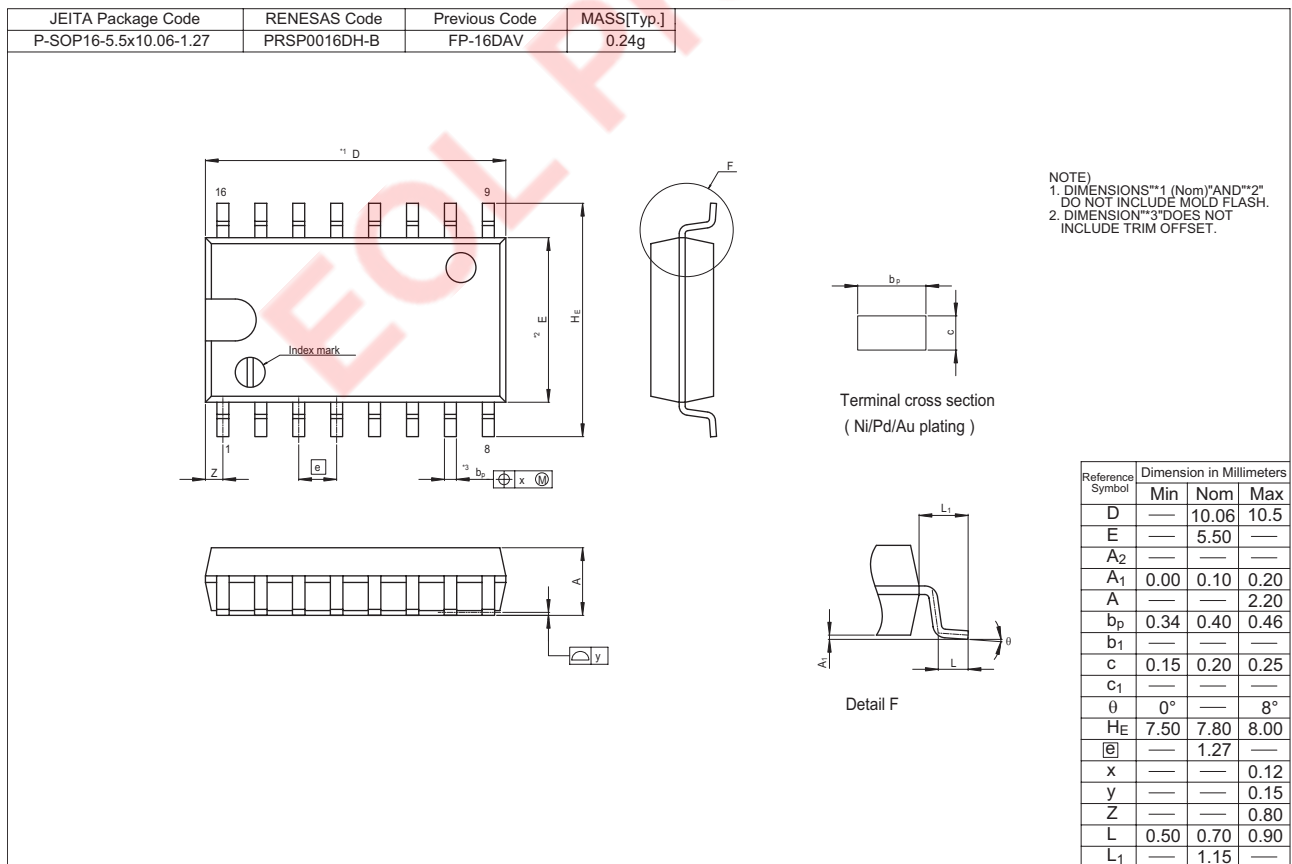
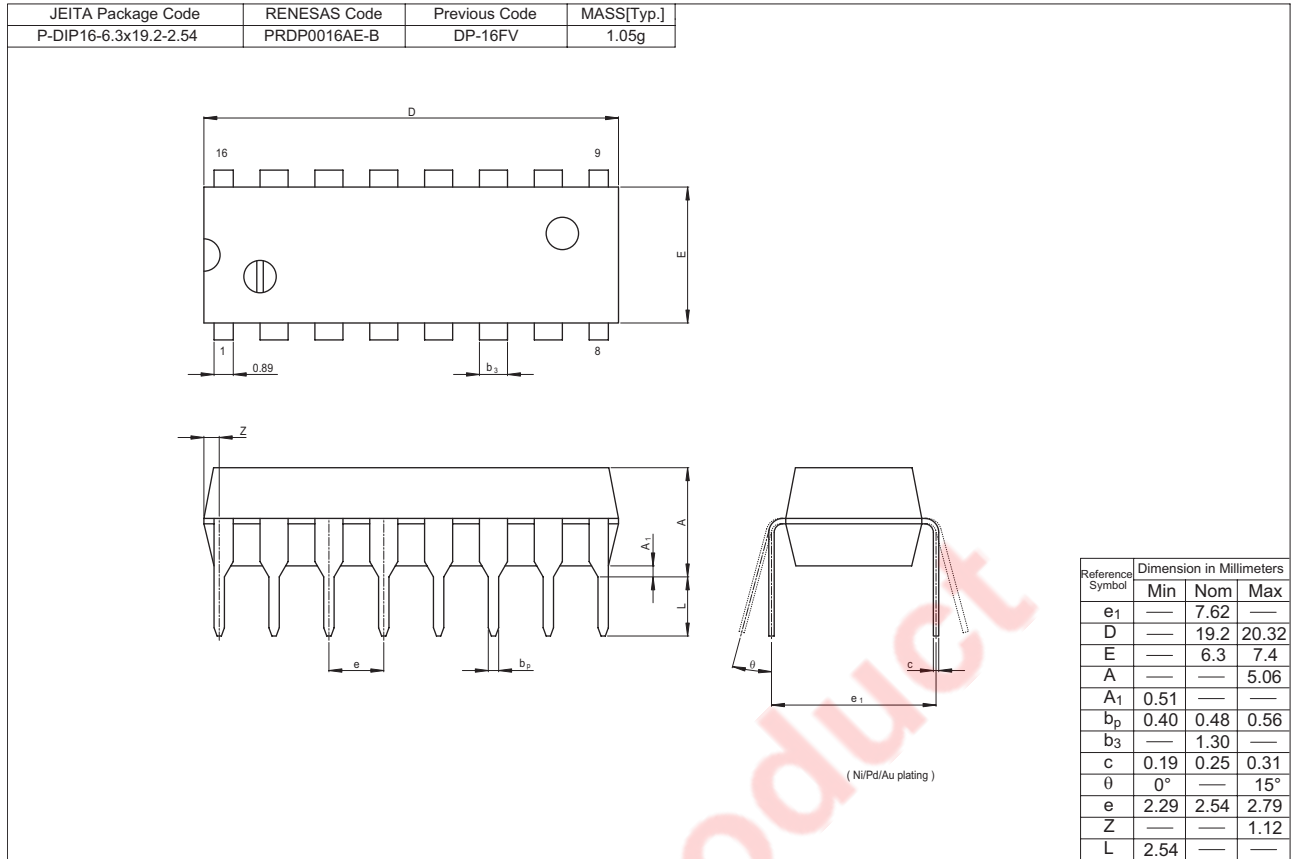
Note : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns

• Waveform – 3



- Notes : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns
- 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
- 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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