

2020

MotorComm

YT8511C YT8511H

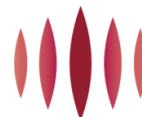
Datasheet

INTEGRATED 10/100/1000 GIGABIT ETHERNET TRANSCEIVER

REV V1.09

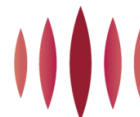
Revision History

| Revision | Release Date | Summary |
|----------|--------------|--|
| 0.1 | | Draft |
| 1.0 | 2019/07/15 | Update register |
| 1.01 | 2019/8/1 | Modify power related pins description |
| 1.02 | 2019/10/09 | Modify Pin description mistakes |
| 1.03 | 2019/12/06 | Update Register table |
| 1.04 | 2019/12/24 | Update LED related Register |
| 1.05 | 2020/01/13 | Modify Pin description Update power on sequence Update Power consumption |
| 1.06 | 2020/02/13 | Modify clock register ext reg 0x0c |
| 1.07 | 2020/02/18 | |
| 1.08 | 2020/03/09 | Modify the default value of extended register 0x37, 0x80, 0xb8, 0xb9, 0xba, 0xbb. Modify package information, ordering information, Add crystal/external clock requirement |
| 1.09 | 2020/03/10 | Official Release |

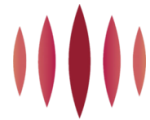


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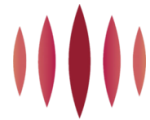
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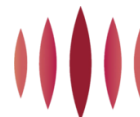
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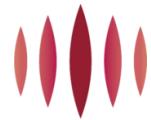
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1. GENERAL DESCRIPTION

The MotorComm YT8511C YT8511H is a triple-speed 10/100/1000BASE-T Gigabit Ethernet (GbE) Ethernet physical layer transceiver (PHY). Ideally suited for a wide range of industry applications, it is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a on Category 5 unshielded twisted-pair (UTP) cabling.

Based on cutting-edge DSP technology, combining adaptive equalizers, echo canceller, phase-locked, ADCs, phase-locked loops, line drivers, encoders/decoders, echo cancelers and all other required support circuitry at a Gigabit data rate to achieve robust performance and exceed automotive electromagnetic interference (EMI) requirements in severe environments with very low power dissipation.

The YT8511C YT8511H is designed to be fully compliant with RGMII interface specifications, allowing compatibility with standard Ethernet media access controllers (MACs) and switch controllers.

The YT8511 delivers the most comprehensive technology solution required by industry operating temperature.

TARGET APPLICATIONS

- HDTV
- Gaming machines
- IP Cameras
- Printers
- LED wall

2. FEATURE

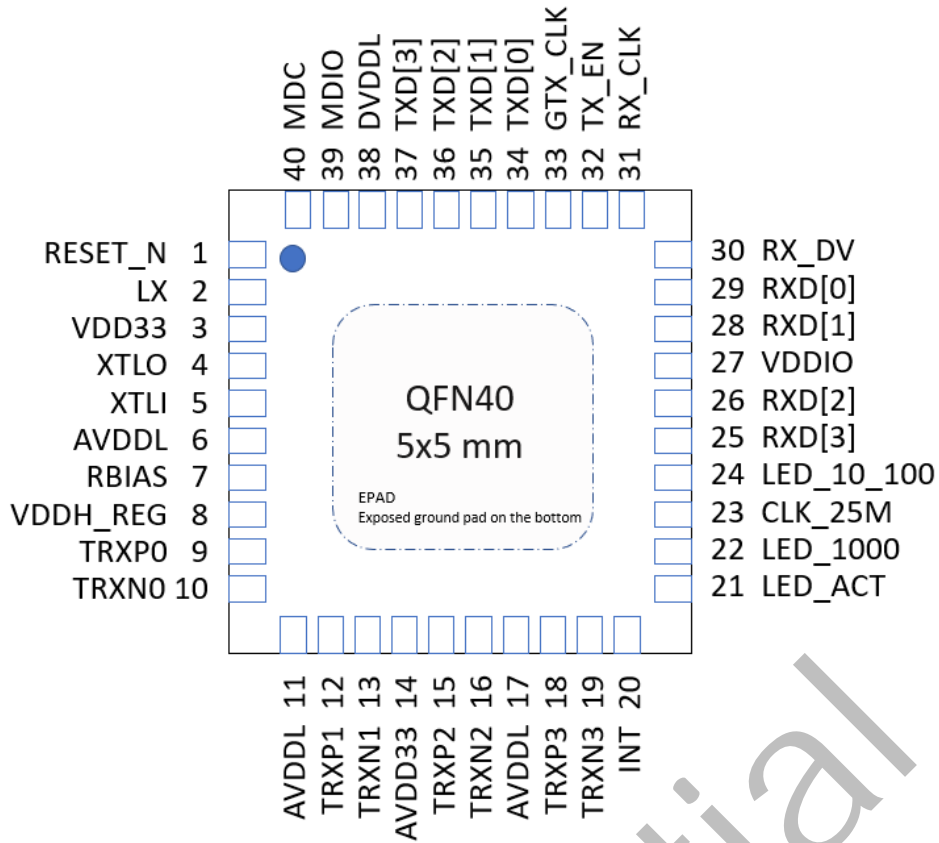
- 10BASE-T_e/100BASE-T_x/1000 BASE-T IEEE 802.3 compliant
- HYPER Range Supported, 4 pair HR-100 mode, enhance 100Mbps distance more than 400 meter
- Supports 1000 BASE-T PCS and auto-negotiation with next page support Supports RGMII interface to MAC devices with a broad I/O voltage level options 2.5V and is compatible with 3.3V I/O.
- RGMII timing modes support internal delay and external delay on Rx path
- Error-free operation up to 120 meters of CAT5e cable.
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Robust Cable Discharge Event (CDE)
- Jumbo Frame support up to 10KB (full duplex)
- All digital baseline wander correction Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Multiple Loopback modes for diagnostics

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3. PIN ASSIGNMENT

QFN40 5X5MM



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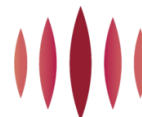
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3.2 PIN DESCRIPTIONS

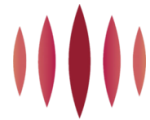
- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open-drain output
- OT = Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- CS = Continuously sampled
- ST = Schmitt trigger
- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = RGMII pin type
- A = Analog pin type

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| Symbol | Pin | Type | Description |
|---|-----------|---------------|--|
| MDI | | | |
| TRXP0, TRXN0 | 9 10 | IA, OA | Media-dependent interface 0, 100Ω transmission line |
| TRXP1, TRXN1 | 12, 13 | IA, OA | Media-dependent interface 1, 100Ω transmission line |
| TRXP2, TRXN2 | 15, 16 | IA, OA | Media-dependent interface 2, 100Ω transmission line |
| TRXP3, TRXN3 | 18, 19 | IA, OA | Media-dependent interface 3, 100Ω transmission line |
| RGMII | | | |
| GTX_CLK | 33 | I, PD | RGMII transmit clock, 125/25/2.5 MHz digital. Adding a 22ohm damping resistor is recommended for EMI design near MAC side. |
| RX_CLK | 31 | I/O, PD | 125MHz digital, adding a 22ohm damping resistor is recommended for EMI design near PHY side. |
| RX_DV | 30 | I/O, PD | RGMII receive data valid |
| RXD[0] | 29 | I/O, PD | RGMII received data 0 |
| RXD[1] | 28 | I/O, PD | RGMII received data 1 |
| RXD[2] | 26 | I/O, PD | RGMII received data 2 |
| RXD[3] | 25 | I/O, PD | RGMII received data 3 |
| TX_EN | 32 | I, PD | RGMII transmit enable |
| TXD[0] | 34 | I, PD | RGMII transmit data 0 |
| TXD[1] | 35 | I, PD | RGMII transmit data 1 |
| TXD[2] | 36 | I, PD | RGMII transmit data 2 |
| TXD[3] | 37 | I, PD | RGMII transmit data 3 |
| MANAGEMENT INTERFACE AND INTERRUPT | | | |
| MDC | 40 | I, PU | Management data clock reference |
| MDIO | 39 | I/O, D, PU | Management data, pull-up resistor to 3.3V/2.5V |
| INT | 20 | I/O, D, PD | Interrupt Signal to System; default OD-gate, needs an external pull up resistor |
| LED | | | |



| | | | |
|--------------------------------------|----------------|------------|---|
| LED_ACT | 21 | I/O, PU | Parallel LED output for 10/100/1000 BASE-T activity, active blinking. LED active based upon power-on strapping. If pulled up, active low, if pulled down, active high |
| LED_1000 | 22 | I/O, PU | Parallel LED output for 1000 BASE-T link, LED active based upon power-on strapping. |
| LED_10_100 | 24 | I/O, PU | Parallel LED output for 10/100 BASE-T link. |
| SYSTEM SIGNAL GROUP/REFERENCE | | | |
| CLK_25M | 23 | O, PD | 25 MHz clock output (default). It can be 125, 62.5 or 25 MHz clock output |
| RESET_N | 1 | I | System reset, active low. Requires an external pull-up resistor |
| XTLI | 5 | IA | Crystal oscillator input. Requires a capacitor to GND. Support external 25 MHz, 1.2V swing clock input through this pin. |
| XTLO | 4 | OA | Crystal oscillator output; add a capacitor to GND |
| RBIAS | 7 | OA | External 2.4 k ohm 1% to GND to set bias current |
| POWER | | | |
| LX | 2 | OA | Power inductor pin. Add an external 4.7 uH power inductor between this pin and pin 38. |
| VDDH_REG | 8 | OA | 3.3V or 2.5 V regulator output. A 1uF capacitor connected to GND. |
| VDDIO | 27 | IA | VDDIO input. Connect this pin to pin 8 (VDDH_REG) directly. |
| AVDDL | 6, 11 17 | P | 1.2 V analog power input. Connect to Pin 38 through a bead |
| DVDDL | 38 | P | 1.2 V digital core power input. Connect to power inductor and 10uF+0.1uF ceramic capacitors to GND |
| VDD33 | 3 | P | 3.3 V power for switching regulator |
| AVDD33 | 14 | P | Analog 3.3 V power input for PHY, from VDD33 through a bead |
| EPAD | - | | Exposed ground pad on back of the chip, tie to ground |

POWER ON STRAPPING

| PHY Pin | PHY Core Config | Description | Default |
|-------------------|--------------------------|--|---------|
| RXD0 | PHYADDRESS0 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 0 |
| RXD1 | PHYADDRESS1 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 0 |
| LED_ACT | PHYADDRESS2 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 1 |
| RX_DV | RGMII IO power selection | 0= RGMII IO 3.3V 1= RGMII IO 2.5V | 0 |
| RXD2 | PLLON selection | 0= PLL off in hibernation when cable unplugged 1= PLL on in hibernation when cable unplugged | 0 |
| LED_1000 | TEST Mode | 0=Test Mode only for internal use 1=Normal Mode, Must external pull up | 1 |
| RXD3 | Low Power Mode selection | 0= Force Low Power mode for shorter cable application 1= Normal cable application | 0 |
| LED_10_100 | RXC delay enable | 0= RXC delay disable 1= RXC delay enable | 1 |
| RX_CLK | clk 25m disable | 0= clk 25m output enable 1= clk 25m output disable | 0 |

NOTE: 0=Pull-down, 1=Pull-up

3 FUNCTION DESCRIPTION

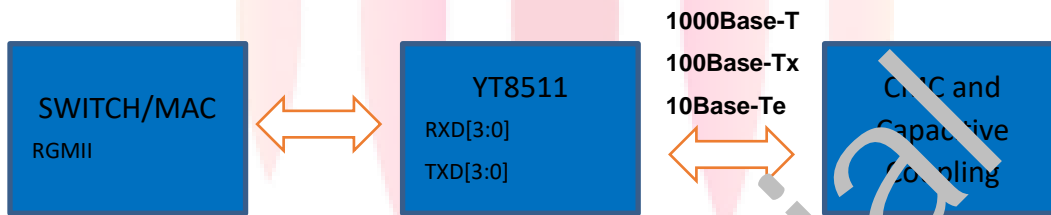
The YT8511 is MotorComm low cost GbE PHY. It is a highly integrated analog front end (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The YT8511 provides physical layer functions for half/full duplex 10 BASE-Te, 100 BASE-Tx and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

The YT8511 10/100/1000 PHY is fully 802.3ab compliant, and supports the reduced Gigabit Media-Independent Interface (RGMI) to connect to a Gigabit-capable MAC.

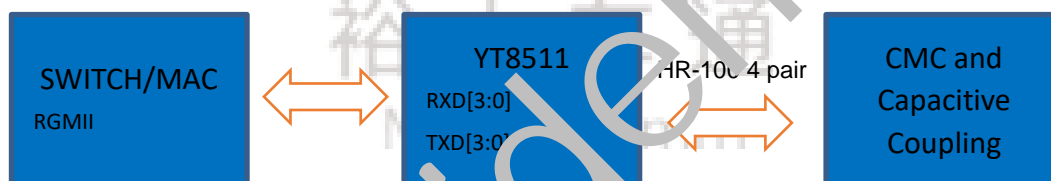
The YT8511 transceiver combines echo canceller, near end cross talk (NEXT) canceller, feed-forward equalizer, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

APPLICATION DIAGRAM

1000BASE-T/100BASE-TX/10BASE-TE APPLICATION



HYPER RANGE HR-100 4 PAIR APPLICATION



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TRANSMIT FUNCTIONS

TRANSMIT ENCODER MODES ENCODER MODE DESCRIPTION

1000 BASE-T

In 1000 BASE-T mode, the YT8511 scrambles transmit data bytes from the MAC interfaces to 8-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.

100 BASE-TX

In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

10 BASE-TE

In 10 BASE-Te mode, the YT8511 transmits and receives Manchester-encoded data.

RECEIVE FUNCTIONS

RECEIVE DECODER MODES

1000 BASE-T

In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

100 BASE-TX

IN 100 BASE-TX MODE, THE RECEIVED

data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.

10 BASE-TE

In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

HYPER RANGE

Hyper-range is the MotorComm proprietary mode in extended cable reach application up to 400m in 100M mode. HR-100 is 100Mbps Mode.

ECHO CANCELLER

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The YT8511 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

NEXT CANCELLER

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The YT8511 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The YT8511 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

BASELINE WANDER CANCELLER

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The YT8511 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

MANAGEMENT INTERFACE

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

AUTO-NEGOTIATION

The YT8511 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

- a) Speed: 10/100/1000Mbps
- b) Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

- a) Power-up/Hardware/Software reset
- b) Auto negotiation restart
- c) Transition from power-down to power up
- d) Link down

Auto negotiation is enabled for YT8511 by default, and can be disabled by software control.

LDS (LINK DISCOVERY SIGNALING)

YT8511 supports long range ethernet (LRE), which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

- a) Master/Slave assignment
- b) Estimate cable length
- c) Confirm pair number and pair connectivity ordering
- d) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy ethernet PHY, YT8511 can detect the standard NLP, FLP, MLT-3 IDLE signal, or 100BASE-T4 signal, and then transits LDS mode into Clause 28 auto negotiation mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link.

POLARITY DETECTION AND AUTO CORRECTION

YT8511 can detect and correct two types of cable errors: swapping of pairs within a UTP cable and swapping of wires within a pair.

EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4 OPERATIONAL DESCRIPTION

RESET

YT8511 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. After RESET_N is released, YT8511 latches input value on strapping pin which is used as configuration information which provides flexibility in application without mdio access. Detailed information please refer to pin description in table x(add index for table and figure).

YT8511 also provides two software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table. Configure bit 15 of lds mii register(address 0x0) or mii register(address 0x0) to 1 to enable software reset. These two bits are self-clear after reset process is done.

PHY ADDRESS

For YT8511, {LED_ACT, RXD[1:0]} is used to generate lower 3 bits of phy address. The upper 2 bits are always 0. So valid phy address is from 5'b00000 to 5'b00111.

YT8511 always response to phy address 0. Bit[6] of extended register(address 0x0) is enable control for phy address 0 and its default value is 1'b1. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0x0) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0x0) is enable control for broadcast phy address and its default value is 1'b1.

| PHY Pin | PHY Core Config | Description | Default |
|---------|-----------------|--|---------|
| RXD0 | PHYADDRESS0 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 0 |
| RXD1 | PHYADDRESS1 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 0 |
| LED_ACT | PHYADDRESS2 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00" | 1 |

RGMII INTERFACE

RGMII

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by tx_en/rx_dv on the falling edge of clock. TXD[3:0] and RXD[3:0] will be duplicated on both rising and falling edge of clock. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz.

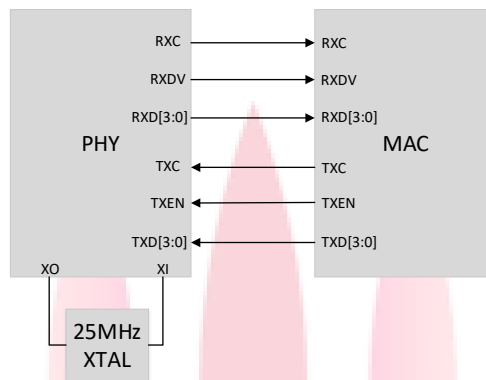


Figure . connection diagram of RGMII

LOOPBACK MODE

There are three loopback modes in YT8511.

DIGITAL LOOPBACK

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the YT8511 device.

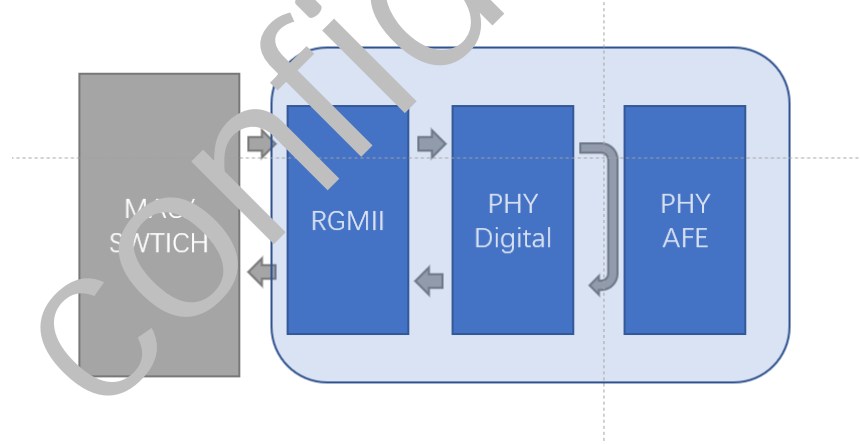


Figure . digital loopback

1000M loopback: write register 0x0 = 0x4140 to enable 1000M digital loopback.

100M loopback: write register 0x0 = 0x6100 to enable 100M digital loopback.

10M loopback: write register 0x0 = 0x4100 to enable 10M digital loopback.

EXTERNAL LOOPBACK

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

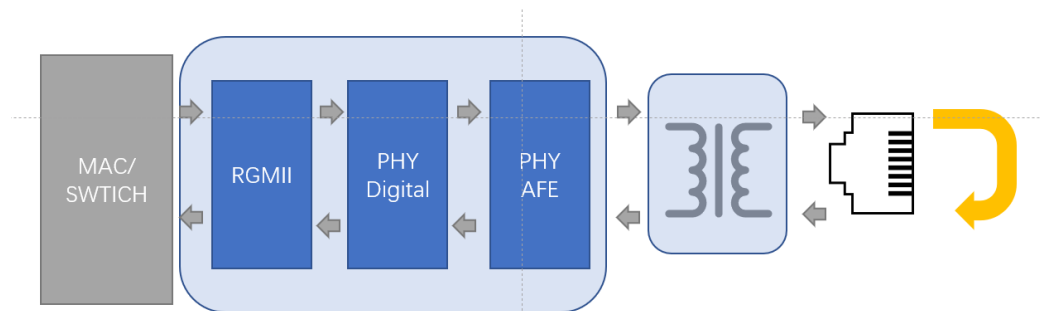


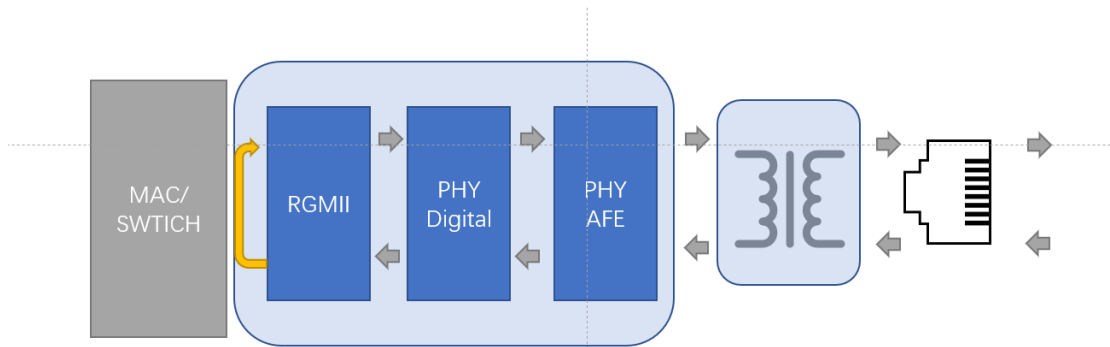
Figure . external loopback

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REMOTE PHY LOOPBACK

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.



MASTER-SLAVE CONFIGURATION

Master and slave configuration only exist in HR-100 mode.

Master and slave configuration is from lds negotiating result or in force mode, it comes from bit 3 of lds mii reg(address 0h0).

LED

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the register interface.

| Symbol | 10M link | 10M active | 100M link | 100M active | 1000M link | 1000M active |
|------------|----------|------------|-----------|-------------|------------|--------------|
| LED_10_100 | off | off | on | on | off | off |
| LED_1000 | off | off | off | off | on | on |
| LED_ACT | on | blink | on | blink | on | blink |

AUTO NEGOTIATION

When auto negotiation is enabled, YT8511 operation mode is based on the negotiation results, including speed and duplex mode. Registers configurations are shown as:

| Register Type | Register Address | Write Value | Comments |
|---------------|------------------|-------------|--------------------------------------|
| Extended | 16'h0100 | 16'h0006 | Bit2: 1'b1, Access IEEE MII regs |
| MII | 16'h0000 | | Bit12: 1'b1, enable auto negotiation |

Table: Enable auto negotiation

| Register Type | Register Address | Write Value | Comments |
|---------------|------------------|-------------|--------------------------------------|
| Extended | 16'h0100 | 16'h0006 | Bit2: 1'b1, Access IEEE MII regs |
| MII | 16'h0000 | | Bit9: 1'b1, restart auto negotiation |

Table: Restart auto negotiation

| Register Type | Register Address | Write Value | Comments |
|---------------|------------------|-------------|--|
| Extended | 16'h0100 | 16'h0006 | Bit2: 1'b1, Access IEEE MII regs |
| MII | 16'h0001 | | Bit5: 1'b1, AN complete; 1'b0, AN not complete Bit3: 1'b1, support AN; 1'b0, not support AN Bit2: 1'b1, Link up; 1'b0, link down |
| MII | 16'h0011 | | Bit15-14: 2'b00, 10Mbps; 2'b01: 100Mbps Bit1: 1'b1, link is downgrade; 1'b0, link is not downgrade |

Table: Auto negotiation status

When auto negotiation is disabled, forcing speed and duplex mode is also support. Forcing 10BASE-T has been discussed in the LDS part. Registers configuration for Forcing 100BASE-TX is shown as:

| Register Type | Register Address | Write Value | Comments |
|---------------|------------------|-------------|---|
| Extended | 16'h0100 | 16'h0006 | Bit2: 1'b1, Access IEEE MII regs |
| MII | 16'h0000 | | Bit12: 1'b0, disable auto negotiation Bit6,13: 2'b01, 100Mbps Bit8: 1'b1, full duplex |

Table: Forcing 100BASE-TX

During auto negotiation, YT8511 supports automatic MDI crossover by detecting and correcting external crossover cable. If the link partner also supports automatic MDI crossover, only one device performs the crossover according to IEEE 802.3 Clause 40.4.4. YT8511 also supports forcing MDI/MDIX mode. Registers configurations are shown as:

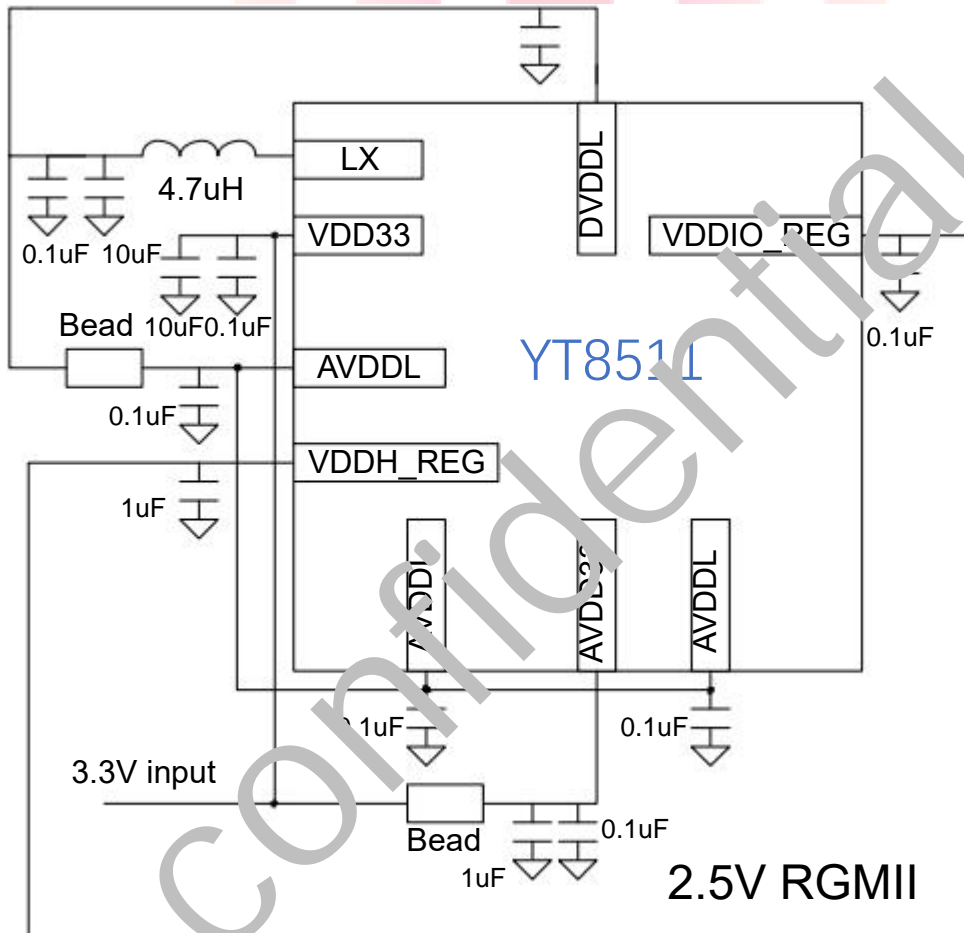
| Register Type | Register Address | Write Value | Comments |
|---------------|------------------|-------------|---|
| Extended | 16'h0100 | 16'h0006 | Bit2: 1'b1, Access IEEE MII regs |
| MII | 16'h0010 | | Bit6-5: 2'b00, forcing MDI; 2'b01, forcing MDIX; 2'b11, automatic MDI crossover |

Table: MDI/MDI-X configuration

POWER SUPPLIES

The YT8511 device requires only one external power supply: 3.3 V. Inside the chip there is a 3.3V rail, 2.5V rail, 1.2V rail.

YT8511 integrates a switch regulator which converts 3.3V to 1.2V at a high-efficiency for core power rail. (It is optional for an external regulator to provide this core voltage).



5 REGISTER OVERVIEW

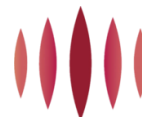
MII MANAGEMENT INTERFACE CLAUSE 22 REGISTER PROGRAMMING

The YT8511 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

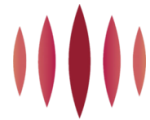
A clock of up to 25 MHz must drive the MDC pin of the YT8511. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

| Notation | Description |
|------------|--------------------------------|
| RW | Read and write |
| SC | Self-clear |
| RO | Read only |
| LH | Latch high |
| LL | Latch low |
| RC | Read clear |
| SWC | Clear to 0 when software reset |
| SWS | Set to 1 when software reset |
| CRW | Read and conditionally Write |
| POS | Power On Strapping |

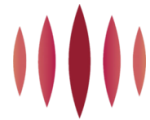


PHY MII REGISTER

| PHY MII 00H: BASIC CONTROL REGISTER 0X00 | | | | |
|--|----------------------|--------|---------|--|
| Bit | Symbol | Access | Default | Description |
| 15 | Reset | RW SC | 0x0 | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset |
| 14 | Loopback | RW SWC | 0x0 | Internal loopback control 1'b0: disable loopback 1'b1: enable loopback |
| 13 | Speed_Selection(LSB) | RW | 0x0 | LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0] Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 12 to zero. 1'b11 = Reserved 1'b10 = 1000Mb/s 1'b01 = 100Mb/s 1'b00 = 10Mb/s |
| 12 | Autoneg_En | RW | 0x1 | 1: to enable auto-negotiation; 0: auto-negotiation is disabled. |
| 11 | Power_down | RW SWC | 0x0 | 1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even |



| | | | | |
|---|----------------------|--------------|-----|--|
| | | | | bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user. |
| 10 | Isolate | RW SWC | 0x0 | Isolate phy from RGMII/SGMII/FIBER. 1'b0: Normal mode 1'b1: Isolate mode |
| 9 | Re_Autoneg | RW SC SWS | 0x0 | Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation |
| 8 | Duplex_Mode | RW | 0x1 | The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] RESTART_AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex |
| 7 | Collision_Test | RW SWC | 0x0 | Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test |
| 6 | Speed_Selection(LSB) | RW | 0x1 | See bit13. |
| 5:0 | Reserved | RO | 0x0 | Reserved. Write as 0, ignore on read |
| PHY MII 01H: BASIC STATUS REGISTER 0X01 | | | | |



| Bit | Symbol | Access | Default | Description |
|-----|-------------------------|-----------|---------|--|
| 15 | 100Base-T4 | RO | 0x0 | PHY doesn't support 100BASE-T4 |
| 14 | 100Base-X_Fd | RO | 0x1 | PHY supports 100BASE-X_FD |
| 13 | 100Base-X_Hd | RO | 0x1 | PHY supports 100BASE-X_HD |
| 12 | 10Mbps_Fd | RO | 0x1 | PHY supports 10Mbps_Fd |
| 11 | 10Mbps_Hd | RO | 0x1 | PHY supports 10Mbps_Hd |
| 10 | 100Base-T2_Fd | RO | 0x0 | PHY doesn't support 100Base-T2_Fd |
| 9 | 100Base-T2_Hd | RO | 0x0 | PHY doesn't support 100Base-T2_Hd |
| 8 | Extended_Status | RO | 0x1 | Whether support EXTended status register in 0Fh 0: Not supported 1: Supported |
| 7 | Unidirect_Ability | RO | 0x0 | 1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established |
| 6 | Mf_Preamble_Suppression | RO | 0x0 | 1'b0: PHY will not accept management frames with preamble suppressed 1'b1: PHY will accept management frames with preamble suppressed |
| 5 | Autoneg_Complete | RO SWC | 0x0 | 1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed |

| | | | | |
|---|---------------------|--------------------|-----|---|
| 4 | Remote_Fault | RO RC SWC LH | 0x0 | 1'b0: no remote fault condition detected 1'b1: remote fault condition detected |
| 3 | Autoneg_Ability | RO | 0x1 | 1'b0: PHY not able to perform Auto-negotiation 1'b1: PHY able to perform Auto-negotiation |
| 2 | Link_Status | RO SWC LL | 0x0 | Link status 1'b0: Link is down 1'b1: Link is up |
| 1 | Jabber_Detect | RO RC SWC LH | 0x0 | 10Baset jabber detected. It would assert if TX activity lasts longer than 42ms. 1'b0: no jabber condition detected 1'b1: Jabber condition detected. |
| 0 | Extended_Capability | RO | 0x1 | To indicate whether support EXTended registers, to access from address register 12h and data register 1Fh 1'b0: Not supported 1'b1: Supported |

PHY MII 02H: PHY IDENTIFICATION REGISTER1 0X02

| Bit | Symbol | Access | Default | Description |
|------|--------|--------|---------|--|
| 15:0 | Phy_Id | RO | 0x0 | Bits 3 to 18 of the Organizationally Unique Identifier |

PHY MII 03H: PHY IDENTIFICATION REGISTER2 0X03

| Bit | Symbol | Access | Default | Description |
|-------|---------|--------|---------|---|
| 15:10 | Phy_Id | RO | 0x0 | Bits 19 to 24 of the Organizationally Unique Identifier |
| 9:4 | Type_No | RO | 0x10 | 6 bits manufacturer's type number |

| 3:0 | Revision_No | RO | 0xa | 4 bits manufacturer's revision number |
|---|--------------------|--------|---------|---|
| PHY MII 04H: AUTO-NEGOTIATION ADVERTISEMENT 0X04 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15 | NEXT_Page | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed.</p> <p>1 = Advertise 0 = Not advertised</p> |
| 14 | Ack | RO | 0x0 | Always 0. |
| 13 | Remote_Fault | RW | 0x0 | <p>1 = Set Remote Fault bit 0 = Do not set Remote Fault bit</p> |
| 12 | Extended_NEXT_Page | RW | 0x1 | <p>Extended nEXT page enable control bit</p> <p>1 = Local device supports transmission of extended next pages</p> |

| | | | | |
|----|------------------|----|-----|---|
| | | | | 0 = Local device does not support transmission of extended next pages. |
| 11 | Asymmetric_Pause | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>1 = Asymmetric_Pause 0 = No asymmetric_Pause</p> |
| 10 | Pause | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented</p> |

| | | | | |
|---|------------------------|----|-----|---|
| 9 | 100BASE-T4 | RO | 0x0 | <p>1 = Able to perform 100BASE-T4</p> <p>0 = Not able to perform 100BASE-T4</p> <p>Always 0</p> |
| 8 | 100BASE-TX_Full_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>1 = Advertise</p> <p>0 = Not advertise</p> |
| 7 | 100BASE-TX_Half_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by |

| | | | | |
|---|---------------------------|----|-----|---|
| | | | | <p>writing register 0x0 bit[11]</p> <ul style="list-style-type: none"> • Link goes down <p>1 = Advertise 0 = Not advertised</p> |
| 6 | 10BASE- Te_Full_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] <p>Link goes down 1 = Advertise 0 = Not advertised</p> |
| 5 | 10BASE- Te_Half_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] |

| | | | | <ul style="list-style-type: none"> • Link goes down 1 = Advertise 0 = Not advertised |
|--|------------------|-----------|---------|--|
| 4:0 | Selector_Field | RW | 0x1 | Selector Field mode. 00001 = IEEE 802.3 |
| PHY MII 05H: AUTO-NEGOTIATION LINK PARTNER ABILITY 0X05 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15 | 1000Base-X_Fd | RO SWC | 0x0 | Received Code Word Bit 15 1 = Link partner is capable of next page 0 = Link partner is not capable of next page |
| 14 | ACK | RO SWC | 0x0 | Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word 0 = Link partner has not received link code word |
| 13 | REMOTE_FAULT | RO SWC | 0x0 | Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault |
| 12 | RESERVED | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 12 |
| 11 | ASYMMETRIC PAUSE | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request |

| | | | | |
|----|----------------------------|-----------|-----|--|
| | | | | asymmetric pause |
| 10 | PAUSE | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation |
| 9 | 100BASE-T4 | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4 |
| 8 | 100BASE- TX_FULL_DUPLEX | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex 0 = Link partner does not support 100BASE-TX full duplex |
| 7 | 100BASE- TX_HALF_DUPLEX | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex |
| 6 | 10BASE- Te_FULL_DUPLEX | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex |

| 5 | 10BASE-Te_HALF_DUPLEX | RO SWC | 0x0 | Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex 0 = Link partner does not support 10BASE-Te half-duplex |
|--|---------------------------------------|--------------------|---------|---|
| 4:0 | SELECTOR_FIELD | RO SWC | 0x0 | Selector Field Received Code Word Bit 4:0 |
| PHY MII 06H: AUTO-NEGOTIATION EXPANSION REGISTER 0X06 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:5 | Reserved | RO | 0x0 | Reserved |
| 4 | Parallel Detection fault | RO RC SWC LH | 0x0 | 1 = Fault is detected 0 = No fault is detected |
| 3 | Link partner nEXT page able | RO SWC LH | 0x0 | 1 = Link partner supports NEXT page 0 = Link partner does not support next page |
| 2 | Local NEXT Page able | RO | 0x1 | 1 = Local Device supports NEXT Page 0 = Local Device does not Next Page |
| 1 | Page received | RO RC LH | 0x0 | 1 = A new page is received 0 = No new page is received |
| 0 | Link Partner Auto negotiation able | RO SWC | 0x0 | 1 = Link partner supports auto- negotiation 0 = Link partner does not support auto-negotiation |
| PHY MII 07H: AUTO-NEGOTIATION NEXT PAGE REGISTER 0X07 | | | | |
| Bit | Symbol | Access | Default | Description |

| | | | | |
|------|---------------------|----|-----|---|
| 15 | NEXT Page | RW | 0x0 | Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page |
| 14 | Reserved | RO | 0x0 | Transmit Code Word Bit 14 |
| 13 | Message page mode | RW | 0x1 | Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page |
| 12 | Ack2 | RW | 0x0 | Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message |
| 11 | Toggle | RO | 0x0 | Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message/Unformatted | RW | 0x1 | Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0. |

PHY MII 08H: AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER 0X08

| Bit | Symbol | Access | Default | Description |
|-----|-------------------|--------|---------|---|
| 15 | NEXT Page | RO | 0x0 | Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page |
| 14 | Reserved | RO | 0x0 | Received Code Word Bit 14 |
| 13 | Message page mode | RO | 0x0 | Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page |

| | | | | |
|------|--------------------|----|-----|---|
| 12 | Ack2 | RO | 0x0 | Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message |
| 11 | Toggle | RO | 0x0 | Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message/Unformatte | RO | 0x0 | Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0. |

PHY MII 09H: MASTER-SLAVE CONTROL REGISTER 0X09

| Bit | Symbol | Access | Default | Description |
|-------|-----------|--------|---------|--|
| 15:13 | Test mode | RW | 0x0 | The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test |

| | | | | |
|----|--|----|-----|---|
| | | | | 110, 111 = Reserved normal operation. |
| 12 | Master/Slave Manual configuration Enable | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration.</p> |
| 11 | Master/Slave configuration | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power |

| | | | | |
|----|-----------------|----|-----|--|
| | | | | <p>down to normal operation by writing register 0x0 bit[11]</p> <ul style="list-style-type: none"> • Link goes down <p>This bit is ignored if bit[12] is 0.</p> <p>1 = Manual configuration as MASTER</p> <p>0 = Manual configuration as SLAVE.</p> |
| 10 | Port Type | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>This bit is ignored if bit[12] is 1.</p> <p>1 = Prefer multi-port device (MASTER)</p> <p>0 = Prefer single port device (SLAVE)</p> |
| 9 | 1000BASE-T Full | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] |

| | | | | <ul style="list-style-type: none"> The port is switched from power down to normal operation by writing register 0x0 bit[11] Link goes down 1 = Advertise 0 = Not advertised |
|---|---------------------------------------|-----------------|---------|---|
| 8 | 1000BASE-T Half- | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> Software reset is asserted by writing register 0x0 bit[15] Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] The port is switched from power down to normal operation by writing register 0x0 bit[11] Link goes down 1 = Advertise 0 = Not advertised (default) |
| 7:0 | Reserved | RW | 0x0 | Write as 0, ignore on read. |
| <hr/> PHY MII 0AH: MASTER-SLAVE STATUS REGISTER 0X0A <hr/> | | | | |
| Bit | Symbol | Access | Default | Description |
| 15 | Master/Slave_cfg_error | RO SWC RH | 0x0 | <p>This register bit will clear on read, rising of MII 0.12 and rising of AN complete.</p> <p>1 = Master/Slave configuration fault detected</p> <p>0 = No fault detected</p> |
| 14 | Master/Slave Configuration Resolution | RO | 0x0 | <p>This bit is not valid unless register 0x1 bit5 is 1.</p> <p>1 = Local PHY configuration</p> |

| | | | | resolved to Master 0 = Local PHY configuration resolved to Slave |
|--|--|--------|---------|---|
| 13 | Local Receiver Status | RO | 0x0 | 1 = Local Receiver OK 0 = Local Receiver not OK |
| 12 | Remote Receiver | RO | 0x0 | 1 = Remote Receiver OK 0 = Remote Receiver not OK |
| 11 | Link Partner 1000Base-T Full Duplex Capability | RO | 0x0 | This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex |
| 10 | Link Partner 1000Base-T Half Duplex Capability | RO | 0x0 | This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000Base-T full duplex 0 = Link Partner does not support 1000Base-T full duplex |
| 9:8 | Reserved | RO | 0x0 | Reserved |
| 7:0 | Idle Error Count | RO RC | 0x0 | MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over. |
| PHY MII 0DH: MMD ACCESS CONTROL REGISTER 0X0D | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:14 | Function | RW | 0x0 | 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes |

| | | | | |
|--|------------------------|--------|---------|--|
| | | | | 11 = Data, post increment on writes only |
| 13:5 | Reserved | RO | 0x0 | Reserved |
| 4:0 | DEVAD | RW | 0x0 | MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7 |
| <hr/> | | | | |
| PHY MII 0EH: MMD ACCESS DATA REGISTER 0X0E | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:0 | Address data | RW | 0x0 | If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register. |
| <hr/> | | | | |
| PHY MII 0FH: EXTENDED STATUS REGISTER 0X0F | | | | |
| Bit | Symbol | Access | Default | Description |
| 15 | 1000BASE-X Full Duplex | RO | 0x0 | 1 = PHY supports 1000BASE-X Full Duplex 0 = PHY does not supports 1000BASE-X Full Duplex Always 0. |
| 14 | 1000BASE-X Half Duplex | RO | 0x0 | 1 = PHY supports 1000BASE-X Half Duplex. 0 = PHY does not support 1000BASE-X Half Duplex. Always 0 |
| 13 | 1000BASE-T Full Duplex | RO | 0x1 | 1 = PHY supports 1000BASE-T Full Duplex 0 = PHY does not supports |

| | | | | 1000BASE-T Full Duplex Always 1 |
|--|------------------------|--------|---------|---|
| 12 | 1000BASE-T Half Duplex | RO | 0x0 | 1 = PHY supports 1000BASE-T Half Duplex 0 = PHY does not support 1000BASE-T Half Duplex Always 0. |
| 11:0 | Reserved | RO | 0x0 | Reserved |
| PHY MII 10H: PHY SPECIFIC FUNCTION CONTROL REGISTER | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:7 | Reserved | RO | 0x0 | Reserved |
| 6:5 | Cross_md | RW | 0x3 | Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes |
| 4 | Reserved | RO | 0x0 | Reserved |
| 3 | Crs_on_tx | RW | 0x0 | This bit is effective in 10BASE-T half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving. |
| 2 | In_sqe_test | RW | 0x0 | 1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically |

| | | | | disabled in full-duplex mode regardless the setting in this bit. |
|---|---------------------------|--------|---------|--|
| 1 | En_pol_inv | RW | 0x1 | If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled |
| 0 | Dis_jab | RW | 0x0 | Jabber takes effect only in 10BASE-Te half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function |
| PHY MII 11H: PHY SPECIFIC STATUS REGISTER 0X11 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:14 | Speed_mode | RO | 0x0 | These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 13 | Duplex | RO | 0x0 | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex |
| 12 | Page Received real-time | RO | 0x0 | 1 = Page received 0 = Page not received |
| 11 | Speed and Duplex Resolved | RO | 0x0 | When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. |

| | | | | |
|-----|-----------------------|----|-----|---|
| | | | | 1 = Resolved 0 = Not resolved |
| 10 | Link status real-time | RO | 0x0 | 1 = Link up 0 = Link down |
| 9:7 | Reserved | RO | 0x0 | Reserved |
| 6 | MDI Crossover Status | RO | 0x0 | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. 1 = MDIX 0 = MDI |
| 5 | Wirespeed downgrade | RO | 0x0 | 1 = Downgrade 0 = No Downgrade |
| 4 | Reserved | RO | 0x0 | Reserved |
| 3 | Transmit Pause | RO | 0x0 | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled |
| 2 | Receive Pause | RO | 0x0 | This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for |

| | | | | |
|---|--------------------|----|-----|--|
| | | | | information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled |
| 1 | Polarity Real Time | RO | 0x0 | 1 = Reverted polarity 0 = Normal polarity |
| 0 | Jabber Real Time | RO | 0x0 | 1 = Jabber 0 = No jabber |

 PHY MII 12H: INTERRUPT MASK REGISTER 0X12

| Bit | Symbol | Access | Default | Description |
|------|---------------------------------|--------|---------|---|
| 15 | Auto-Negotiation Error INT mask | RW | 0x0 | 1 = Interrupt enable 0 = Interrupt disable |
| 14 | Speed Changed INT mask | RW | 0x0 | same as bit 15 |
| 13 | Duplex changed INT mask | RW | 0x0 | same as bit 15 |
| 12 | Page Received INT mask | RW | 0x0 | same as bit 15 |
| 11 | Link Failed INT mask | RW | 0x0 | same as bit 15 |
| 10 | Link Succeed INT mask | RW | 0x0 | same as bit 15 |
| 9:7 | reserved | RW | 0x0 | No used. |
| 6 | WOL INT mask | RW | 0x0 | same as bit 15 |
| 5 | Wirespeed downgrade INT mask | RW | 0x0 | same as bit 15 |
| 4:02 | Reserved | RW | 0x0 | Reserved |
| 1 | Polarity changed INT mask | RW | 0x0 | same as bit 15 |
| 0 | Jabber Happened INT mask | RW | 0x0 | same as bit 15 |

| PHY MII 13H: INTERRUPT MASK REGISTER 0X13 | | | | |
|---|----------------------------|--------|---------|---|
| Bit | Symbol | Access | Default | Description |
| 15 | Auto-Negotiation Error INT | RW | 0x0 | Error can take place when any of the following happens: <ul style="list-style-type: none"> • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place |
| 14 | Speed Changed INT | RW | 0x0 | 1 = Speed changed 0 = Speed not changed |
| 13 | Duplex changed INT | RW | 0x0 | 1 = duplex changed 0 = duplex not changed |
| 12 | Page Received INT | RW | 0x0 | 1 = Page received 0 = Page not received |
| 11 | Link Failed INT | RW | 0x0 | 1 = Phy link down takes place 0 = No link down takes place |
| 10 | Link Succeed INT | RW | 0x0 | 1 = Phy link up takes place 0 = No link up takes place |
| 9:07 | Reserved | RW | 0x0 | Reserved |
| 6 | WOL INT | RW | 0x0 | 1 = PHY received WOL magic frame. 0 = PHY didn't receive WOL magic frame |

| 5 | Wirespeed downgraded INT | RW | 0x0 | 1 = speed downgraded. 0 = Speed didn't downgrade. |
|--|--------------------------|--------|---------|--|
| 4:02 | Reserved | RW | 0x0 | Reserved |
| 1 | Polarity changed INT | RW | 0x0 | 1 = PHY reversed MDI polarity 0 = PHY didn't revert MDI polarity |
| 0 | Jabber Happened INT | RW | 0x0 | 1 = 10BaseT TX jabber happened 0 = 10BaseT TX jabber didn't happen Please refer to mii.1.1 Jabber_Detect. |
| PHY MII 14H: SPEED AUTO DOWNGRADE CONTROL REGISTER 0X14 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:12 | Reserved | RO | 0x0 | Reserved |
| 11 | En_mdio_latch | RW | 0x1 | 1 = To latch MII/MMD register's read out value during MDIO read 0 = Do not latch MII/MMD register's read out value during MDIO read |
| 10 | Start_autoneg | RW | 0x0 | Set it to cause PHY to restart auto-negotiation. |
| 9 | Reverse_autoneg | RW | 0x0 | 1 = reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s. 0 = normal autoneg direction |
| 8 | Dis_giga | RW | 0x0 | 1 = disable advertise Giga ability in autoneg; 0 = don't disable, so PHY advertises Giga ability based on MII register 0x9. |
| 7:6 | Reserved | RO | 0x0 | Reserved |

| | | | | |
|-----|-----------------------------------|-----------|-----|--|
| 5 | En_speed_downgrade | RW POS | 0x1 | When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update. This bit will be set to 1'b0 in UTP_TO_FIBER_FORCE and UTP_TO_FIBER_AUTO mode; else set to 1'b1, only take effect after software reset |
| 4:2 | Autoneg retry limit pre-downgrade | RW | 0x3 | If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. only take effect after software reset |
| 1 | Bp_autospd_timer | RW | 0x0 | 1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; only take effect after software reset 0 = not bypass the timer, then links that established but hold for less than 1.5s would still be taken as failure, autoneg retry counter will increase by 1. |
| 0 | Reserved | RO | 0x0 | Reserved |

PHY MII 15H: RX ERROR COUNTER REGISTER 0X15

| Bit | Symbol | Access | Default | Description |
|------|----------------|--------|---------|---|
| 15:0 | Rx_err_counter | RO | 0x0 | This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over. |

PHY MII 1EH: DEBUG REGISTER'S ADDRESS OFFSET REGISTER 0X1E

| Bit | Symbol | Access | Default | Description |
|--|-------------------------------------|--------|---------|--|
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7:0 | Extended Register Address Offset | RW | 0x0 | It's the address offset of the debug register that will be Write or Read |
| PHY MII 1FH: DEBUG REGISTER'S DATA REGISTER | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:0 | Extended Register Datas | RW | 0x0 | It's the data to be written to the debug register indicated by the address offset in register 0x1E, or the data read out from that debug register. |

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PHY EXTENDED REGISTER

| PHY EXT 00H: MS CONFIG DEBUG REGISTER 0X00 | | | | |
|--|--------------------------------|--------|---------|---|
| Bit | Symbol | Access | Default | Description |
| 7 | En_mii_deglitch | RW | 0x1 | set to 1 to enable rgmii clock deglitch feature |
| 6 | uldata_loopback | RW | 0x0 | when set to 1, upload data to rgmii when remote loopback is set |
| 5 | jumbo_enable | RW | 0x0 | set to 1 to enable jumbo packet transmit and receive |
| 0 | MS config for autoneg disabled | RW | 0x1 | Control the master/slave configuration when autoneg is disabled and MII register 0x9 Master/Slave Manual configuration Enable is 0. |

| PHY EXT 04H: MANUAL EEE ABILITY REGISTER 0X04 | | | | |
|---|-----------------|-----------|---------|---|
| Bit | Symbol | Access | Default | Description |
| 15 | EEE_nptx_ctrl | RW SWC | 0x1 | Transmission of EEE NEXT page control bit. |
| 14 | EEE_xnprx_ctrl | RW SWC | 0x0 | Reception of EEE NEXT pages control bit. |
| 13 | EEE_ability_cfg | RW SWC | 0x0 | 0 = for debug, force Local device to enable EEE ability; 1 = the auto-negotiation result decides if Local device enable EEE ability. |
| 12:0 | Reserved | RO | 0x0 | Reserved |

| PHY EXT 09H: 100BT EXTRA TEST MODE REGISTER 0X09 | | | | |
|--|-----------------|--------|---------|--|
| Bit | Symbol | Access | Default | Description |
| 12 | En_rgmii_crs | RW | 0x0 | set to 1 to enable rgmii crs pattern |
| 11 | En_rgmii_fd_crs | RW | 0x0 | set to 1 to enable rgmii crs pattern in full duplex mode |
| 10:8 | Reserved | RO | 0x0 | Reserved |
| 7 | Jitter_test | RW | 0x0 | Jitter test enable |
| 6 | Over_Shoot_Test | RW | 0x0 | Overshoot test enable |
| 5 | Dcd_test | RW | 0x0 | Duty cycle distortion test enable |
| 4:3 | Pmd_lpbk | RW | 0x0 | Bit 4: 100BT PMD loopback, loopback TX MLT-3 Encoder output to RX MLT-3 Decoder input; Bit 3: 100BT PMD loopback, loopback TX Scrambler output to RX Descrambler input. |
| 2:1 | Pma_lpbk | RW | 0x0 | Bit 2: 100BT PMA loopback, test Carrier Detect and Link Monitor |
| 0 | Pcs_lpbk | RW | 0x0 | 100BT PCS loopback, loopback the serial output of 4B5B encoder on TX side to the serial input of 5B4B decoder on RX side. |

| PHY EXT 0AH: 10BT DEBUG, LPBKSR REGISTER 0X0A | | | | |
|---|-------------|--------|---------|--|
| Bit | Symbol | Access | Default | Description |
| 15:11 | Reserved | RO | 0x0 | Reserved |
| 10 | En_10bt_idl | RW | 0x0 | 1 = In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC; For FPGA due to mdio control, this bit is set to 1'b0 0 = In 10BT, DAC will not be turn off. |

| | | | | |
|-----|-------------------|-----------|-----|--|
| 9 | Bt10_squelch_ctrl | RW | 0x1 | 1 = while receiving pulse_p/n toggle, bt10 carrier sense will be set even though link is no up; |
| 8:5 | Reserved | RW | 0x0 | Reserved |
| 4 | Ext_lpbk | RW | 0x0 | External loopback. |
| 3 | Lpbk_ctrl_10bt | RW SWC | 0x1 | Control the loopback depth in 10BT when MII register 0x0 bit14 loopback is set. 1 = deep Loopback mode 0 = shallow Loopback mode |
| 2:0 | Test_mode_10bt | RW SWC | 0x0 | Test_mode[2:0] is for 10BT test mode select: 3'b001: packet with all ones, 10MHz sine wave, For harmonic test. 3'b010: pseudo random, for TP_IDLE/Jitter/Differential Voltage test. 3'b011: normal link pulse only, 3'b100: 5MHz sin wave. Others: normal mode. |

PHY EXT 0CH: PHY CLOCK GATING REGISTER 0X0

| Bit | Symbol | Access | Default | Description |
|-------|---------------------|--------|---------|---|
| 12 | En_gate_rx_clk_gmii | RW | 0x0 | To enable gate phy rx_clk_gmii when phy is link down |
| 11 | En_output_clk | RW | 0x0 | enable debug clock output to rx_clk_rgmii pad |
| 10:08 | Clk_out_sel | RW | 0x0 | select which clock is out to rx_clk_rgmii pad. Clk_out_sel[2]: 1, adc clock is selected; 0, dac clock is selected. Clk_out_sel[1:0]: 2'b00, chn0 is selected; 2'b01, chn1 is selected; 2'b10, chn2 is selected; 2'b11, chn3 is selected |
| 7:04 | Tx_clk_delay_sel | RW | 0x5 | Tx Delay time = 150ps * N – 250ps N is the decimal value of bit[7:4]. |

| | | | | |
|------|-----------------|-----------|-----|---|
| | | | | Default value 5 means about 500 ps clock delay compared to txd_rgmii in typical corner.. |
| 3 | Clk_25m_disable | RW POS | 0x0 | set to 1 to disable clk 25m pad output |
| 2:01 | Clk_25m_sel | RW | 0x1 | select which clock is output to clk_25m pad 2'b00, 25m from pll; 2'b01, 25m from xtl; 2'b10: 62.5m from pll; 2'b11: 125m from pll |
| 0 | Rx_clk_delay_en | RW POS | 0x1 | set to 1 to enable 1.8ns delay (1000Mbps) 8ns delay (10/100Mbps) on rx_clk_rgmii |

| PHY EXT 0DH: DELAY AND DRIVER STRENGTH CFG REGISTER 0X0D | | | | |
|--|------------------|--------|---------|--|
| Bit | Symbol | Access | Default | Description |
| 15:12 | Txc_delay_sel_fe | RW | 0xf | select tx_clk_rgmii delay in chip which is used to latch txd_rgmii in 100B/10BTe mode. 150ps step. Default value 15 means about 2ns clock delay compared to txd_rgmii in typical corner. |
| 11:08 | Reserved | RW | 0xf | Reserved |
| 7:06 | Dr_mdio | RW | 0x0 | driver strength of mdio pad. 2'b11: strongest; 2'b00: weakest |
| 5:04 | Dr_rx_rgmii | RW | 0x3 | driver strength of rx_clk_rgmii ,rx_d and rx_ctl pad. 2'b11: strongest; 2'b00: weakest |
| 3:02 | Reserved | RO | 0x0 | Reserved |
| 1:0 | Dr_led | RW | 0x0 | driver strength of led pad. 2'b11: strongest; 2'b00: weakest |

| PHY EXT 27H: SLEEP CONTROL1 0X27 | | | | |
|----------------------------------|----------------|--------|---------|---|
| Bit | Symbol | Access | default | Description |
| 15 | En_sleep_sw | RW | 0x1 | 1 = enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer; |
| 14 | Pllon_in_slp | RO | 0x0 | 1 = keep PLL on in sleep mode; 0 = close PLL in sleep mode. |
| 13 | Slp_pulse_sw | RW | 0x1 | when PHY enter sleep, 1 = enable PHY to send out one pulse periodic; 0 = disable PHY to send pulse. |
| 12 | En_upd_afe_sbs | RW | 0x0 | When AFE control is changed, no matter it's triggered by sleep control logic or normal work mode change, 1 = Update AFE step by step; 0 = Update AFE at once. |
| 11:6 | Reserved | RO | 0x0 | Reserved |
| 5 | Sleeping | RO | 0x0 | status register. 1 = PHY is slpt; 0 = PHY is waked |
| 4 | Reserved | RO | 0x0 | Reserved |
| 3:0 | Slp_state | RO | 0x0 | FSM state of internal sleep control logic. |

| PHY EXT 2DH: EEE 1000B7 WAKE UP ROT TIMER 0X2D | | | | |
|--|---------------|--------|---------|--|
| Bit | Symbol | Access | default | Description |
| 15:0 | Eee_wake_time | RW | 0x80 | lpi_wake_timer in Spec. it's the expected time for the PHY to transition from the LPI mode to normal operation. The condition lpi_wake_timer_done becomes true upon timer expiration. For each transition of |

| | | | | lpi_wake_timer_done from false to true, the wake error counter MMD 3.22 shall be incremented. This timer shall have a period that does not exceed 16.5 μ s. |
|--|------------------|--------|---------|---|
| <hr/> | | | | |
| PHY EXT 2EH: EEE 100BT WAKE ERROR TIMER 0X2E | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Eee_wake_time_fe | RW | 0x370 | It's the timer threshold to identify that SNR is OK in 100BT EEE refresh or wake case. |

| <hr/> | | | | |
|--------------------------------------|-------------|--------|---------|---|
| PHY EXT 30H: EEE QUITE TIMER TH 0X30 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | quite_timer | RW | 0x29f5 | Quite timer for 802.3az. Spec is 20~24ms. Real timer = quite_timer * 20.48ns. Default is ~22ms. |

| <hr/> | | | | |
|--------------------------------|-------------------|--------|---------|-----------------------------------|
| PHY EXT 34H: EEE CONTROL2 0X34 | | | | |
| Bit | Symbol | Access | default | Description |
| 15 | bp_fast_link_down | RW | 0x1 | 1 = bypass fast link down feature |

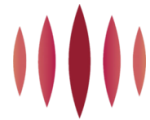
| <hr/> | | | | |
|--------------------------------------|------------|--------|---------|---|
| PHY EXT 36H: EEE 100BT CONTROL2 0X36 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:12 | Eee_idle_t | RW | 0x6 | lpi_rx_ti_timer in Spec. The minimum duration of received consecutive IDLE symbols before the receiver move to the Idle state. The timer shall have a period between 0.8 μ s and 0.9 μ s. |

| 11:8 | Eee_rxquiet_t | RW | 0x7 | lpi_rx_tq_timer in Spec. 100BT PCS RX counts the maximum duration the PHY stays in the Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure. The timer shall have a period between 24 ms and 26 ms. |
|--------------------------------------|-----------------|--------|---------|--|
| 7:0 | Eee_rxsleep_t | RW | 0x7a | lpi_rx_ts_timer in Spec, 100BT PCS RX counts the maximum duration the PHY is allowed to stay in the Sleep state before assuming a link failure. The timer shall have a period between 240 μ s and 260 μ s |
| PHY EXT 37H: EEE 100BT CONTROL3 0X37 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:13 | fld_timer_sel | RW | 0x1 | fast link down timer sel. 3'b000=0ms; 3'b001=5ms; 3'b010=10ms; 3'b011=20ms; 3'b100=40ms; 3'b101=80ms; 3'b110=160ms; 3'b111=320ms |
| 12:8 | Eee_lnk_fault_t | RW | 0x15 | lpi_lnk_fail_timer in Spec. This timer defines the maximum time allowed for the PHY between entry into the Wake state and subsequent entry into the Quiet, Sleep, or Idle states before assuming a link failure. The timer shall have a period between 90 μ s and 110 μ s. |
| 7 | Reserved | RW | 0x0 | Not used. |
| 6 | E_eee_rxmode | RW | 0x0 | To assert RX is active in 100BT EEE or not. |

| 5:0 | Eee_rxwake_t | RW | 0x14 | lpi_rx_tw_timer in Spec. It's the expected duration for the PHY to identify if valid SLEEP symbols for the Refresh state or valid IDLES for the Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer expires, the wake error counter as defined in MMD 3.22 shall be incremented. The timer shall have a period that does not exceed 20.5 μ s. |
|------------------------------|------------------|--------|---------|--|
| PHY EXT 38H: PKGEN CFG1 0X38 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:13 | Reserved | RO | 0x0 | Reserved |
| 12 | En_pkgen_da_sa | RW | 0x0 | |
| 11 | Pkgen_brdest | RW | 0x0 | |
| 10 | Pkgchk_txsrc_sel | RW | 0x0 | |
| 9 | Pkgen_en_az | RW | 0x0 | |
| 8:0 | Pkgen_in_az_t | RW | 0x1ff | |

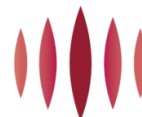
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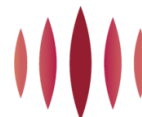
| PHY EXT 80H: VCT_CFG0 0X80 | | | | |
|----------------------------|---------------------|----------|---------|--|
| Bit | Symbol | Access | default | Description |
| 15:13 | Small_gap_th | RW | 0x4 | Small_gap_threshold[9:5]. |
| 12:10 | Vct_auto_gain_min | RW | 0x4 | It's the minimal AGC gain that the automatic AGC gain adjustment logic in VCT could reach in VCT test. |
| 9:4 | Vct_manu_gain | RW | 0x24 | The fixed AGC gain used during VCT test. It's valid only when en_vct_manu_gain is 1. |
| 3 | En_vct_manu_gain | RW | 0x1 | To using fixed AGC gain during VCT test. |
| 2 | En_gate_vct | RW | 0x0 | To enable clock gating of VCT module or not when vct_start is not asserted. 1, enable; 0, disable. |
| 1 | Vct_tlp_sel | RW | 0x1 | To send +1 or -1 symbol during VCT test. For FPGA, set it to 1 due to reversed dac polar. |
| 0 | En_vct | RW SC | 0x0 | At the rising edge of this bit, VCT test will start. |
| PHY EXT 81H: VCT_CFG1 0X81 | | | | |
| Bit | Symbol | Access | default | Description |
| 15 | En_chk_fe_found_cnt | RW | 0x1 | To enable to check the times that far-end echo was found during the VCT test. If the times that far-end echo was found is not bigger than the fe_found_cnt_th, the echo would be taken as invalid. |
| 14:10 | Fe_found_cnt_th | RW | 0x19 | See en_chk_fe_found_cnt. |
| 9:8 | Reserved | RW | 0x01 | Reserved |
| 7:0 | Busy_det_th | RW | 0x20 | The amplitude threshold to judge RX channel is not idle. During VCT RX |

| | | | | busy detection, if RX signals' amplitude is large than this threshold, RX channel will be treated as busy and VCT test will quit. |
|----------------------------|---------------------|--------|---------|--|
| <hr/> | | | | |
| PHY EXT 82H: VCT_CFG2 0X82 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:8 | Fecho_amp_th | RW | 0x1c | The amplitude threshold to judge far-end echo. During VCT far-end echo detection, the reflections larger than this will be treated as echoes. |
| 7:0 | Necho_amp_th | RW | 0x32 | The amplitude threshold to judge near-end echo. During VCT near-end echo detection, the reflections larger than this will be treated as echoes |
| <hr/> | | | | |
| PHY EXT 83H: VCT_CFG3 0X83 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:14 | Vct_manu_gain_necho | RW | 0x0 | |
| 13:8 | Num_pulse_intra | RW | 0x1e | |
| 7 | Tx_sin | RW | 0x0 | |
| 6 | Ignore_ne_found | RW | 0x0 | |
| 5 | Bp_ne_loc | RW | 0x0 | |
| 4 | Vct_fix_echo_dac | RW | 0x0 | |
| 3:0 | Vct_record_cfg | RW | 0x0 | To control debug register 0x8F~0x92 to record which case's VCT intermediate result. Vct_record_cfg[3:0] = {tx_pair, rx_pair}. For example, 4'b1001 means to record the VCT intermediate status of the case channel 2 transmit and channel 1 receive. |

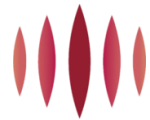


| PHY EXT 84H: VCT_MON0 0X84 | | | | |
|----------------------------|----------------|--------|---------|--|
| Bit | Symbol | Access | default | Description |
| 15 | Vct_in_process | RO | 0x0 | 1 = VCT test is still on-going. |
| 14:12 | Reserved | RO | 0x0 | Reserved |
| 11:8 | Mdi_busy | RO | 0x0 | 4 channel's MDI is busy or not while doing VCT test. |
| 7:6 | Self_st_3 | RO | 0x0 | Intra pair status of channel 3. |
| 5:4 | Self_st_2 | RO | 0x0 | Intra pair status of channel 2. |
| 3:2 | Self_st_1 | RO | 0x0 | Intra pair status of channel 1. |
| 1:0 | Self_st_0 | RO | 0x0 | Intra pair status of channel 0. |
| PHY EXT 85H: VCT_MON1 0X85 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:12 | Inter_st_3 | RO | 0x0 | Inter pair status between channel 3 and other three channels. |
| 11:8 | Inter_st_2 | RO | 0x0 | Inter pair status between channel 2 and other three channels. |
| 7:4 | Inter_st_1 | RO | 0x0 | Inter pair status between channel 1 and other three channels. |
| 3:0 | Inter_st_0 | RO | 0x0 | Inter pair status between channel 0 and other three channels. |
| PHY EXT 86H: VCT_MON2 0X86 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:12 | Inter_err_3 | RO | 0x0 | Error status while doing inter pair test between channel 3 and other three channels. |
| 11:8 | Inter_err_2 | RO | 0x0 | Error status while doing inter pair test between channel 2 and other three channels. |

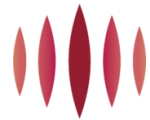
| | | | | |
|----------------------------|-----------------|--------|---------|--|
| 7:4 | Inter_err_1 | RO | 0x0 | Error status while doing inter pair test between channel 1 and other three channels. |
| 3:0 | Inter_err_0 | RO | 0x0 | Error status while doing inter pair test between channel 0 and other three channels. |
| <hr/> | | | | |
| PHY EXT 87H: VCT_MON3 0X87 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Self_dmg_loc_0 | RO | 0x0 | The intra pair damage location of channel 0. In unit cm. |
| <hr/> | | | | |
| PHY EXT 88H: VCT_MON4 0X88 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Self_dmg_loc_1 | RO | 0x0 | The intra pair damage location of channel 1. In unit cm. |
| <hr/> | | | | |
| PHY EXT 89H: VCT_MON5 0X89 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Self_dmg_loc_2 | RO | 0x0 | The intra pair damage location of channel 2. In unit cm. |
| <hr/> | | | | |
| PHY EXT 8AH: VCT_MON6 0X8A | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Self_dmg_loc_3 | RO | 0x0 | The intra pair damage location of channel 3. In unit cm. |
| <hr/> | | | | |
| PHY EXT 8BH: VCT_MON7 0X8B | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Inter_dmg_loc_0 | RO | 0x0 | The inter pair damage location of channel 0. In unit cm. |
| <hr/> | | | | |
| PHY EXT 8CH: VCT_MON8 0X8C | | | | |



| Bit | Symbol | Access | default | Description |
|----------------------------|-----------------|--------|---------|---|
| 15:0 | Inter_dmg_loc_1 | RO | 0x0 | The inter pair damage location of channel 1. In unit cm. |
| PHY EXT 8DH: VCT_MON9 0X8D | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Inter_dmg_loc_2 | RO | 0x0 | The inter pair damage location of channel 2. In unit cm. |
| PHY EXT 8EH: VCT_MONA 0X8E | | | | |
| Bit | Symbol | Access | default | Description |
| 15:0 | Inter_dmg_loc_3 | RO | 0x0 | The inter pair damage location of channel 3. In unit cm. |
| PHY EXT 8FH: VCT_MONB 0X8F | | | | |
| Bit | Symbol | Access | default | Description |
| 15:10 | Ne_loc_phs | RO | 0x0 | The phase index of the location of the near-end echo. |
| 9:0 | Ne_loc_cycle | RO | 0x0 | The location of the near-end echo, in unit of symbol cycle, which is 8ns. |
| PHY EXT 90H: VCT_MONC 0X90 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:10 | Fe_loc_phs | RO | 0x0 | The phase index of the location of the Far-end echo.. |
| 9:0 | Fe_loc_cycle | RO | 0x0 | The location of the Far-end echo, in unit of symbol cycle, which is 8ns |
| PHY EXT 91H: VCT_MOND 0X91 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:8 | Fe_max_amp | RO | 0x0 | The far-end echo's amplitude in last intermediate VCT test. |



| | | | | |
|-----------------------------|----------------|--------|---------|--|
| 7:0 | Ne_max_amp | RO | 0x0 | The near-end echo's amplitude in last VCT test. |
| <hr/> | | | | |
| PHY EXT 92H: VCT_MONE 0X92 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7 | ne_found | RO | 0x0 | near end echo is found |
| 6 | fe_found | RO | 0x0 | far end echo is found |
| 5:0 | Fe_found_cnt | RO | 0x0 | The times far-end echo was found in last intermediate VCT test. |
| <hr/> | | | | |
| PHY EXT 93H: VCT_MONF 0X93 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:14 | Reserved | RO | 0x0 | Reserved |
| 13:8 | Vct_used_agc_3 | RO | 0x0 | The AGC gain used for channel 3 while doing VCT and rx_pair=2'b11. |
| 7:6 | Reserved | RO | 0x0 | Reserved |
| 5:0 | Vct_used_agc_2 | RO | 0x0 | The AGC gain used for channel 2 while doing VCT and rx_pair=2'b10. |
| <hr/> | | | | |
| PHY EXT 94H: VCT_MON10 0X94 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:14 | Reserved | RO | 0x0 | Reserved |
| 13:8 | Vct_used_agc_1 | RO | 0x0 | The AGC gain used for channel 1 while doing VCT and rx_pair=2'b01. |
| 7:6 | Reserved | RO | 0x0 | Reserved |
| 5:0 | Vct_used_agc_0 | RO | 0x0 | The AGC gain used for channel 0 while doing VCT and rx_pair=2'b00. |
| <hr/> | | | | |
| PHY EXT 95H: VCT_CFG4 0X95 | | | | |
| Bit | Symbol | Access | default | Description |



| | | | | |
|----------------------------|----------------------|--------|---------|-------------|
| 15:6 | Expect_ne_loc | RW | 0x1c | |
| 5:0 | Num_pulse_inter | RW | 0xa | |
| <hr/> | | | | |
| PHY EXT 96H: VCT_CFG5 0X96 | | | | |
| Bit | Symbol | Access | default | Description |
| 15 | En_inter_small_th | RW | 0x1 | |
| 14:8 | Fecho_amp_th_small | RW | 0xf | |
| 7:4 | Inter_small_th | RW | 0xa | |
| 3:0 | Fecho_amp_th_tiny | RW | 0xa | |
| <hr/> | | | | |
| PHY EXT 97H: VCT_CFG6 0X97 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:8 | Fecho_amp_th_huge | RW | 0x6e | |
| 7:0 | Fecho_amp_th_big | RW | 0x50 | |
| <hr/> | | | | |
| PHY EXT 98H: VCT_CFG7 0X98 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:13 | Inter_small_th_small | RW | 0x5 | |
| 12:8 | Inter_small_th_hugh | RW | 0x1e | |
| 7:5 | Inter_small_th_tiny | RW | 0x5 | |
| 4:0 | Inter_small_th_big | RW | 0xa | |
| <hr/> | | | | |
| PHY EXT 99H: VCT_CFG8 0X99 | | | | |
| Bit | Symbol | Access | default | Description |
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7:6 | ADC_ver_cfg_vct | RW | 0x0 | |
| 5:4 | ADC_ref_l_cfg_vct | RW | 0x0 | |
| 3:0 | VGA_amp_gain_cfg_vct | RW | 0xf | |

| EXT B7H: LED GENERAL CONTROL | | | | |
|------------------------------|-----------------|--------|---------|--|
| Bit | Symbol | Access | default | Description |
| 15 | Col_blk_sel | RW | 1'b1 | 1 = when collision happens, LED blink at Blink Mode2 with higher frequency; |
| | | | | 0 = when collision happens, LED blink at Blink Mode1 with lower frequency; |
| 14 | Jabber_led_dis | RW | 1'b1 | 1 = when 10Mb/s Jabber happens, LED will not blink; |
| | | | | 0 = when 10Mb/s Jabber happens, LED will still blink if it's configured to blink on TX. |
| 13 | Lpbk_led_dis | RW | 1'b1 | 1 = In internal loopback mode, LED will not blink; |
| | | | | 0 = In internal loopback mode, LED will still blink if it's configured to blink on activity. |
| 12 | Dis_led_an_try | RW | 1'b0 | when auto-negotiation is at LINK_GOOD_CHECK status, |
| | | | | 1 = LED will be on; 0 = LED will be off. |
| 11:09 | Reserved | RO | 3'b0 | Not used. |
| 8 | Led_3_force_en | RW | 1'b0 | 1 = enable LED3 force mode. |
| 7:06 | Led_3_force_mod | RW | 2'b0 | Valid when bit5 is set. |
| | | | | 00 = force LED3 OFF; |
| | | | | 01 = force LED3 ON; |
| | | | | 10 = force LED3 to blink at Blink Mode1; |

| | | | | 11 = force LED3 to blink at Blink Mode2. |
|-----------------------|-------------------|--------|---------|---|
| 5 | Led_2_force_en | RW | 1'b0 | 1 = enable LED2 force mode. |
| 4:03 | Led_2_force_mode | RW | 2'b0 | Valid when bit5 is set. |
| | | | | 00 = force LED2 OFF; |
| | | | | 01 = force LED2 ON; |
| | | | | 10 = force LED2 to blink at Blink Mode1; |
| | | | | 11 = force LED2 to blink at Blink Mode2. |
| 2 | Led_1_force_en | RW | 1'b0 | 1 = enable LED1 force mode. |
| 1:00 | Led_1_force_mode | RW | 2'b0 | Valid when bit2 is set. |
| | | | | 00 = force LED1 OFF; |
| | | | | 01 = force LED1 ON; |
| | | | | 10 = force LED1 to blink at Blink Mode1; |
| | | | | 11 = force LED1 to blink at Blink Mode2. |
| <hr/> | | | | |
| EXT B8H: LED1 CONTROL | | | | |
| Bit | Symbol | Access | default | Description |
| 15:14 | Reserved | RO | 2'b0 | Not used. |
| 13 | Led_act_blk_ind_1 | RW | 1'b0 | When traffic is present, make LED1 BLINK no matter the previous LED status is ON or OFF, or make LED1 blink only when the previous LED is ON. |
| | | | | 1 = when bit10 and(or) bit9 are(is) 1 and copper link up and active, make LED1 to blink, no matter bit12~11 |

| | | | | |
|----|--------------------|----|------|---|
| | | | | <p>(duplex control) and bit6~4 (speed control) are 1 or 0;</p> <p>0 = when bit10 and(or) bit9 are(is) 1 and copper link up and active, make LED1 to blink only when one (more) of bit12~11 (duplex control) and bit6~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.</p> |
| 12 | Led_fdx_on_en_1 | RW | 1'b0 | <p>If BLINK status is not activated, when PHY link up and duplex mode is full duplex,</p> <p>1 = make LED1 ON;</p> <p>0 = don't make LED1 ON;</p> |
| 11 | Led_hdx_on_en_1 | RW | 1'b0 | <p>If BLINK status is not activated, when PHY link up and duplex mode is half duplex,</p> <p>1 = make LED1 ON;</p> <p>0 = don't make LED1 ON;</p> |
| 10 | Led_txact_blk_en_1 | RW | 1'b1 | <p>If bit12 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active,</p> <p>1 = make LED1 BLINK;</p> <p>0 = don't make LED1 BLINK.</p> |
| 9 | Led_rxact_blk_en_1 | RW | 1'b1 | <p>If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active,</p> <p>1 = make LED1 BLINK;</p> <p>0 = don't make LED1 BLINK.</p> |

| | | | | |
|---|-------------------|----|------|--|
| 8 | Led_txact_on_en_1 | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up and TX is active, make LED1 ON at least 10ms; |
| 7 | Led_rxact_on_en_1 | RW | 1'b0 | 1 = if BLINK status is not activated, when PHY link up and RX is active, make LED1 ON at least 10ms; |
| 6 | Led_gt_on_en_1 | RW | 1'b1 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 1000Base-T, make LED1 ON; |
| 5 | Led_ht_on_en_1 | RW | 1'b1 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 100Base_TX, make LED1 ON; |
| 4 | Led_bt_on_en_1 | RW | 1'b1 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 10Base-T, make LED1 ON; |
| 3 | Led_col_blk_en_1 | RW | 1'b0 | 1 = if PHY link up and collision happen, make LED1 BLINK; |
| 2 | Led_gt_blk_en_1 | RW | 1'b0 | 1 = if PHY link up and speed mode is 1000Base-T, make LED1 BLINK; |
| 1 | Led_ht_blk_en_1 | RW | 1'b0 | 1 = if PHY link up and speed mode is 100Base-T, make LED1 BLINK; |
| 0 | Led_bt_blk_en_1 | RW | 1'b0 | 1 = if PHY link up and speed mode is 10Base-T, make LED1 BLINK; |

EXT B9H: LED2 CONTROL

| Bit | Symbol | Access | default | Description |
|-------|--------------------|--------|---------|-----------------------------|
| 15:14 | Reserved | RO | 2'b0 | Not used. |
| 13 | Led_txact_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 12 | Led_fdx_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 11 | Led_rdx_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 10 | Led_txact_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |

| | | | | |
|---|--------------------|----|------|-----------------------------|
| 9 | Led_rxact_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 8 | Led_txact_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 7 | Led_rxact_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 6 | Led_gt_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 5 | Led_ht_on_en_2 | RW | 1'b1 | Same logic as LED1 control. |
| 4 | Led_bt_on_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 3 | Led_col_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 2 | Led_gt_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 1 | Led_ht_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |
| 0 | Led_bt_blk_en_2 | RW | 1'b0 | Same logic as LED1 control. |

EXT BAH: LED BLINK CONTROL

| Bit | Symbol | Access | default | Description |
|----------------------|------------|--------|---------|-----------------------------------|
| 15:12 | Reserved | RO | 4'b0 | Not used. |
| 11:09 | Duty_sel_2 | RW | 3'b0 | Select duty cycle of Blink Mode2. |
| | | | | 000 = 50% on 50% off; |
| | | | | 001 = 75% on 25% off; |
| | | | | 010 = 25% on 75% off; |
| | | | | 011 = 33% on 67% off; |
| | | | | 100 = 67% on 33% off; |
| | | | | 101 = 17% on 83% off; |
| | | | | 110 = 83% on 17% off; |
| 111 = 8% on 92% off. | | | | |
| 8:06 | Freq_sel_2 | RW | 3'b000 | Select frequency of Blink Mode2. |
| | | | | 000 = 2 Hz; 001 = 4Hz; |
| | | | | 010 = 8Hz; 011 = 16Hz; |
| | | | | 100 = 32Hz; 101 = 64Hz; |
| | | | | 110 = 128Hz; 111 = 256Hz. |

| | | | | |
|----------------------|------------|----|--------|-----------------------------------|
| 5:03 | Duty_sel_1 | RW | 3'b000 | Select duty cycle of Blink Mode1. |
| | | | | 000 = 50% on 50% off; |
| | | | | 001 = 75% on 25% off; |
| | | | | 010 = 25% on 75% off; |
| | | | | 011 = 33% on 67% off; |
| | | | | 100 = 67% on 33% off; |
| | | | | 101 = 17% on 83% off; |
| | | | | 110 = 83% on 17% off; |
| 111 = 8% on 92% off. | | | | |
| 2:00 | Freq_sel_1 | RW | 3'b110 | Select frequency of Blink Mode1. |
| | | | | 000 = 2 Hz; 001 = 4Hz; |
| | | | | 010 = 8Hz; 011 = 16Hz; |
| | | | | 100 = 32Hz; 101 = 64Hz; |
| | | | | 110 = 128Hz; 111 = 256Hz. |

EXT BBH: LED3 CONTROL

| Bit | Symbol | Access | default | Description |
|-------|--------------------|--------|---------|-----------------------------|
| 15:14 | Reserved | RO | 2'b0 | Not used. |
| 13 | Led_act_blk_ind_3 | RW | 1'b0 | Same logic as LED1 control. |
| 12 | Led_fdx_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 11 | Led_hdx_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 10 | Led_txact_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 9 | Led_rxact_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 8 | Led_txact_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 7 | Led_rxact_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 6 | Led_gt_on_en_3 | RW | 1'b1 | Same logic as LED1 control. |
| 5 | Led_mt_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 4 | Led_bt_on_en_3 | RW | 1'b0 | Same logic as LED1 control. |

| | | | | |
|---|------------------|----|------|-----------------------------|
| 3 | Led_col_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 2 | Led_gt_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 1 | Led_ht_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |
| 0 | Led_bt_blk_en_3 | RW | 1'b0 | Same logic as LED1 control. |

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PHY MMD1

| PHY MMD1 00H: PMA/PMD CONTROL 1 REGISTER 0X00 | | | | |
|---|-----------------|----------|---------|--|
| Bit | Symbol | Access | Default | Description |
| 15 | Pma_rst | RW SC | 0x0 | Setting this bit will set all PMA/PMD registers to their default states. This action also initiate a reset in MMD3 and MMD7. |
| 14:0 | Reserved | RO | 0x0 | Reserved |
| PHY MMD1 05H: PMA/PMD DEVICES IN PACKAGE 0X05 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7 | Autoneg_present | RO | 0x1 | 1= Auto-Negotiation present in package; 0= Auto-negotiation not present in package |
| 6:4 | Reserved | RO | 0x0 | Reserved |
| 3 | PCS_present | RO | 0x1 | 1= PCS present in package; 0= PCS not present in package. |
| 2 | Reserved | RO | 0x0 | Reserved |
| 1 | PMA_present | RO | 0x1 | 1= PMA present in package; 0= PMA not present in package. |
| 0 | MII_reg_present | RO | 0x1 | 1= Clause 22 registers present in package; 0= Clause 22 registers not present in package. |
| PHY MMD1 08H: PMA/PMD STATUS 2 REGISTER 0X08 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:14 | MMD1_present | RO | 0x2 | Always 2'b10. |

| | | | | |
|-------|------------------|----|-----|--|
| 13 | TX_fault_ability | RO | 0x0 | PMA/PMD does not have the ability to detect a fault condition on the transmit path. |
| 12 | RX_fault_ability | RO | 0x0 | PMA/PMD does not have the ability to detect a fault condition on the receive path. |
| 11:10 | Reserved | RO | 0x0 | Reserved |
| 9 | Extended_ability | RO | 0x0 | When read as a one, bit 1.8.9 indicates that the PMA/PMD has EXTended abilities listed in register 1.11. |
| 8:0 | Extra_abilities | RO | 0x0 | Reserved |

PHY MMD3

| Bit | Symbol | Access | Default | Description |
|--|-----------------|-----------|---------|--|
| PHY MMD3 00H: PCS CONTROL 1 REGISTER 0X00 | | | | |
| 15 | Pcs_rst | RW SC | 0x0 | Setting this bit will set all PCS registers to their default states. This action also initiate a reset in MMD1 and MMD7. |
| 14:11 | Reserved | RO | 0x0 | Reserved |
| 10 | Clock_stoppable | RW SWC | 0x0 | Not used. |
| 9:0 | Reserved | RO | 0x0 | Reserved |
| PHY MMD3 01H: PCS STATUS 1 REGISTER 0X01 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:12 | Reserved | RO | 0x0 | Reserved |
| 11 | Tx_lpi_rxd | RO LH | 0x0 | When read as 1, it indicates that the transmit PCS has received low power idle signaling one or |

| | | | | |
|--|------------------|----------|---------|--|
| | | | | more times since the register was last read. Lach High. |
| 10 | Rx_lpi_rxed | RO LH | 0x0 | When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Lach High. |
| 9 | Tx_lpi_indic | RO | 0x0 | When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals. |
| 8 | Rx_lpi_indic | RO | 0x0 | When read as 1, it indicates that the receive PCS is currently receiving low power idle signals. |
| 7:3 | Reserved | RO | 0x0 | Reserved |
| 2 | Pcsrx_Ink_status | RO LL | 0x0 | PCS status, latch low. |
| 1:0 | Reserved | RO | 0x0 | Reserved |
| <hr/> | | | | |
| PHY MMD3 05H: PCS DEVICES IN PACKAGE REGISTER 0X 5 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7 | Autoneg_present | RO | 0x1 | 1= Auto-Negotiation present in package; 0= Auto-negotiation not present in package |
| 6:4 | Reserved | RO | 0x0 | Reserved |
| 3 | PCS_present | RO | 0x1 | 1= PCS present in package; 0= PCS not present in package. |
| 2 | Reserved | RO | 0x0 | Reserved |
| 1 | PMA_present | RO | 0x1 | 1= PMA present in package; 0= PMA not present in package. |
| 0 | MII_reg_present | RO | 0x1 | 1= Clause 22 registers present in package; |

| | | | | 0= Clause 22 registers not present in package. |
|--|-------------------|-----------------|---------|---|
| <hr/> | | | | |
| PHY MMD3 08H: PCS DEVICES IN PACKAGE REGISTER 0X08 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:14 | MMD3_present | RO | 0x2 | Always 2'b10. |
| 13:0 | Reserved | RO | 0x0 | Reserved |
| <hr/> | | | | |
| PHY MMD3 14H: EEE CONTROL AND CAPABILITY REGISTER 0X14 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:3 | Reserved | RO | 0x0 | Reserved |
| 2 | 1000BASE-T EEE | RO | 0x1 | Always 1. EEE is supported for 1000BASE-T |
| 1 | 100BASE-TX EEE | RO | 0x1 | Always 1. EEE is supported for 100BASE-TX |
| 0 | Reserved | RO | 0x0 | Reserved |
| <hr/> | | | | |
| PHY MMD3 16H: EEE WAKE ERROR COUNTER 0X16 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:0 | Lpi_wake_err_cnt | RO RC SWC | 0x0 | Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. |

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PHY MMD7

| PHY MMD7 00H: AN CONTROL REGISTER 0X00 | | | | |
|---|----------|-----------|---------|---|
| Bit | Symbol | Access | Default | Description |
| 15 | An_rst | RW SC | 0x0 | Setting this bit will set all AN registers to their default states. This action also initiate a reset in MMD1 and MMD3. |
| 14 | Reserved | RO | 0x0 | Reserved |
| 13 | Xnp_ctrl | RW SWC | 0x1 | If mii register4 bit12 is set to 0, setting of this bit shall have no effect. 1 = Local device intends to enable the exchange of extended next page; 0 = Local device does not intend to enable the exchange of extended next page; |
| 12:0 | Reserved | RO | 0x0 | Reserved |
| PHY MMD7 01H: AN STATUS REGISTER 0X01 | | | | |
| Bit | Symbol | Access | Default | Description |
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7 | Xnp_ctrl | RW SWC | 0x0 | AN result of EXTended nEXT page. 1 = Extended Next Page format is used 0 = Extended Next Page is not allowed |
| 6:0 | Reserved | RO | 0x0 | Reserved |
| PHY MMD7 05H: AN DEVICES IN PACKAGE REGISTER 0X05 | | | | |
| Bit | Symbol | Access | Default | Description |

| | | | | |
|------|-----------------|----|-----|--|
| 15:8 | Reserved | RO | 0x0 | Reserved |
| 7 | Autoneg_present | RO | 0x1 | 1= Auto-Negotiation present in package; 0= Auto-negotiation not present in package |
| 6:4 | Reserved | RO | 0x0 | s |
| 3 | PCS_present | RO | 0x1 | 1= PCS present in package; 0= PCS not present in package. |
| 2 | Reserved | RO | 0x0 | Reserved |
| 1 | PMA_present | RO | 0x1 | 1= PMA present in package; 0= PMA not present in package. |
| 0 | MII_reg_present | RO | 0x1 | 1= Clause 22 registers present in package; 0= Clause 22 registers not present in package. |

PHY MMD7 3CH: LOCAL DEVICE EEE ABILITY 0X3C

| Bit | Symbol | Access | Default | Description |
|------|------------|-----------|---------|---------------------------|
| 15:3 | Reserved | RO | 0x0 | Reserved |
| 2 | EEE_1000BT | RW POS | 0x0 | PHY's 1000BT EEE ability. |
| 1 | EEE_100BT | RW POS | 0x0 | PHY's 100BT EEE ability. |
| 0 | Reserved | RO | 0x0 | Reserved |

PHY MMD7 3DH: LINK PARTNER EEE ABILITY 0X3D

| Bit | Symbol | Access | Default | Description |
|------|-------------------|--------|---------|------------------------------------|
| 15:3 | Reserved | RO | 0x0 | Reserved |
| 2 | LP_ge_eee_ability | RO | 0x0 | Link partner's 1000BT EEE ability. |
| 1 | LP_ge_eee_ability | RO | 0x0 | Link partner's 100BT EEE ability. |

| | | | | |
|---|----------|----|-----|----------|
| 0 | Reserved | RO | 0x0 | Reserved |
|---|----------|----|-----|----------|

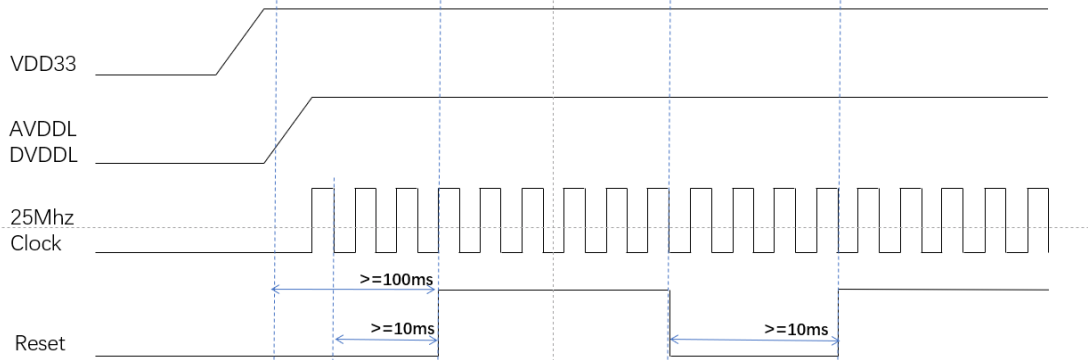
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6 TIMING AND AC CHARACTERISTICS

POWER ON SEQUENCE

Power On Sequence, Reset and Clock



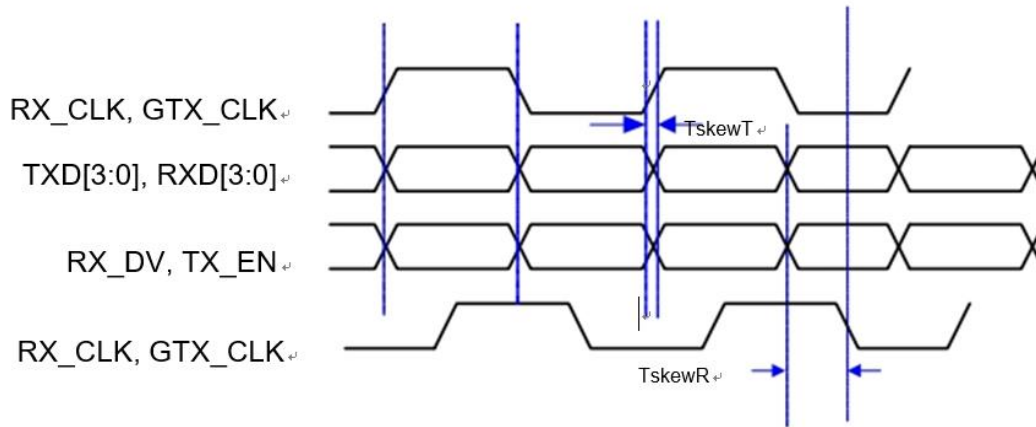
When using crystal, the clock is generated internally after power is stable.

For a reliable power on reset, suggest to keep asserting the reset low long enough (100ms) to ensure the clock is stable and clock-to-reset 10ms requirement is satisfied.

RGMI CHARACTERISTICS

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|------------------------------|-----------------------------------|------------------|---------|---------|-------------|-------|
| VDD33, AVDD33 | 3.3V Supply Voltage | - | 2.97 | 3.3 | 3.63 | V |
| 1. MDIO, MDC 2. RGMII I/O | 2.5V RGMII Supply Voltage | - | 2.25 | 2.5 | 2.75 | V |
| Voh (3.3V) | Minimum High Level Output Voltage | - | 2.7 | - | VDD33 + 0.3 | V |
| Voh (2.5V) | Minimum High Level Output Voltage | - | 2.0 | - | VDD25 + 0.3 | V |
| Vol (3.3V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| Vol (2.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| Vih (3.3V) | Minimum High Level Input Voltage | - | 2.0 | - | - | V |
| Vil (3.3V) | Maximum Low Level Input Voltage | - | - | - | 0.8 | V |
| Vih (2.5V) | Minimum High Level Input Voltage | - | 1.7 | - | - | V |
| Vil (2.5V) | Maximum Low Level Input Voltage | - | - | - | 0.7 | V |
| Iin | Input Current | Vin=VDD33 or GND | 0 | - | 0.5 | μA |

RGMII TIMING W/O DELAY

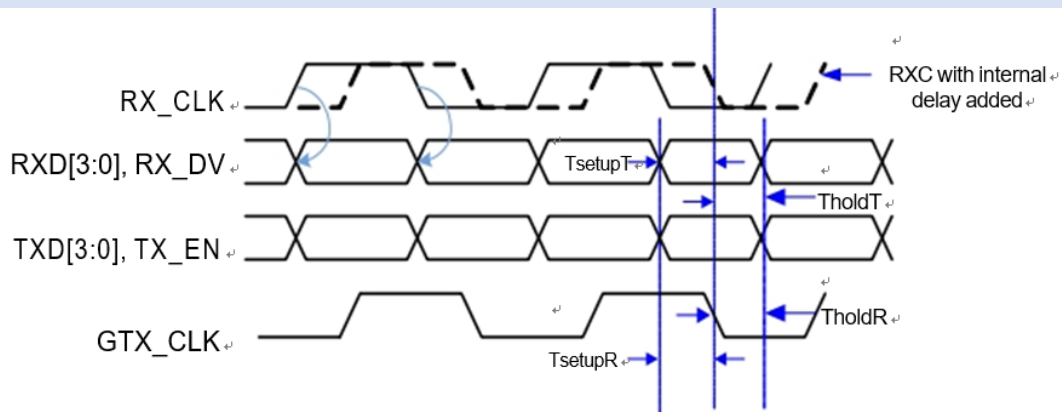


| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--|------|-----|------|------|
| T_{skewT} | Data to clock output skew (at Transmitter) | -500 | 0 | 500 | ps |
| T_{skewR} | Data to clock output skew (at Receiver) | 1 | — | — | ns |
| T_{cyc} | Clock cycle duration | 7.2 | 8.0 | 8.8 | ns |
| Duty_G | Duty cycle for Gigabit | 45 | 50 | 55 | % |
| Duty_T | Duty cycle for 10/100T | 40 | 50 | 60 | % |
| T_r/T_f | Rise/Fall time (20 - 80%) | — | — | 0.75 | ns |

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RGMII TIMING WITH INTERNAL DELAY



| Symbol | Parameter | Min | Typ | Max | Unit |
|---------|---|------|-----|-----|------|
| TsetupT | Data to Clock output Setup Time at Transmitter (with delay integrated at transmitter) | 1.65 | 2.0 | 2.2 | ns |
| TholdT | Clock to Data output Hold Time at Transmitter (with delay integrated at transmitter) | 1.65 | 2.0 | 2.2 | ns |
| TsetupR | Data to Clock input Setup Time at Receiver (with delay integrated at transmitter) | 1.0 | 2.0 | | ns |
| TholdR | Data to Clock output Setup Time at Receiver (with delay integrated at transmitter) | 1.0 | 2.0 | | ns |

MDIO

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---------------------|-----|-----|------|
| I _{IH} | Input high current | | 0.4 | mA |
| I _{IL} | Input low current | 0.4 | — | mA |
| V _{OH} | Output high voltage | 2.4 | — | V |
| V _{OL} | Output low voltage | — | 0.4 | V |
| V _{IH} | Input high voltage | 2.0 | — | V |
| V _{IL} | Input low voltage | — | 0.8 | V |

CRYSTAL REQUIREMENT

| Symbol | Description | Min | Typ | Max | Unit |
|-----------------|---------------------------------------|-----|-----|-----|------|
| F ref | Crystal Reference Frequency | - | 25 | - | MHz |
| F ref Tolerance | Crystal Reference Frequency tolerance | -50 | - | 50 | ppm |
| Duty Cycle | Reference clock input duty cycle | 40 | - | 60 | % |
| ESR | Equivalent Series Resistance | - | - | 50 | ohm |
| DL | Drive Level | - | - | 0.5 | mW |

OSCILLATOR/EXTERNAL CLOCK REQUIREMENT

| Parameter | Condition | Min | Typ | Max | Unit |
|---------------------|--------------|-----------|-----|-----------|------|
| Frequency | | | 25 | | MHz |
| Frequency tolerance | Ta= -40~85 C | -50 | | 50 | PPM |
| Duty Cycle | | 40 | - | 60 | % |
| Peak to Peak Jitter | | | | 200 | ps |
| Vih | | AVDDL-0.2 | | AVDDL+0.2 | V |
| Vil | | | | 0.4 | V |
| Rise Time | 10%~90% | | | 10 | ns |
| Fall Time | 10%~90% | | | 10 | ns |
| Temperature Range | YT8512H | -40 | | 85 | °C |
| Temperature Range | YT8512C | 0 | | 70 | °C |

7 POWER REQUIREMENTS

POWER REQUIREMENT

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|------------------------------|-----------------------------------|---------------------|---------|---------|-------------|-------|
| VDD33, AVDD33 | 3.3V Supply Voltage | - | 2.97 | 3.3 | 3.63 | V |
| 1. MDIO, MDC 2. RGMII I/O | 2.5V RGMII Supply Voltage | - | 2.25 | 2.5 | 2.75 | V |
| Voh (3.3V) | Minimum High Level Output Voltage | - | 2.4 | - | VDD33 + 0.3 | V |
| Voh (2.5V) | Minimum High Level Output Voltage | - | 2.0 | - | VDD25 + 0.3 | V |
| Vol (3.3V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| Vol (2.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| Vih (3.3V) | Minimum High Level Input Voltage | - | 2.0 | - | - | V |
| Vil (3.3V) | Maximum Low Level Input Voltage | - | - | - | 0.8 | V |
| Vih (2.5V) | Minimum High Level Input Voltage | - | 1.7 | - | - | V |
| Vil (2.5V) | Maximum Low Level Input Voltage | - | - | - | 0.7 | V |
| Iin | Input Current | Vin=VDD33 or GND | 0 | - | 0.5 | μA |

POWER CONSUMPTION (TYPICAL)

| MODE | | 3.3V Domain | | Power (mW) |
|------------|---------------|-------------|---------------|------------|
| | | VDD33(Pin3) | AVDD33(Pin14) | |
| Reset | | 3 | 12 | 47.2 |
| Sleep | | 2 | 6 | 24.1 |
| power down | | 3 | 12 | 48.8 |
| Active | normal unplug | 14 | 25 | 129.4 |
| | link 10M | 6 | 24 | 100.7 |
| | link 100M | 19 | 27 | 153.5 |
| | link 1000M | 118 | 75 | 633.6 |
| Traffic | link 10M | 7 | 31 | 125.7 |
| | link 100M | 19 | 29 | 158.4 |
| | link 1000M | 131 | 81 | 699.6 |

Using internal switching regulator, Inductor P/N:SLW3012S4R7MST DCR=0.12ohm

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8 MECHANICAL AND THERMAL

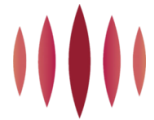
ROHS-COMPLIANT PACKAGING

Motor-comm offers an RoHS package that is compliant with RoHS

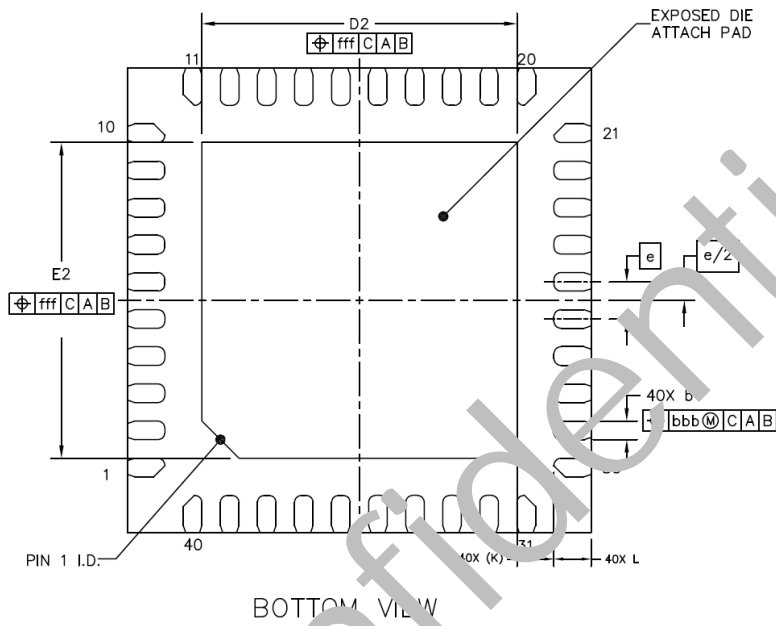
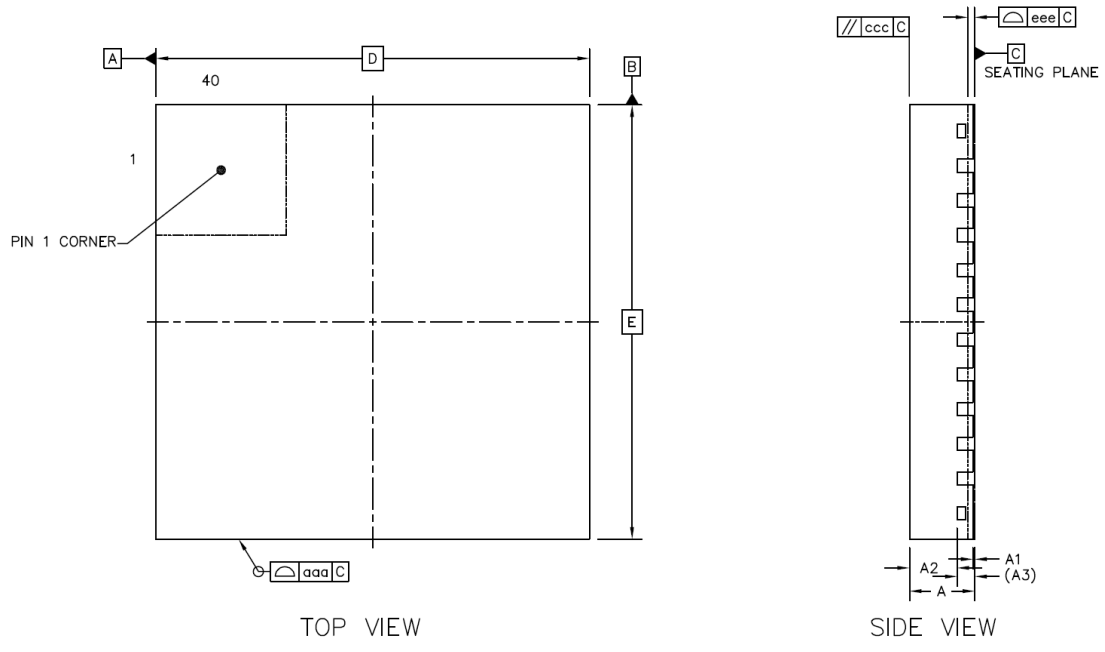
| Part Number | Status | Package Qty | Op temp (°C) | Note |
|-------------|--------|---------------------|--------------|------|
| YT8511C | Active | 3000; tape and reel | 0 to 70 | |
| YT8511H | Active | 3000; tape and reel | -40 to 85 | |

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9 MECHANICAL INFORMATION



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| | | SYMBOL | MIN | NOM | MAX |
|------------------------------|---|--------|-----------|------|------|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | --- |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | 5 BSC | | |
| | Y | E | 5 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| EP SIZE | X | D2 | 3.3 | 3.4 | 3.5 |
| | Y | E2 | 3.3 | 3.4 | 3.5 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | 0.4 REF | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | ccc | 0.1 | | |
| COPLANARITY | | eee | 0.08 | | |
| LEAD OFFSET | | bbb | 0.07 | | |
| EXPOSED PAD OFFSET | | fff | 0.1 | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

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10 ORDERING INFORMATION

| Part Number | Grade | Package | Packaging | Status | Operation Temp |
|-------------|------------|------------------|--------------------------|--------------------|----------------|
| YT8511C | Consumer | QFN 40 5x5 mm | Tape & Reel Qty: 3000 | Mass Production | 0 ~70°C |
| YT8511H | Industrial | QFN 40 5x5 mm | Tape & Reel Qty: 3000 | Mass Production | -40 ~ 85°C |

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