Motorcomm YT8618 Datasheet

INTEGRATED OCTAL 10/100/1000M ETHERNET TRANSCEIVER

VERSION DRAFT_08

DATE 2020-04-23

Copyright Statement

Disclaimer

This document only provides periodic information, and its contents will/may be updated from time to time according to actual situation of Motorcomm's products without further notice. Motorcomm will not take any responsibility for any direct or indirect losses caused due to improper use of this document.

Revision History

Revision	Release Date	Summary
Draft	2019/09/07	First Version
Draft 01	2019/09/12	Update
Draft 02	2019/10/18	Modify Pin arrangement
Draft 03	2020/01/07	Modify Errors
Draft 04	2020/01/09	Modify Errors
Draft 05	2020/02/06	Modify Errors. Add register description.
Draft 06	2020/03/21	Add mechanical information.
Draft 07	2020/03/24	Add SGMII timing parameters. Revise MDC/MDIO timing parameters.
Draft 08	2020/04/23	Upadte pin assignment.

Content

List of Table

List of Figures

1. General Description

The YT8618 integrates octal independent 10/100/1000M Ethernet transceivers into a single IC, and performs all the physical layer (PHY) functions for 1000Base-T, 100Base-TX, and 10Base-Te Ethernet on category 5 UTP cable except 1000Base-T half-duplex. 10Base-T functionality can also be achieved on standard category 3 or 4 cable.

This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The YT8618 also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the four independent transceivers features an innovative QSGMII for reduced PCB trace.

1.1. TARGET APPLICATIONS

- High Port Density Switch
- QSGMII MAC

1.2. System Application

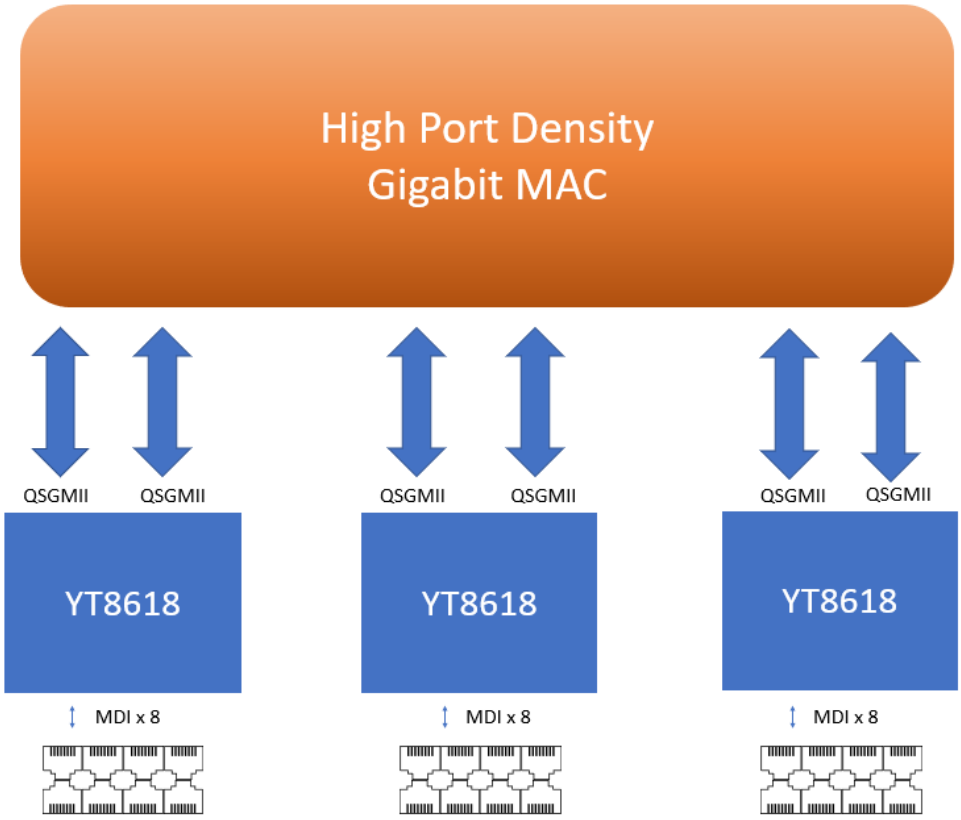


Figure 1. System Application

1.3. Feature

- Octal-port integrated 10/100/1000M Ethernet transceiver
- Each port supports full duplex in 10/100/1000M
- Support LRE100-4, disabled by default
  - Cable reach up to 400 meter @100Mbps
- Support QSGMII (Quad Serial Gigabit Media Independent Interface) in 10/100/1000M mode
- Support SGMII mode direct link to one designated Copper Giga PHY w/ speed adaption
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
  - EEE Buffering
  - Incorporates EEE buffering for seamless support of legacy MACs
- Supports Synchronous Ethernet (Sync-E)
- Supports crossover detection and auto-correction
- Auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports Cable diagnostic
- Supports one interrupt output to external CPU for notification
- Fast link failure indication support
- Support Serial LED interface
- SerDes Test pattern
  - PRBS-7/10/31
  - IDLE/K28.5/D5.6
  - Customized define by user
  - SerDes BIST
- Packet Generator and Checker
- Low power consumption
- Easy layout, good EMI, and good thermal performanc
- 25MHz crystal or 3.3V OSC input
- 3.3V and 1.1V power supply
- LQPF 128 package

2. PiN assigment

2.1. LQFP-128

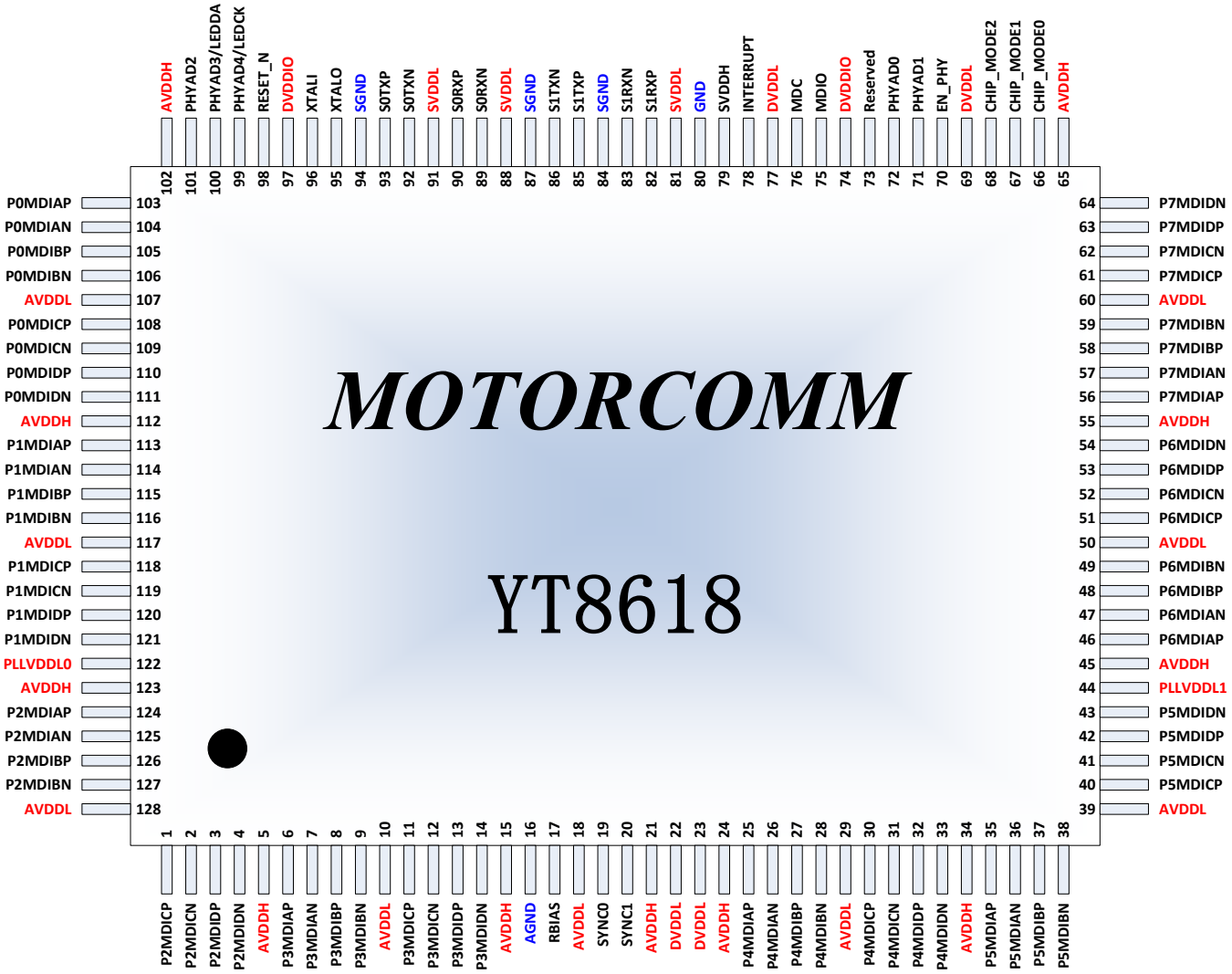


Figure 2. YT8618 Pin Assignment

2.2. Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- I/O: Bidirectional Input/Output Pin
- AI/O: Analog Bidirectional Input/Output Pin
- P: Digital Power Pin
- AP: Analog Power Pin
- A: Analog Pin
- G: Digital Ground Pin
- I_{PD}: Input Pin With internal Pull-Down resistor
- I_{PU}: Input Pin With internal Pull-Up resistor
- O_{PU}: Output Pin With internal Pull-Down Resistor
- O_{PD}: Output Pin With internal Pull-up Resistor
- SP: SerDes Power
- SG: SerDes Ground

2.2.1. All pins

Table 1. All Pins Description

No.	Pin Name	Type
1	P2MDICP	AI/O
2	P2MDICN	AI/O
3	P2MDIDP	AI/O
4	P2MDIDN	AI/O
5	AVDDH	AP
6	P3MDIAP	AI/O
7	P3MDIAN	AI/O
8	P3MDIBP	AI/O
9	P3MDIBN	AI/O
10	AVDDL	AP
11	P3MDICP	AI/O
12	P3MDICN	AI/O
13	P3MDIDP	AI/O
14	P3MDIDN	AI/O
15	AVDDH	AP
16	AGND	P
17	RBIAS	AO
18	AVDDL	AP
19	SYNC0	AO
20	SYNC1	AO
21	AVDDH	AP
22	DVDDL	P
23	DVDDL	P
24	AVDDH	AP
25	P4MDIAP	AI/O
26	P4MDIAN	AI/O
27	P4MDIBP	AI/O
28	P4MDIBN	AI/O
29	AVDDL	AP
30	P4MDICP	AI/O
31	P4MDICN	AI/O
32	P4MDIDP	AI/O
33	P4MDIDN	AI/O
34	AVDDH	AP
35	P5MDIAP	AI/O
36	P5MDIAN	AI/O
37	P5MDIBP	AI/O
38	P5MDIBN	AI/O
39	AVDDL	AP
40	P5MDICP	AI/O
41	P5MDICN	AI/O
42	P5MDIDP	AI/O
43	P5MDIDN	AI/O
44	PLLVDDL1	AP
45	AVDDH	AP
46	P6MDIAP	AI/O
47	P6MDIAN	AI/O
48	P6MDIBP	AI/O
49	P6MDIBN	AI/O
50	AVDDL	AP
51	P6MDICP	AI/O
52	P6MDICN	AI/O
53	P6MDIDP	AI/O
54	P6MDIDN	AI/O
55	AVDDH	AP
56	P7MDIAP	AI/O
57	P7MDIAN	AI/O
58	P7MDIBP	AI/O
59	P7MDIBN	AI/O
60	AVDDL	AP
61	P7MDICP	AI/O
62	P7MDICN	AI/O
63	P7MDIDP	AI/O
64	P7MDIDN	AI/O
65	AVDDH	AP
66	CHIP_MODE0	IPU
67	CHIP_MODE1	IPU
68	CHIP_MODE2	IPU
69	DVDDL	P

70	EN_PHY	I/OPU
71	PHYAD1	I/OPU
72	PHYAD0	I/OPU
73	Reserved	I/OPD
74	DVDDIO	P
75	MDIO	I/OPU
76	MDC	I
77	DVDDL	P
78	INTERRPUT	I/OPU
79	SVDDH	SP
80	GND	GND
81	SVDDL	SP
82	S1RXP	AO
83	S1RXN	AO
84	SGND	SG
85	S1TXP	AI
86	S1TXN	AI
87	SGND	SG
88	SVDDL	SP
89	S0RXN	AO
90	S0RXP	AO
91	SVDDL	SP
92	S0TXN	AI
93	S0TXP	AI
94	SGND	SG
95	XTALO	AO
96	XTALI	AI
97	DVDDIO	P
98	RESET_N	IPU
99	PHYAD4/LEDCK	OPD

100	PHYAD3/LEDDA	I/OPD
101	PHYAD2	IPD
102	AVDDH	AP
103	P0MDIAP	AI/O
104	P0MDIAN	AI/O
105	P0MDIBP	AI/O
106	P0MDIBN	AI/O
107	AVDDL	AP
108	P0MDICP	AI/O
109	P0MDICN	AI/O
110	P0MDIDP	AI/O
111	P0MDIDN	AI/O
112	AVDDH	AP
113	P1MDIAP	AI/O
114	P1MDIAN	AI/O
115	P1MDIBP	AI/O
116	P1MDIBN	AI/O
117	AVDDL	AP
118	P1MDICP	AI/O
119	P1MDICN	AI/O
120	P1MDIDP	AI/O
121	P1MDIDN	AI/O
122	PLLVDDL0	AP
123	AVDDH	AP
124	P2MDIAP	AI/O
125	P2MDIAN	AI/O
126	P2MDIBP	AI/O
127	P2MDIBN	AI/O
128	AVDDL	AP
EPAD	GND EPAD	GND

2.2.2. Media Dependent Interface

Table 2. Media Dependent Interface

Pin Name	Pin No.	Type	Description
P0MDIAP	103	AI/O	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P0MDIAN	104	AI/O	
P0MDIBP	105	AI/O	
P0MDIBN	106	AI/O	
P0MDICP	108	AI/O	
P0MDICN	109	AI/O	
P0MDIDP	110	AI/O	
P0MDIDN	111	AI/O	
P1MDIAP	113	AI/O	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P1MDIAN	114	AI/O	
P1MDIBP	115	AI/O	
P1MDIBN	116	AI/O	
P1MDICP	118	AI/O	
P1MDICN	119	AI/O	
P1MDIDP	120	AI/O	
P1MDIDN	121	AI/O	
P2MDIAP	124	AI/O	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P2MDIAN	125	AI/O	
P2MDIBP	126	AI/O	
P2MDIBN	127	AI/O	
P2MDICP	1	AI/O	
P2MDICN	2	AI/O	
P2MDIDP	3	AI/O	
P2MDIDN	4	AI/O	
P3MDIAP	6	AI/O	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P3MDIAN	7	AI/O	
P3MDIBP	8	AI/O	
P3MDIBN	9	AI/O	
P3MDICP	11	AI/O	
P3MDICN	12	AI/O	
P3MDIDP	13	AI/O	
P3MDIDN	14	AI/O	
P4MDIAP	25	AI/O	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and
P4MDIAN	26	AI/O	
P4MDIBP	27	AI/O	

P4MDIBN	28	AI/O	10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P4MDICP	30	AI/O	
P4MDICN	31	AI/O	
P4MDIDP	32	AI/O	
P4MDIDN	33	AI/O	
P5MDIAP	35	AI/O	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P5MDIAN	36	AI/O	
P5MDIBP	37	AI/O	
P5MDIBN	38	AI/O	
P5MDICP	40	AI/O	
P5MDICN	41	AI/O	
P5MDIDP	42	AI/O	
P5MDIDN	43	AI/O	
P6MDIAP	46	AI/O	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P6MDIAN	47	AI/O	
P6MDIBP	48	AI/O	
P6MDIBN	49	AI/O	
P6MDICP	51	AI/O	
P6MDICN	52	AI/O	
P6MDIDP	53	AI/O	
P6MDIDN	54	AI/O	
P7MDIAP	56	AI/O	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P7MDIAN	57	AI/O	
P7MDIBP	58	AI/O	
P7MDIBN	59	AI/O	
P7MDICP	61	AI/O	
P7MDICN	62	AI/O	
P7MDIDP	63	AI/O	
P7MDIDN	64	AI/O	

2.2.3. MAC SerDes Interface

Table 3. MAC SerDes Interface

Pin Name	Pin No.	Type	Description
S0RXP	90	AO	QSGMII Differential Output. 5GHz serial interfaces to transfer data to an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0RXN	89	AO	
1RXP	82	AO	
S1RXN	83	AO	
S0TXP	93	AI	QSGMII Differential Input. 5GHz serial interfaces to receive data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXN	92	AI	
S1TXP	85	AI	
S1TXN	86	AI	

2.2.4. Serial LED Interface

Table 4. Serial LED Interface

Pin Name	Pin No.	Type	Description
PHYAD4/LEDCK	99	I/O_{PD}	Serial LED Clock Output
PHYAD3/LEDDA	100	I/O_{PD}	Serial LED Data Output

2.2.5. SYNCE Interface

Table 5. SYNCE Interface

Pin Name	Pin No.	Type	Description
SYNCE0	19	AO/PD	SYNCE 0 clock output
SYNCE1	20	AO/PD	SYNCE 1 clock output

2.2.6. Configuration

Table 6. Configuration

Pin Name	Pin No.	Type	Description
PHYAD0	72	I/O_{PD}	PHYADDR0, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.
PHYAD1	71	I/O_{PD}	PHYADDR1, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYAD2	101	I_{PD}	PHYADDR2, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYAD4/LEDCK	100	I/O_{PD}	PHYADDR3, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYAD4/LEDCK	99	I/O_{PD}	PHYADDR4, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
EN_PHY	70	I/O_{PD}	Enable PHY Power 1: Power up all ports. 0: Power down all ports and set the MII register 0.11 power down as 1. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
CHIP_MODE2	68	I_{PU}	CHIP MODE [2:0] refer to: 3'b000 or 3'b001: Reserved for feature useage; 3'b010: Qsgmii x1 and Sgmii x1 + Copper x5 mode; 3'b011: Sgmii x2 + Copper x2 mode; 3'b100 or 3'b101: Qsgmii x2 + Copper x8 mode; 3'b110: SGMII x1 + Combo x1; 3'b111: Qsgmii x1 + Copper x3 and Combo x1;
CHIP_MODE1	67	I_{PU}	
CHIP_MODE0	66	I_{PU}	

2.2.7. Miscellaneous Interface

Table 7. Miscellaneous Interface

Pin Name	Pin No.	Type	Description
MDC	76	I	MII Management Interface Clock Input. The clock reference for the MII management interface. The maximum frequency support is 12.5MHz.
MDIO	75	I/O_{PU}	MII Management Interface Data Input/Output. MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.
INTERRUPT	78	I/O_{PU}	Interrupt output when Interrupt even occurs. Active High by pull-down to GND via a 1K resistor. Active Low by pull-up to DVDDIO via a 4.7K resistor.
RESET_N	98	I_{PU}	Hardware Reset (Active Low Reset Signal). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
RBIAS	17	AO	MDI Bias Resistor. Adjusts the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.
XTALI	96	AI	25MHz Crystal Clock Input. 25MHz±50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
XTALO	95	AO	25MHz Crystal Clock Output. 25MHz±50ppm tolerance crystal output. Refer to XTALI.
Reserved	73	IO/PD	Reserved. Must be floating or tied to GND via a 1K resistor for normal operation

2.2.8. Power and GND

Table 8. Power and GND

Pin Name	Pin No.	Type	Description
AVDDH	5, 15, 21, 24, 34, 45, 55, 65, 102, 112, 123	AP	Analog High Voltage Power
AVDDL	10,18,29.39,50,60, 107,117,128	AP	Analog Low Voltage Power
PLLVDDL0	122	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
PLLVDDL1	44	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
SVDDH	79	SP	QSGMII SerDes High Voltage Power
SVDDL	81,88,91	SP	QSGMII SerDes Low Voltage Power
DVDDIO	74,97	P	Digital I/O Power
DVDDL	22,23,69,77	P	Digital Low Voltage Power
AGND	16	AG	Analog Ground
SGND	84,87,94	SG	SerDes Ground
GND	80	G	Ground
GND	EPAD	G	Digital/Analog Ground

3. Function Description

3.1. Mode selcetion

3.1.1. QSGMII x 2 + Copper x 8

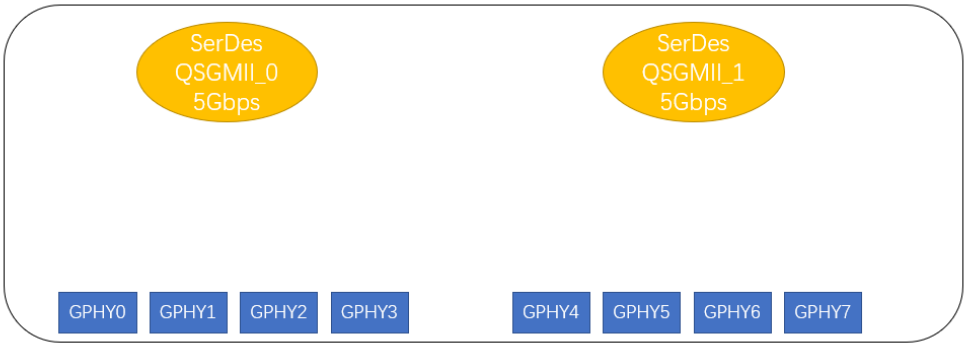


Figure 3. QSGMII x 2 + Copper x 8

3.1.2. QSGMII x 1 + SGMII x 1 + Copper x 5

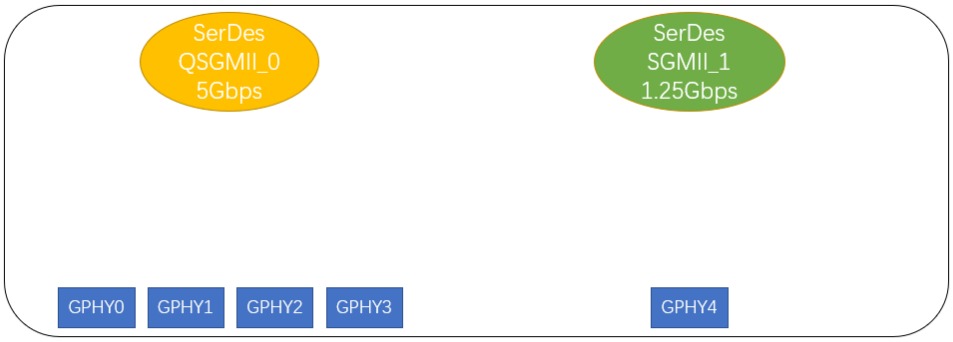


Figure 4. QSGMII x 1 + SGMII x 1 + Copper x 5

3.1.3. QSGMII x 1 + Copper x 3 + Combo x 1

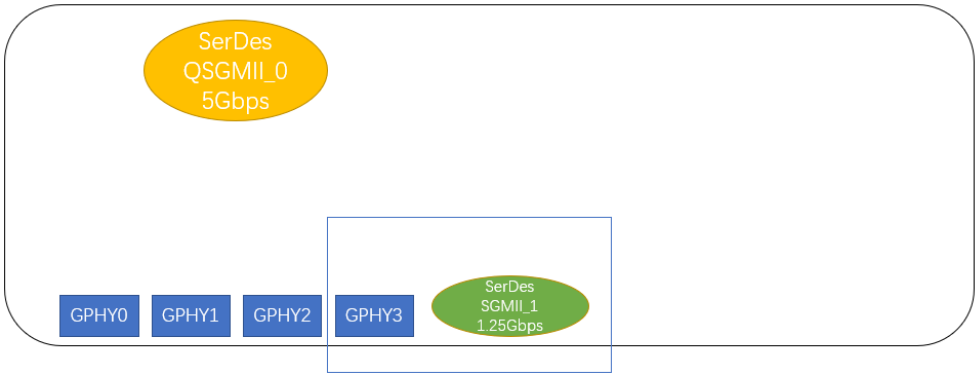


Figure 5. QSGMII x 1 + Copper x 3 + Combo x 1

3.1.4. SGMII x 2 + Copper x 2

Figure 6. SGMII x 2 + Copper x 2

3.1.5. SGMII x 1 + Combo x 1

Figure 7. SGMII x 1 + Combo x 1

3.2. Transmit Functions

3.2.1. Transmit Encoder Modes

3.2.1.1. 1000 BASE-T

In 1000 BASE-T mode, the YT8618 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.

3.2.1.2. 100 BASE-TX

In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

3.2.1.3. 10 BASE-Te

In 10 BASE-Te mode, the YT8618 transmits and receives Manchester-encoded data.

3.3. Receive Functions

3.3.1. Receive Decoder Modes

3.3.1.1. 1000 BASE-T

In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

3.3.1.2. 100 BASE-TX

In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/ 4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.

3.3.1.3. 10 BASE-Te

In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

3.4. LRE100-4

LRE100-4 is the Motorcomm proprietary mode in long reach Ethenet application up to 400m in 100M mode by 4 pairs.

3.5. MDC/MDIO interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

3.6. Auto-Negoitation

The YT8618 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100/1000Mbps

b) Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

a) Power-up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power-down to power up

d) Link down

Auto negotiation is enabled for YT8618 by default, and can be disabled by hardware or software control.

3.7. LDS (Link discovey signaling)

YT8618 supports long range ethernet (LRE), which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

a) Master/Slave assignment
b) Estimate cable length
c) Confirm pair number and pair connectivity ordering
d) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy Ethernet PHY, YT8618 can detect the standard NLP, FLP, MLT-3 IDLE signal, or 100BASE-T4 signal, and then transits LDS mode into Clause 28 auto negotiation mode. If the link partner is an IEEE automotive ethernet PHY, YT8618 can also detect link partner's master/slave mode, and configure itself as an opposite master/slave mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link.

3.8. Polarity detection and auto correction

YT8618 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

3.9. EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4. Operational Description

4.1. Reset

YT8618 has a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. During RESET_N is active, YT8618 latches input values on strappings which are used as configuration information to provide flexibility in application without MDIO access.

Table 9. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

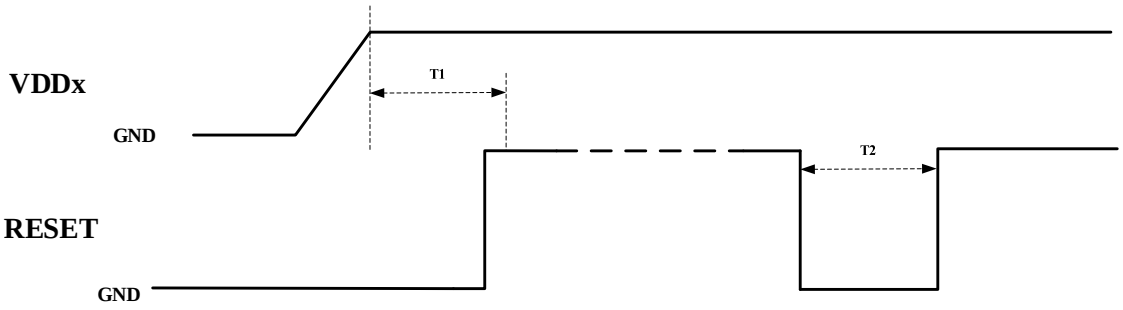


Figure 8. Reset Timing Diagram

4.2. PHY Address

For YT8618, Strapping PHYAD[4:0] is used to generate phy address.

4.3. Loopback mode

There are three loopback modes in YT86182.

4.3.1. Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the YT8618 device.

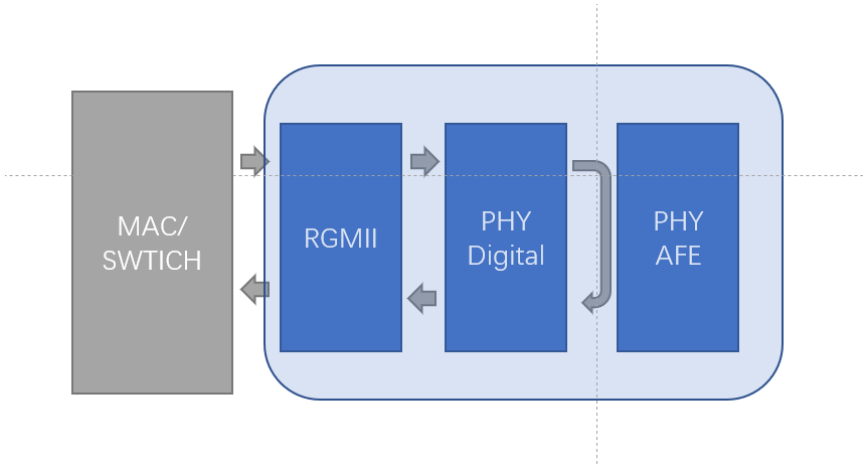


Figure 9. Digital Loopback

4.3.2. External Loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

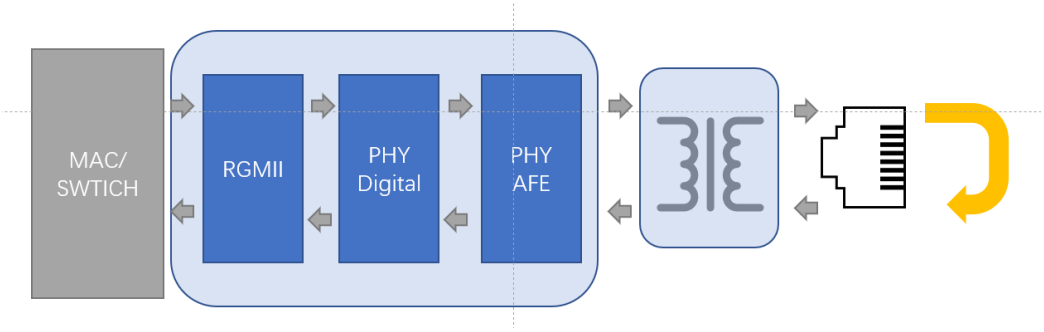


Figure 10. External Loopback

4.3.3. Remote PHY Loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.

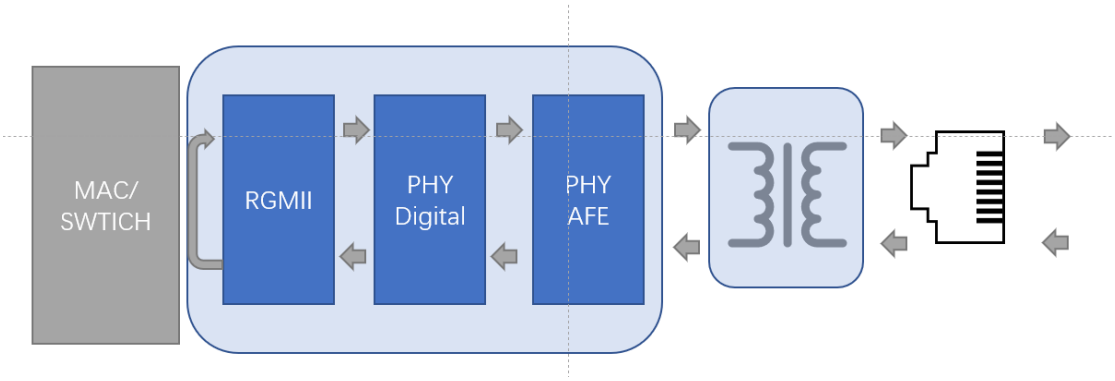


Figure 11. Remote PHY Loopback

4.4. LED

The YT8618 supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins.

Each MDI port has three indicator symbols and each fiber port has three indicator symbols. Each symbol may have different indicator

4.5. Power Supplies

5. Register Overview

5.1. Common Register

5.1.1. SMI Mux (EXT 0xA000)

Table 10. SMI Mux (EXT 0xA000)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	en_brdst_phy	RW	0x0	When bit1 smi_sds_phy is 0, this bit controls to broadcast write to all PHYs. 0: disable. 1: enable broadcast write.
3	en_brdst_q	RW	0x0	When bit1 smi_sds_phy is 1, this bit controls to broadcast write to all QSGMII channels. 0: disable. 1: enable broadcast write;.
2	en_brdst_sf	RW	0x0	When bit1 smi_sds_phy is 1, this bit controls to broadcast write to all SGMIIs. 0: disable. 1: enable broadcast write.
1	Smi_sds_phy	RW	0x0	To control access whether phy register or sds register. 0: to access phy. 1: to access sds.
0	smi_sf	RW	0x0	When smi_sds_phy is 1, this bit controls to access whether sds 2/3/4/5 (SGMII) register or sds 0/1 (QSGMII) register. 0: to access QSGMII register. 1: to access SGMII register;

5.1.2. SLED cfg0 (EXT 0xA001)

Bit	Symbol	Access	Default	Description
15	led_manu_en	RW	0x0	to control serial LEDs status manually. 1: enable; 0: disable, SLED are controled by internal status then.
14:12	led_manu_st	RW	0x0	SLEDs' manul status, corresponding to each port's 3 SLEDs.
11	led_act_low	RW	0x1	control SLED's polarity. 1: active low; 0: active high.
10:8	led_bit_mask	RW	0x7	
7:0	led_en_ctrl	RW	0xFF	

5.1.3. SLED cfg1 (EXT 0xA002)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	always 0.
14:12	led_sel_p3	RW	0x3	to select which internal port's status to controls the port3 3 SLEDs.
11	Reserved	RO	0x0	always 0.
10:8	led_sel_p2	RO	0x2	to select which internal port's status to controls the port2 3 SLEDs.
7	Reserved	RO	0x0	always 0.
6:4	led_sel_p1	RW	0x1	to select which internal port's status to controls the port1 3 SLEDs.
3	Reserved	RO	0x0	always 0.
2:0	led_sel_p0	RW	0x0	to select which internal port's status to controls the port0 3 SLEDs.

5.1.4. SLED cfg2 (EXT 0xA003)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	always 0.
14:12	led_sel_p7	RW	0x7	to select which internal port's status to controls the port7 3 SLEDs.
11	Reserved	RO	0x0	always 0.
10:8	led_sel_p6	RO	0x6	to select which internal port's status to controls the port6 3 SLEDs.
7	Reserved	RO	0x0	always 0.
6:4	led_sel_p5	RW	0x5	to select which internal port's status to controls the port5 3 SLEDs.
3	Reserved	RO	0x0	always 0.
2:0	led_sel_p4	RW	0x4	to select which internal port's status to controls the port4 3 SLEDs.

5.1.5. SLED cfg3 (EXT 0xA004)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	always 0.
9	led_x2	RW	0x0	
8	led_seri_dis	RW	0x0	
7:6	Reserved	RO	0x0	always 0.
5:4	led_mode	RW	0x3	

3:2	reserved	RO	0x0	always 0.
1:0	led_clk_cycle	RW	0x1	

5.1.6. mode_chg_reset (EXT 0xA005)

Bit	Symbol	Access	Default	Description
15	mode_chg_reset	RW, SC	0x0	This bit will asserts when ext.a007.12 en_phy or ext.a007.3:0 changes. When this bit asserts, whole chip will be reset. This bit is self-cleared.
14:13	reserved	RO	0x0	always 0.
12	iddq_mode_reg	RW	0x0	1: control to enter IDDQ mode.
11	int_polarity	RW	0x0	1: INT_N is active LOW; 0: INT_N is active HIGH.
10	Bypass_mdio_watchdog	RW	0x0	bypass mdio watch dog
9:8	Reserved	RO	0x0	Reserved
7	En_mdc_la	RW	0x1	enable mdc latch for read data
6	En_phyaddr0	RW	0x1	enable phyaddr0
5	En_bdcst_addr	RW	0x0	enable broadcast address
4:0	Bdcst_addr	RW	0x0	broadcast address

5.1.7. Chip_Mode (Ext 0xA007)

Table 11. Chip_Mode (Ext 0xA007)

Bit	Symbol	Access	Default	Description
15:13	reserved	RO	0x0	
12	en_phy	RW, SOR	0x1	0: disable all the copper ports and serdes ports. 1: enable all the coppers port and serdes ports.
11:6	reserved	RO	0x0	always 0.
5	en_pwron_light	RW, SOR	0x1	make SLEDs or direct LEDs light for 200ms after hardware reset or power on reset.
4	dis_sled	RW, SOR	0x1	0: to enable SLED. 1: to disable SLED.
3	reserved	RO	0x0	always 0.

2:0	chip_mode	RW, SOR	0x4	3'b000 Reserved for feature useage; 3'b001 Reserved for feature useage; 3'b010, Qsgmii x1 and Sgmii x1 + Copper x5 mode; 3'b011, Sgmii x2 + Copper x2 mode; 3'b100, Qsgmii x2 + Copper x8 mode; 3'b101, Qsgmii x2 + Copper x8 mode; 3'b110, SGMII x1 + Combo x1; 3'b111, Qsgmii x1 + Copper x3 and Combo x1;

5.1.8. SYNCE0 cfg (EXT 0xA006)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_0	RW	0x0	1=enable to output the synce_clk0 to the PAD SYNC0
14	bp_sync_lock_gating_0	RW	0x0	When synce_clk0 is not locked, this bit controls whether to output the synce_clk0 or crystal clock to the PAD SYNC0. 1: to output; 0: to not output.
13	sel_synce_125m_0	RW	0x0	controls the synce_clk0's frequence. 1: 125MHz; 0: 25MHz.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_0	RW	0x0	when ext.a006.13 sel_synce_125m_0 is 0, this bit controls to output the crystal clock to the PAD SYNC0. 1: to output; 0: to not output.
9	sel_rclk_sds1_0	RW	0x0	bit9:0, select the source of the synce_clk0 from the recovered RX clocks. The recovered RX clocks include that from 8 port copper PHYs and 2 5G serdes PHYs; MSB has the higher priority, for example, bit9:0=280h means to output the sds1's RX recovered clock; bit9:0=030h means to output the port 6's RX recovered clock. sds1, means the 5G serdes connected to port 4~7; sds0, means the 5G serdes connencted to port 0~3. phy7, means the copper port 7; phy6, means the copper port 6; phy5, means the copper port 5; phy4, means the copper port 4;
8	sel_rclk_sds0_0	RW	0x0	
7	sel_rclk_phy7_0	RW	0x0	
6	sel_rclk_phy6_0	RW	0x0	
5	sel_rclk_phy5_0	RW	0x0	
4	sel_rclk_phy4_0	RW	0x0	
3	sel_rclk_phy3_0	RW	0x0	
2	sel_rclk_phy2_0	RW	0x0	
1	sel_rclk_phy1_0	RW	0x0	
0	sel_rclk_phy0_0	RW	0x0	

				phy3, means the copper port 3. phy2, means the copper port 2. phy1, means the copper port 1. phy0, means the copper port 0.

5.1.9. SYNCE1 cfg (EXT 0xA00E)

Bit	Symbol	Access	default	Description
15	sync_clk_en_1	RW	0x0	1=enable to output the synce_clk1 to the PAD SYNC1.
14	bp_sync_lock_gating_1	RW	0x0	When synce_clk1 is not locked, this bit controls whether to output the synce_clk1 or crystal clock to the PAD SYNC0. 1: to output; 0: to not output.
13	sel_synce_125m_1	RW	0x0	controls the synce_clk1's frequence. 1: 125MHz; 0: 25MHz.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_1	RW	0x0	when ext.a006.13 sel_synce_125m_0 is 0, this bit controls to output the crystal clock to the PAD SYNC0. 1: to output; 0: to not output.
9	sel_rclk_sds1_1	RW	0x0	bit9:0, select the source of the synce_clk1 from the recovered RX clocks. The recovered RX clocks include that from 8 port copper PHYs and 2 5G serdes PHYs. MSB has the higher priority, for example, bit9:0=280h means to output the sds1's RX recovered clock; bit9:0=030h means to output the port 6's RX recovered clock. sds1, means the 5G serdes connected to port 4~7 sds0, means the 5G serdes connencted to port 0~3. phy7, means the copper port 7; phy6, means the copper port 6; phy5, means the copper port 5; phy4, means the copper port 4; phy3, means the copper port 3. phy2, means the copper port 2.
8	sel_rclk_sds0_1	RW	0x0	
7	sel_rclk_phy7_1	RW	0x0	
6	sel_rclk_phy6_1	RW	0x0	
5	sel_rclk_phy5_1	RW	0x0	
4	sel_rclk_phy4_1	RW	0x0	
3	sel_rclk_phy3_1	RW	0x0	
2	sel_rclk_phy2_1	RW	0x0	
1	sel_rclk_phy1_1	RW	0x0	
0	sel_rclk_phy0_1	RW	0x0	

				phy1, means the copper port 1. phy0, means the copper port 0.

5.2. Phy MII Register

The YT8618 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 25 MHz must drive the MDC pin of the YT8618. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

5.2.1. Basic Control Register (0x00)

Table 12. Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW SWC	0x0	Internal loopback control
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW SWC	0x0	1 = Power down
10	Isolate	RW SWC	0x0	Isolate phy from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW SC SWS	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

5.2.2. Basic Status Register (0x01)

Table 13. Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation
2	Link_Status	RO SWC LL	0x0	Link status
1	Jabber_Detect	RO RC SWC LH	0x0	10Baset jabber detected
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

5.2.3. PHY Identification Register1 (0x02)

Table 14. PHY Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x0	Bits 3 to 18 of the Organizationally Unique Identifier

5.2.4. PHY Identification Register2 (0x03)

Table 15. PHY Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number

3:0	Revision_No	RO	0xa	4 bits manufacturer's revision number

5.2.5. Auto-Negotiation Advertisement (0x04)

Table 16. Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
14	Ack	RO	0x0	Always 0.
13	Remote_Fault	RW	0x0	1 = Set Remote Fault bit
12	Extended_NEXT_Page	RW	0x1	Extended nEXT page enable control bit
11	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
10	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
9	100BASE-T4	RO	0x0	1 = Able to perform 100BASE-T4
8	100BASE-TX_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
7	100BASE-TX_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
6	10BASE-Te_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
5	10BASE-Te_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
4:0	Selector_Field	RW	0x1	Selector Field mode.

5.2.6. Auto-Negotiation Link Partner Ability (0x05)

Table 17. Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	0x0	Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13
12	RESERVED	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 12

11	ASYMMETRIC_PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 11
10	PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 10
9	100BASE-T4	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 9
8	100BASE-TX_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 8
7	100BASE-TX_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 7
6	10BASE-Te_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 6
5	10BASE-Te_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 5
4:0	SELECTOR_FIELD	RO SWC	0x0	Selector Field Received Code Word Bit 4:0

5.2.7. Auto-Negotiation Expansion Register (0x06)

Table 18. 6.2.7. Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	Parallel Detection fault	RO RC SWC LH	0x0	1 = Fault is detected
3	Link partner nEXT page able	RO SWC LH	0x0	1 = Link partner supports NEXT page
2	Local NEXT Page able	RO	0x1	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Link Partner Auto negotiation able	RO	0x0	1 = Link partner supports auto-negotiation

5.2.8. Auto-Negotiation NEXT Page Register (0x07)

Table 19. Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RW	0x0	Transmit Code Word Bit 15
14	Reserved	RO	0x0	Transmit Code Word Bit 14
13	Message page mode	RW	0x1	Transmit Code Word Bit 13
12	Ack2	RW	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	Transmit Code Word Bit 11
10:0	Message/Unformatte	RW	0x1	Transmit Code Word Bits [10:0].

5.2.9. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Table 20. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO	0x0	Received Code Word Bit 15
14	Reserved	RO	0x0	Received Code Word Bit 14
13	Message page mode	RO	0x0	Received Code Word Bit 13
12	Ack2	RO	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	Received Code Word Bit 11
10:0	Message/Unformatte	RO	0x0	Received Code Word Bit 10:0

5.2.10. MASTER-SLAVE control register (0x09)

Table 21. MASTER-SLAVE control register (0x09)

Bit	Symbol	Access	Default	Description
15:13	Test mode	RW	0x0	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation.
12	Master/Slave Manual configuration Enable	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
11	Master/Slave configuration	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
10	Port Type	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
9	1000BASE-T Full	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
8	1000BASE-T Half-	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
7:0	Reserved	RW	0x0	Write as 0, ignore on read.

5.2.11. MASTER-SLAVE Status Register (0x0A)

Table 22. MASTER-SLAVE Status Register (0x0A)

Bit	Symbol	Access	Default	Description
15	Master/Slave_cfg_error	RO RC SWC LH	0x0	This register bit will clear on read
14	Master/Slave	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1.
13	Local Receiver Status	RO	0x0	1 = Local Receiver OK
12	Remote Receiver	RO	0x0	1 = Remote Receiver OK
11	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1.
10	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1.
9:8	Reserved	RO	0x0	Reserved
7:0	Idle Error Count	RO RC	0x0	MSB of Idle Error Counter.

5.2.12. MMD Access Control Register (0x0D)

Table 23. MMD Access Control Register (0x0D)

Bit	Symbol	Access	Default	Description
15:14	Function	RW	0x0	00 = Address
13:5	Reserved	RO	0x0	Reserved
4:0	DEVAD	RW	0x0	MMD register device address.

5.2.13. MMD Access Data Register (0x0E)

Table 24. MMD Access Data Register (0x0E)

Bit	Symbol	Access	Default	Description
15:0	Address data	RW	0x0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

5.2.14. Extended status register (0x0F)

Table 25. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x0	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x1	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

5.2.15. PHY Specific Function Control Register (0x10)

Table 26. PHY Specific Function Control Register (0x10)

Bit	Symbol	Access	Default	Description

15:7	Reserved	RO	0x0	Reserved
6:5	Cross_md	RW	0x3	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset.
4	Int_polar_sel	RW	0x0	To control the polarity of interrupt PINs.
3	Crs_on_tx	RW	0x0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:
2	En_sqe_test	RW	0x0	1 = SQE test enabled
1	En_pol_inv	RW	0x1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te.
0	Dis_jab	RW	0x0	Jabber takes effect only in 10BASE-Te half-duplex mode.

5.2.16. PHY Specific Status Register (0x11)

Table 27. PHY Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
12	Page Received real-time	RO	0x0	1 = Page received
11	Speed and Duplex Resolved	RO	0x0	When Auto-Negotiation is disabled, this bit is set to
10	Link status real-time	RO	0x0	1 = Link up
9:7	Reserved	RO	0x0	Reserved
6	MDI Crossover Status	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
5	Wirespeed downgrade	RO	0x0	1 = Downgrade
4	Reserved	RO	0x0	
3	Transmit Pause	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed.
2	Receive Pause	RO	0x0	This status bit is valid only when bit[11] is 1. Bit[11]
1	Polarity Real Time	RO	0x0	1 = Reverted polarity
0	Jabber Real Time	RO	0x0	1 = Jabber

5.2.17. Interrupt Mask Register (0x12)

Table 28. Interrupt Mask Register (0x12)

Bit	Symbol	Access	Default	Description

15	Auto-Negotiation Error INT mask	RW	0x0	1 = Interrupt enable
14	Speed Changed INT mask	RW	0x0	1 = Interrupt enable
13	Duplex changed INT mask	RW	0x0	1 = Interrupt enable
12	Page Received INT mask	RW	0x0	1 = Interrupt enable
11	Link Failed INT mask	RW	0x0	1 = Interrupt enable
10	Link Succeed INT mask	RW	0x0	1 = Interrupt enable
9:7	reserved	RW	0x0	No used.
6	WOL INT mask	RW	0x0	1 = Interrupt enable
5	Wirespeed downgraded INT mask	RW	0x0	1 = Interrupt enable
4	Reserved	RW	0x0	No used.
3	Serdes Link Failed INT mask	RW	0x0	1 = Interrupt enable
2	Serdes Link Success INT mask	RW	0x0	1 = Interrupt enable
1	Polarity changed INT mask	RW	0x0	1 = Interrupt enable
0	Jabber Happened INT mask	RW	0x0	1 = Interrupt enable

5.2.18. Interrupt Status Register (0x13)

Table 29. Interrupt Status Register (0x13)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT	RW	0x0	Error can take place when any of the following
14	Speed Changed INT	RW	0x0	1 = Speed changed
13	Duplex changed INT	RW	0x0	1 = duplex changed
12	Page Received INT	RW	0x0	1 = Page received
11	Link Failed INT	RW	0x0	1 = Phy link down takes place
10	Link Succeed INT	RW	0x0	1 = Phy link up takes place
6	WOL INT	RW	0x0	1 = PHY received WOL magic frame.
5	Wirespeed downgraded INT	RW	0x0	1 = speed downgraded.
4	Reserved	RW	0x0	No used.
3	Serdes Link Failed INT	RW	0x0	1 = Sds link down takes place
2	Serdes Link Success INT	RW	0x0	1 = Sds link up takes place
1	Polarity changed INT	RW	0x0	1 = PHY revered MDI polarity
0	Jabber Happened INT	RW	0x0	1 = 10BaseT TX jabber happened

5.2.19. Speed Auto Downgrade Control Register (0x14)

Table 30. Speed Auto Downgrade Control Register (0x14)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	En_mdio_latch	RW	0x1	1 = To latch MII/MMD register's read out value during MDIO read

10	Start_autoneg	RW	0x0	Set it to cause PHY to restart auto-negotiation.
9	Reverse_autoneg	RW	0x0	1 = reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s.
8	Dis_giga	RW	0x0	1 = disable advertise Giga ability in autoneg;
7:6	Reserved	RO	0x0	Reserved
5	En_speed_downgrade	RW POS	0x1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update. This bit will be set to 1'b0 in UTP_TO_FIBER_FORCE and UTP_TO_FIBER_AUTO mode; else set to 1'b1, only take effect after software reset
4:2	Autoneg retry limit pre-downgrade	RW	0x3	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. only take effect after software reset
1	Bp_autospd_timer	RW	0x0	1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; only take effect after software reset
0	Reserved	RO	0x0	Reserved

5.2.20. Rx Error Counter Register (0x15)

Table 31. Rx Error Counter Register (0x15)

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	0x0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

5.2.21. Extended Register's Address Offset Register (0x1E)

Table 32. Extended Register's Address Offset Register (0x1E)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Extended Register Address Offset	RW	0x0	It's the address offset of the extended register that will be Write or Read

5.2.22. Extended Register's Data Register (0x1F)

Table 33. Extended Register's Data Register (0x1F)

Bit	Symbol	Access	Default	Description
15:0	Extended Register Data	RW	0x0	It's the data to be written to the extended register indicated by the address offset in register 0x1E, or the data read out from that extended register.

5.3. Phy EXT Register

5.3.1. LPBKs Register (EXT 0x0A)

Table 34. LPBKs Register (EXT 0x0A)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	En_mskbt10_inan	RW	0x1	1 = enable the function of dividing Manchester code from MLT-3 code.
10	En_10bt_idl	RW	0x1	1 = In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC; For FPGA due to mdio control, this bit is set to 1'b0
9	Bt10_squlch_ctrl	RW	0x1	1 = while receiving pulse_p/n toggle, bt10 carrier sense will be set even though link is no up;
8:06	Reserved	RW	0x0	Reserved
5	rem_phy_lpbk	RW	0x0	control to set UTP to remote phy loopback mode or not.
4	Ext_lpbk	RW	0x0	External loopback.
3	Lpbk_ctrl_10bt	RW SWC	0x1	Control the loopback depth in 10BT when MII register 0x0 bit14 loopback is set.
2:0	Test_mode_10bt	RW SWC	0x0	Test_mode[2:0] is for 10BT test mode select:

5.3.2. Pkgen Cfg1 (EXT 0x38)

Table 35. Pkgen Cfg1 (EXT 0x38)

Bit	Symbol	Access	default	Description
15:13	Reserved	RW	0x0	Reserved
12	En_pkgen_da_sa	RW	0x0	
11	Pkgen_brdcst	RW	0x0	
10	Pkgchk_txsrc_sel	RW	0x0	
9	Pkgen_en_az	RW	0x0	
8:0	Pkgen_in_az_t	RW	0x1ff	

5.3.3. Pkgen Cfg3 (EXT 0x3A)

Table 36. Pkgen Cfg3 (EXT 0x3A)

Bit	Symbol	Access	default	Description
7:0	Pkgen_da	RW	0x0	
7:0	Pkgen_sa	RW	0x0	

5.3.4. Pkg Cfg0 (EXT 0xA0)

Table 37. Pkg Cfg0 (EXT 0xA0)

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
13	Bp_pkg_gen	RW	0x1	1: normal mode, to send xMII TX data from PAD;
12	Pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.
11:8	Pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	0xc	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages.
1:0	Pkg_payload	RW	0x0	Control the payload of the generated packages.

5.3.5. Pkg Cfg1 (EXT 0xA1)

Table 38. Pkg Cfg1 (EXT 0xA1)

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	0x40	To set the length of the generated packages.

5.3.6. Pkg Cfg2 (EXT 0xA2)

Table 39. Pkg Cfg2 (EXT 0xA2)

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

5.3.7. Pkg Rx Valid0 (EXT 0xA3)

Table 40. Pkg Rx Valid0 (EXT 0xA3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.8. Pkg Rx Valid1 (EXT 0xA4)

Table 41. Pkg Rx Valid1 (EXT 0xA4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.9. Pkg Rx Os0 (EXT 0xA5)

Table 42. Pkg Rx Os0 (EXT 0xA5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.10. Pkg Rx Os1 (EXT 0xA6)

Table 43. Pkg Rx Os1 (EXT 0xA6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.11. Pkg Rx Us0 (EXT 0xA7)

Table 44. Pkg Rx Us0 (EXT 0xA7)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

5.3.12. Pkg Rx Us1 (EXT 0xA8)

Table 45. Pkg Rx Us1 (EXT 0xA8)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.13. Pkg Rx Err (EXT 0xA9)

Table 46. Pkg Rx Err (EXT 0xA9)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

5.3.14. Pkg Rx Os Bad (EXT 0xAA)

Table 47. Pkg Rx Os Bad (EXT 0xAA)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

5.3.15. Pkg Rx Fragment (EXT 0xAB)

Table 48. Pkg Rx Fragment (EXT 0xAB)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

5.3.16. Pkg Rx Nosfd (EXT 0xAC)

Table 49. Pkg Rx Nosfd (EXT 0xAC)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO/RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

5.3.17. Pkg Tx Valid0 (EXT 0xAD)

Table 50. Pkg Tx Valid0 (EXT 0xAD)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.18. Pkg Tx Valid1 (EXT 0xAE)

Table 51. Pkg Tx Valid1 (EXT 0xAE)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO/RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.19. Pkg Tx Os0 (EXT 0xAF)

Table 52. Pkg Tx Os0 (EXT 0xAF)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.20. Pkg Tx Os1 (EXT 0xB0)

Table 53. Pkg Tx Os1 (EXT 0xB0)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.21. Pkg Tx Us0 (EXT 0xB1)

Table 54. Pkg Tx Us0 (EXT 0xB1)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

5.3.22. Pkg Tx Us1 (EXT 0xB2)

Table 55. Pkg Tx Us1 (EXT 0xB2)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO/RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.23. Pkg Tx Err (EXT 0xB3)

Table 56. Pkg Tx Err (EXT 0xB3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

5.3.24. Pkg Tx Os Bad (EXT 0xB4)

Table 57. Pkg Tx Os Bad (EXT 0xB4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

5.3.25. Pkg Tx Fragment (EXT 0xB5)

Table 58. Pkg Tx Fragment (EXT 0xB5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

5.3.26. Pkg Tx Nosfd (EXT 0xB6)

Table 59. Pkg Tx Nosfd (EXT 0xB6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

5.4. SDS(1.25G/5G) MII Register

5.4.1. Basic Control Register (0x00)

Table 60. Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW	0x0	Internal loopback control
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW	0x0	1 = Power down
10	Isolate	RW	0x0	Isolate phy from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW SC	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
7	Collision_Test	RW	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_ Selection(MSB)	RW	0x1	See bit13.

5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

5.4.2. Basic Status Register (0x01)

Table 61. Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x0	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x0	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x0	Whether support EXTended status register in 0Fh
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC L	0x0	1'b0: no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation
2	Link_Status	RO LL SWC	0x0	Link status
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

5.4.3. Sds Identification Register1 (0x02)

Table 62. Sds Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x0	Bits 3 to 18 of the Organizationally Unique Identifier

5.4.4. Sds Identification Register2 (0x03)

Table 63. Sds Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number
3:0	Revision_No	RO	0xa	4 bits manufacturer's revision number

5.4.5. Auto-Negotiation Advertisement (0x04)

Table 64. Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

5.4.6. Auto-Negotiation Link Partner Ability (0x05)

Table 65. Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO SWC	0x0	NEXT page. Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved. Received Code Word Bit 11:9
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved. Received Code Word Bit 4:0

5.4.7. Auto-Negotiation Expansion Register (0x06)

Table 66. 6.2.7. Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local NEXT Page able	RO	0x0	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Reserved	RO	0x0	Reserved

5.4.8. Auto-Negotiation NEXT Page Register (0x07)

Table 67. Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15:0	NEXT Page	RO	0x0	always be 0

5.4.9. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Table 68. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner NEXT Page	RO	0x0	always be 0

5.4.10. Extended status register (0x0F)

Table 69. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

5.4.11. Sds Specific Status Register (0x11)

Table 70. Sds Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.

12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up
9	Rx_lpi_active	RO	0x0	rx lpi is active
8	Duplex_error	RO	0x0	realtime duplex error
7:6	Reserved	RO	0x0	
5:4	Ser_mode_cfg	RO	0x0	realtime serdes working mode. 00: SG_MAC; 01: SG_PHY; 10: FIB_1000; 11: FIB_100.
3:1	Xmit	RO	0x0	realtime transmit statemachine. 001: Xmit Idle; 010: Xmit Config; 100: Xmit Data.
0	Syncstatus	RO	0x0	realtime syncstatus

5.4.12. 100FX Cfg (0x14)

Table 71. 100FX Cfg (0x14)

Bit	Symbol	Access	Default	Description
15	Force_sg_status	RW	0x0	Force sds linkup
14	Duplex_to_mac_100fx	RW	0x1	duplex setting to mac in 100fx mode
13:12	Pause_to_mac_100fx	RO	0x3	Pause setting to mac in 100fx mode
11:0	Reserved	RO	0x0	Reserved

5.4.13. Receive Err Counter (0x15)

Table 72. Receive Err Counter (0x15)

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO	0x0	receive error counter

5.4.14. Link Fail Counter (0x16)

Table 73. Link Fail Counter (0x16)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Link_fail_cnt	RO	0x0	link fail counter

6. Timing and AC Characteristics

6.1. AC Characteristics

6.1.1. Crystal Requirement

Table 74. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
F_{ref} Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-		50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.4	V

6.1.2. Oscillator/External Clock Requirement

Table 75. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency tolerance	-50		50	PPM
Duty Cycle	40	-	60	%
Peak to Peak Jitter			200	ps
Vih	1.4		AVDD33+0.3	V
Vil			0.4	V
Rise Time (10%~90%)			10	ns
Fall Time (10%~90%)			10	ns

6.1.3. SGMII Differential Transmitter Characteristics

Table 76. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	125	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.35UI
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

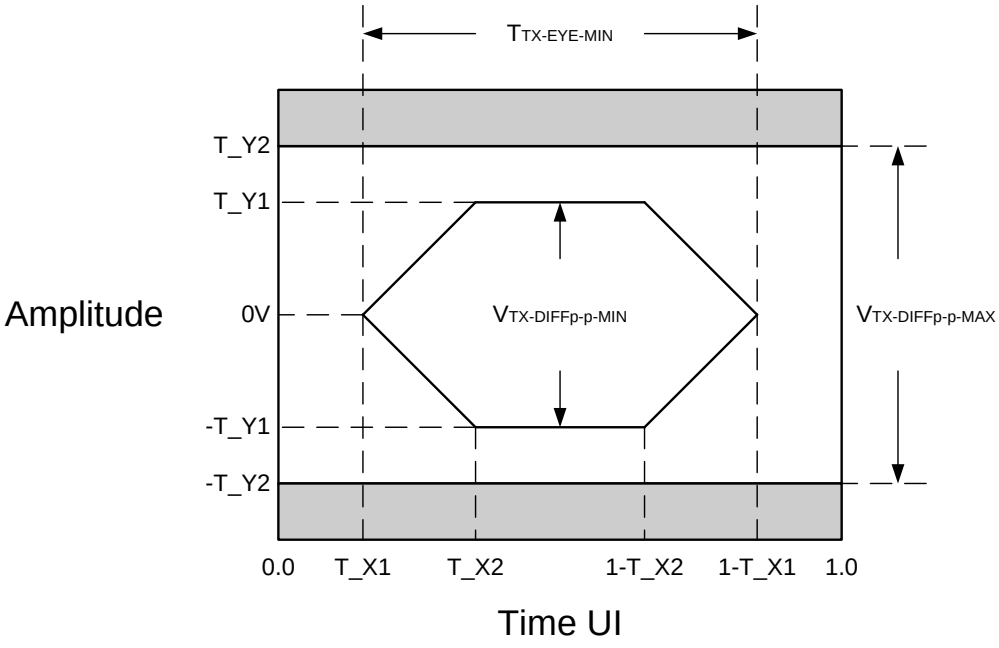


Figure 12. SGMII Differential Transmitter Eye Diagram

6.1.4. SGMII Differential Receiver Characteristics

Table 77. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI

Symbol	Parameter	Min	Typ	Max	Units	Notes
R_{RX}	Differential Resistance	80	100	120	ohm	-

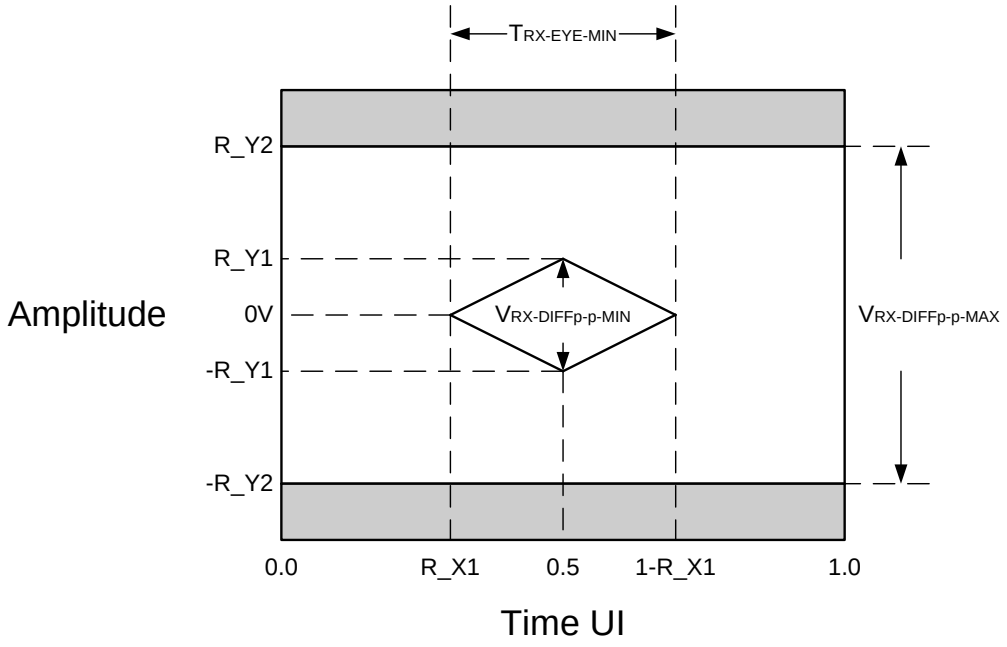


Figure 13. SGMII Differential Receiver Eye Diagram

6.1.5. MDC/MDIO Interface Characteristics

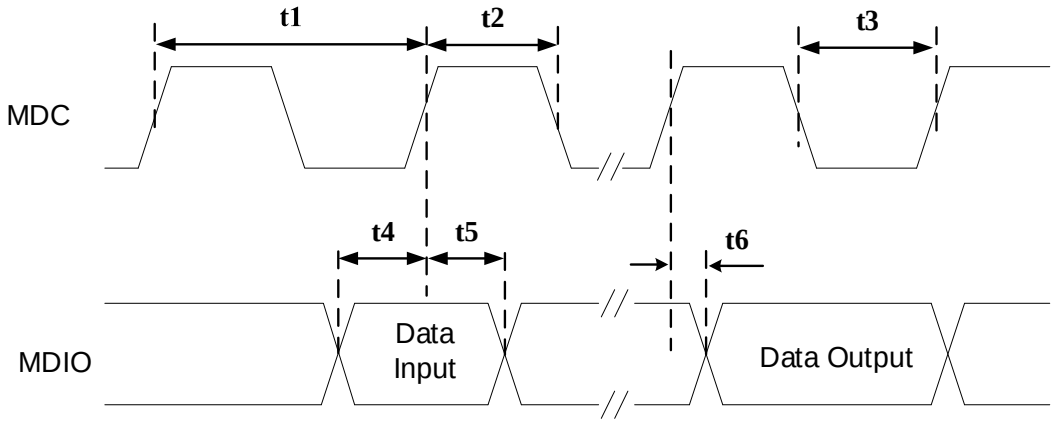


Figure 14. MDC/MDIO Timing Parameters

Table 78. MDC/MDIO Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	80	-	-	ns
t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns

Symbol	Description	Min	Typ	Max	Units
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7. Power Requirements

7.1. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
AVDDH	3.3 V power supply	-0.3	3.7	V
DVDDIO	3.3 V power supply	-0.3	3.7	V
AVDDL	1.2 V power supply	-0.2	1.5	V
DVDDL	1.2 V power supply	-0.2	1.5	V
PLLVDDL	1.2 V power supply	-0.2	1.5	
Junction Temperature			125	°C
Storage Temperature		-45	125	°C

7.2. Recommended Operating Conduction

Description	Pins	Min	Typ	Max	Unit
Power supply	DVDDIO	3.14	3.30	3.47	V
	AVDDH	3.14	3.30	3.47	V
	AVDDL	1.14	1.20	1.26	V
	DVDDL	1.14	1.20	1.26	V
	PLLVDDL	1.14	1.20	1.26	V
Ambient Operation Temperature Ta Industry		-40.00	-	85.00	°C
Ambient Operation Temperature Ta Commercial		0.00	-	70.00	°C

8. Mechanical and Thermal

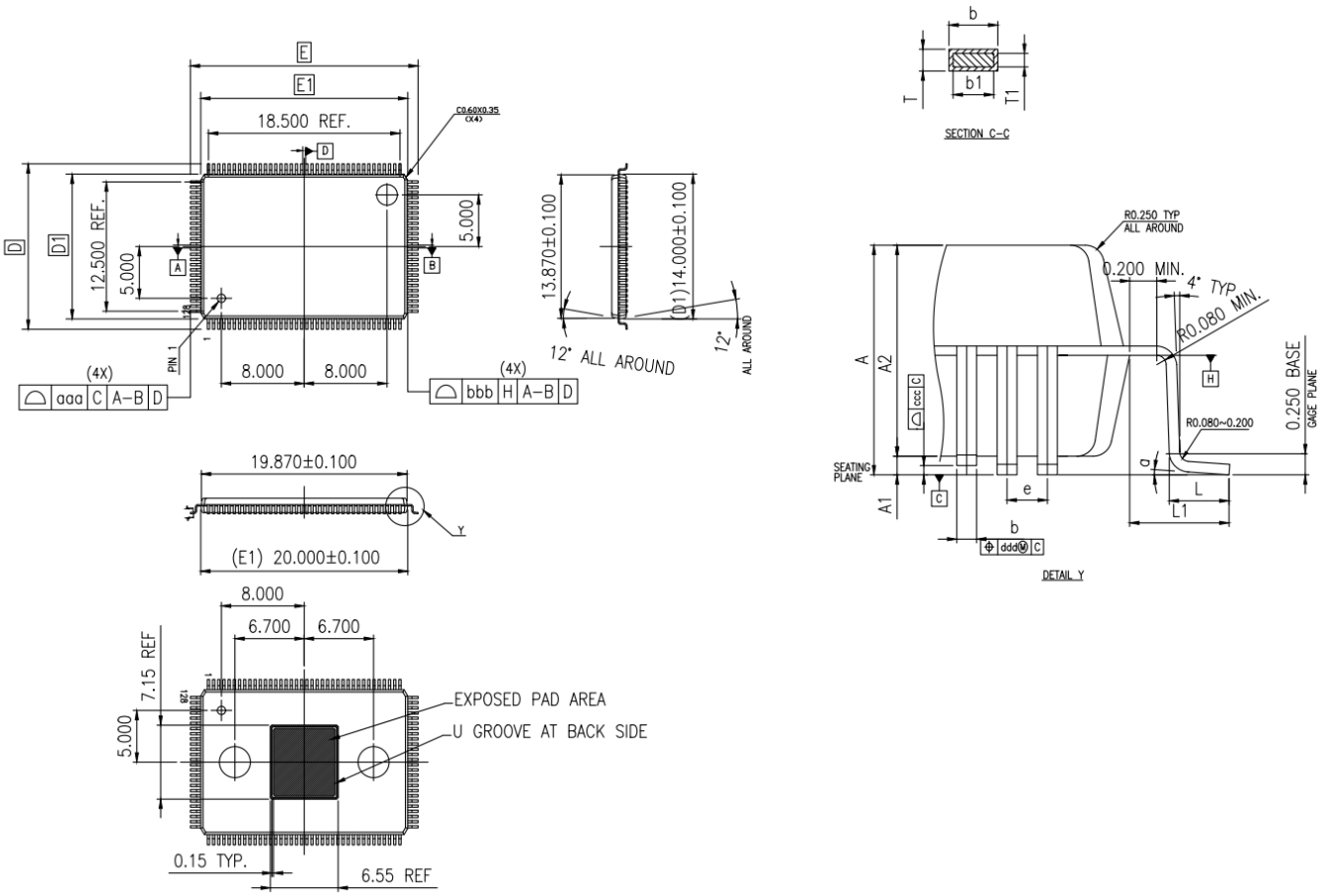
8.1. RoHS-Compliant Packaging

Motorcomm offers an RoHS package that is compliant with RoHS

RoHS-compliant parts have the letter G added to the top line of the part marking.

Part Number	Status	Package Qty	Op temp (℃)	Note
YT8618 C	Active	TBD	0 to 70	
YT8618 H	Active	TBD	-40 to 85	

9. Mechanical Information



DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.10±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.10	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	22.00±0.10	LEAD TIP TO TIP
7	E1	20.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF.	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	FRAME THICKNESS
11	T1	0.127±0.030	FRAME BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.05	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	aaa	0.20	PROFILE OF LEAD TIPS
17	bbb	0.20	PROFILE OF MOLD SURFACE
18	ccc	0.08	FOOT COPLANARITY
19	ddd	0.08	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

10. Ordering Information

Part Number	Package	Status	Operation Temp
YT8618 C XXXX	LQFP128		0 ~70°C
YT8618 H XXXX	LQFP128		-40 ~ 85°C