IS66066

4.8V to 16V Input, 12A Sync Step-Down Converter W/ Light Load Mode, Programmable Switching Frequency and Over Current Limit

Rev1.6 5/2020

Part Number	Input Voltage	Output Voltage	Current Rating
IS66066	4.8V~16V	0.6V~5.5V	12A

Description

The IS66066 is a high power density, fully integrated synchronous buck converter. It has wide input voltage range and can support up to 12A continuous output current at defined conditions. LDO is integrated internally, which is very suitable for single input supply condition. External bias is optional for maximizing the efficiency. A differential sensing scheme and a 0.6V internal feedback reference voltage achieve ±1% tolerance over full temperature range and perform an excellent line and load regulation.

Switching frequency can be easily adjusted among 600 kHz, 800 kHz and 1 MHz. The IS66066 uses patented Turbo Constant On Time (TCOT™) to control the algorithm with fast transient response. Pure MLCC output capacitors can be used to save space and cost.

The IS66066 has fully integrated protection features including OCP, NOCP, OVP, UVP and over temperature protection (OTP).

The IS66066 is available in a QFN 3mm x 4mm package with 21-Pin.

Moisture Sensitivity Leve 3.

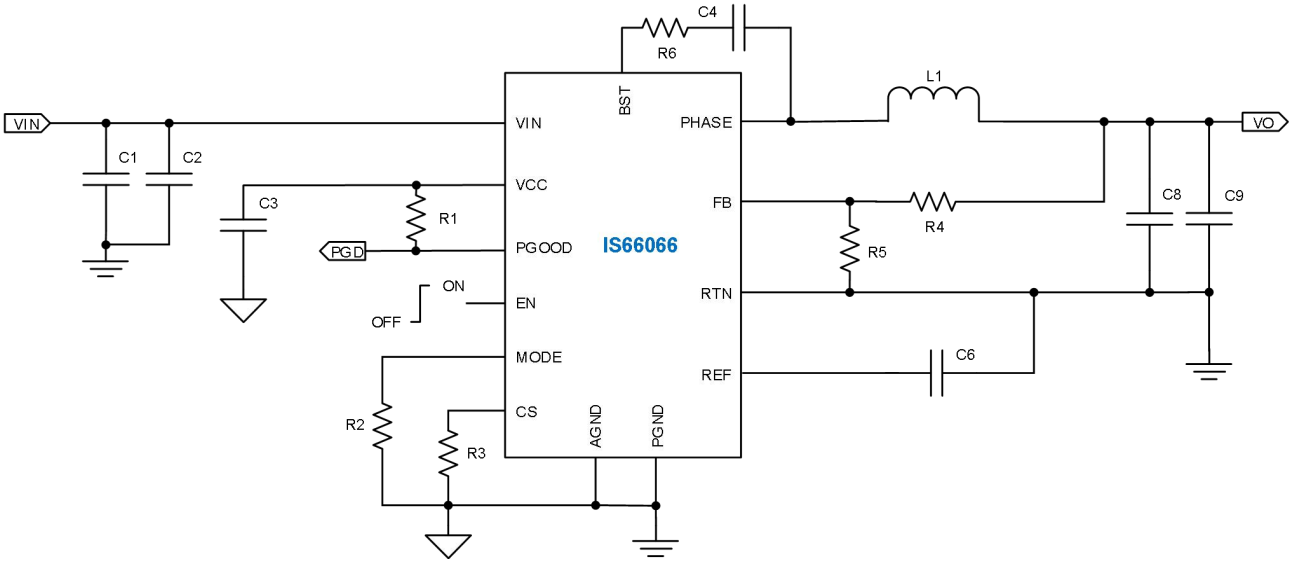
Applications

- Telecom/Datacom
- Computers and Servers
- Point of Load Module

Features

- Turbo Constant On Time (TCOT™) Control with Fast Transient Response.
- VIN Input Voltage Range: 2.4 V to 16V with External Bias VCC voltage, or 4.8V to 16V with Internal Bias VCC voltage.
- Output Voltage Range: 0.6V to 5.5V, and 90% Max Duty Cycle.
- 12A Continuous Output Current.
- Excellent Load and Line Regulations with 0.5% Voltage Accuracy.
- Up to 90% Efficiency at V_{IN}=12V, V_{OUT}=1.2V
- Differential Remote Sense
- Mode Selection between Pulse Skip and CCM at Light Load
- Output Voltage Track and Discharge
- Pre-bias Start-up
- Junction Temperature Range from -40ºC to 125ºC
- Programmable Soft-Start Time
- 1.0μA Current into VIN Pin during Shutdown
- Programmable Switching Valley Current Limit
- Adjustable Switching Frequency: 600kHz, 800kHz and 1MHz
- OCP, NOCP, OVP, UVLO and OTP
- QFN 3mm x 4mm Package with 21-Pin

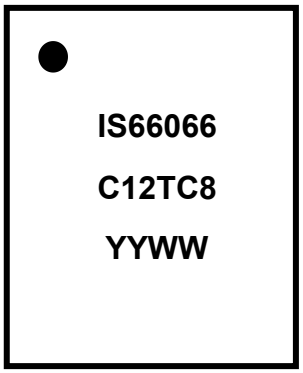
Typical Application Circuit



Order Information

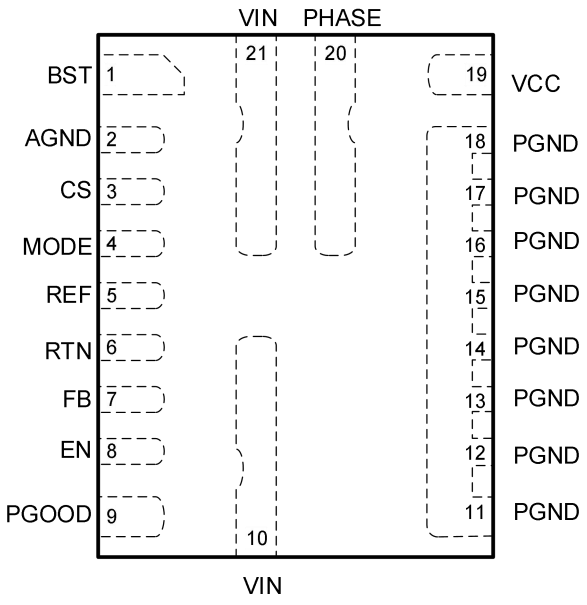
Part Number	Package	Shipping Method	Package Marking
IS66066	QFN-21(3mm x 4mm)	5000u Tape & Reel	IS66066

TOP MARKING (IS66066)



IS: Innovision Semiconductor prefix
6606: First five digits of the part number
C12TC8: Lot ID
Y: Year code
W: Week code

Package Reference



Top View

Absolute Maximum Ratings

Supply Voltage (V_{in})..... -0.3V to 20V
V_{cc}.....-0.3V to 5.5V
Switch Node Voltage (V_{PH}) DC.....-0.3V to 20V
Switch Node Voltage (V_{PH}) 25ns ..... -5V to 25V
BST Pin (V_{bst-sw}) DC..... -0.3V to 5.5V
All other pins.....0.3V to 5.5V
Junction Temperature (T_j).....150°C
Storage Temperature.....-65°C to 150°C

Thermal Ratings

θ_{JC} Max.....10°C/W
θ_{JB} Typ (Still Air, No Heat Sink).....8°C/W

Recommended Operating Conditions

Supply Voltage (V_{in}).....2.4V to 16V
V_{cc}.....3.0V to 5V
Output Voltage (V_o).....0.6V to 5.5V
Max Output Current (I_{o_max}).....12A
Junction Temperature (T_j).....-40°C to 125°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

Electrostatic Discharge	Standard	Value
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	±1500V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	±1000V

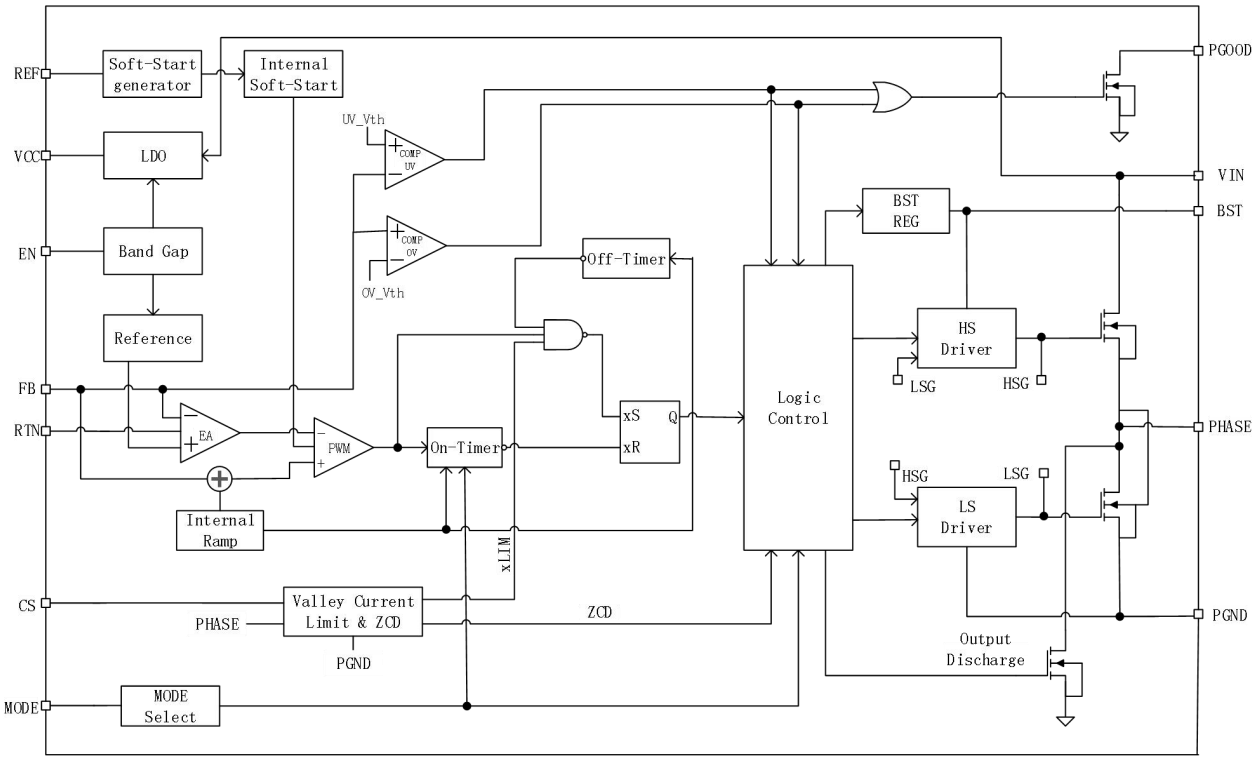
1). JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2). JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Pin Out and Package

IS66066(QFN-21)

Pin Number	Name	Description
1	BST	Bootstrap connection. Connect a capacitor between PHASE and BST, which is required to form a floating supply across the high-side switch driver.
2	AGND	Signal logic ground. A Kelvin connection to PGND is required.
3	CS	Current limit and inductor current report. Connect a resistor to AGND to set the valley current limit trip point. A voltage indicating the inductor current during operating.
4	MODE	Operation mode selection. Connect a resistor to AGND to set switching frequency and DCM/FCCM operation.
5	REF	Connect a capacitor to PGND to set soft start time or to an external reference for output voltage tracking. The capacitance of this capacitor determines the soft-start time.
6	RTN	Output remote sense feedback. Connect the pin to the negative side of the voltage sense point.
7	FB	Output remote sense return. An external resistor divider from the output to RTN (tapped to FB) sets the output voltage.
8	EN	Enable pin. An input signal turns the regulator on or off. Connect EN to VIN through a pull-up resistor. Do not float this pin.
9	PGOOD	Power good output with open drain. If the output voltage is within regulation, the pull-up resistor is required to indicate high.
10, 21	VIN	Supply voltage. Input to the power stage and internal LDO. Make the connection with wide PCB traces.
11~18	PGND	System ground. PGND is power ground of the power stage. Make the connection with wide PCB traces.
19	VCC	Internal 5V LDO output. Supply power for the drive and control circuits.
20	PHASE	Switch output. Switch node of power stage. Connect PH to the inductor and bootstrap capacitor. Make the connection with wide PCB traces.

FUNCTIONAL BLOCK DIAGRAM



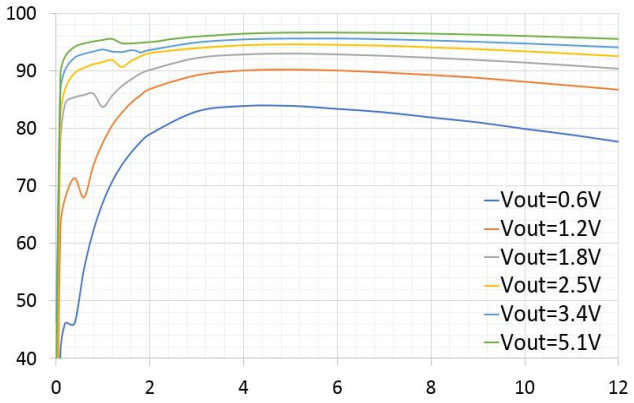
ELECTRICAL CHARACTERISTICS

Parameters		Definition/Datasheet			Units
		Min	Typ	Max	
SUPPLY VOLTAGE & CURRENT					
VIN Supply Voltage (with internal LDO)		4.8		16	V
VIN Supply Voltage (with external bias VCC voltage)		2.4		16	V
VIN Supply Current (Quiescent)	EN=2V ,V_{FB} = 0.62V		1700		μA
VIN Shutdown Current	EN="Lo"			10	μA
VCC Supply					
VCC Output Voltage (6V<VIN<16V)			4.8		V
VCC Output Current limit		25			mA
Load Regulation	Ivcc=25mA			2.2	%
DUTY CYCLE AND FREQUENCY CONTROL					
Switching frequency (Vin=12V, Vo=1V)	MODE=GND, CCM		600		kHz
	MODE=30.1K, CCM		800		kHz
	MODE=60.4K, CCM		1000		kHz
	MODE=VCC, DCM		600		kHz
	MODE=243K, DCM		800		kHz
	MODE=121K, DCM		1000		kHz
	MODE=15K, DCM		300		kHz
	MODE=7.5K, FCCM		300		kHz
Minimum On-Time			70	90	ns
Minimum Off-Time			180		ns
On-time at DCM (for DCM/CCM HYS)			120		%
Discharge					
Soft Discharge Transistor Resistance			180		Ω
MOSFET					
HFET R_{ds_on} (5V VCC)			13.2		mΩ
LFET R_{ds_on} (5V VCC)			4.5		mΩ
Switch Leakage			0	10	μA
SOFT START & FB					
VOUT=0% to VOUT=95%	C_{REFIN}=1nF		1.5		ms
Soft Start Delay Time			400		μs
FB Voltage	Tj=-40 to 125°C		600		mV
	Tj=-0 to 70°C		600		mV
REF Sourcing Current			36		μA
REF Sinking Current			12		μA

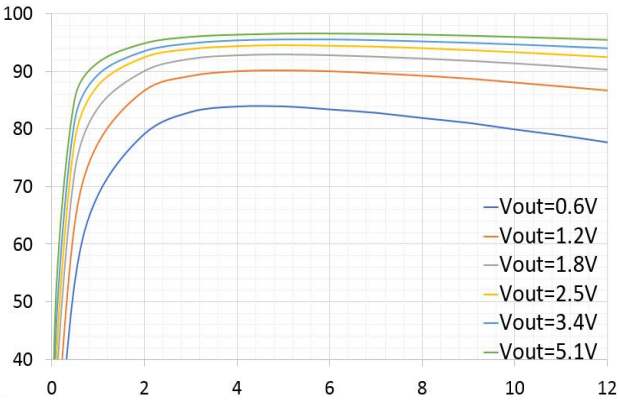
Power Good					
PGOOD Lower Threshold (rising edge) VOUT< Target		89	92.5	95	%
PGOOD Lower Threshold (falling edge) VOUT< Target		65	70	75	%
PGOOD Lower Threshold (rising edge) VOUT > Target			116		%
PGOOD Low to High Delay			0.9		ms
PGOOD Low Sink Current Capability @ 10mA				0.4	V
PGOOD Leakage Current VPG=3.3V				2.66	μA
PGOOD Low-Level Output Voltage	VIN=0V, 10KΩ Pull up		0.8	1	V
Current Limit					
Vcs Limit Voltage			0.6		V
Ics to Iout Ratio			10		μA/A
LS Negative Current Limit			-9		A
OSM (Output Sinking Mode)					
OSM Threshold (rising edge) VOUT< Target			105		%
OSM Threshold (falling edge) VOUT< Target			102		%
OSM Negative Current Limit			-4		A
OVP & UVP					
Output Over voltage (OVP)	Trip Threshold	113	116	119	%
	LS OFF threshold		50		%
Output Under voltage (UVP)	Trip Threshold	77	80	83	%
UVLO					
VCC UVLO	VCC rising		4.6		V
	Hysteresis		0.5		V
VIN UVLO	VIN rising		2.4		V
	Hysteresis		0.6		V
Enable					
EN Threshold Voltage	EN rising	1.15	1.22	1.25	V
EN Threshold Hysteresis			0.2		V
EN Input Current	EN=2V		0		μA
Thermal Protection					
Over Temperature (OTP)	Shutdown Temperature		160		˚C
	Hysteresis		30		˚C

TYPICAL PERFORMANCE

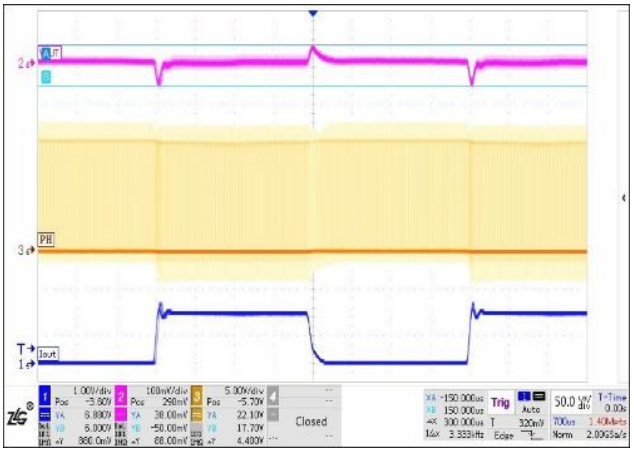
Efficiency
Pulse Skip, 800kHz



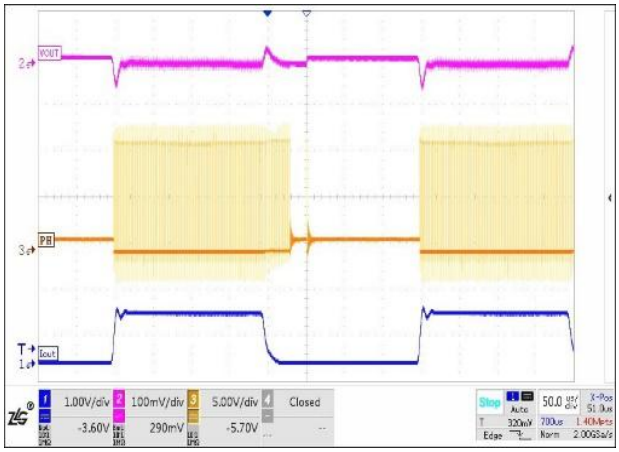
Efficiency
Forced CCM, 800kHz



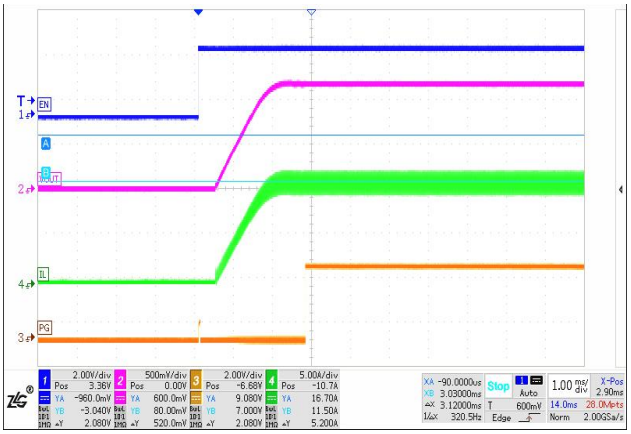
Load Transient
I_{OUT}=0-6A, Forced CCM



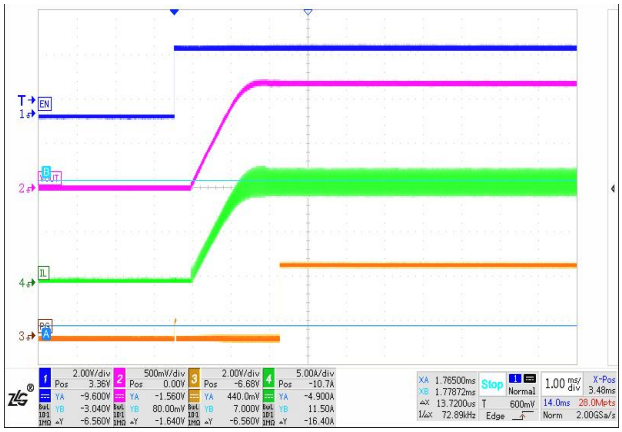
Load Transient
I_{OUT}=0-6A, Pulse Skip



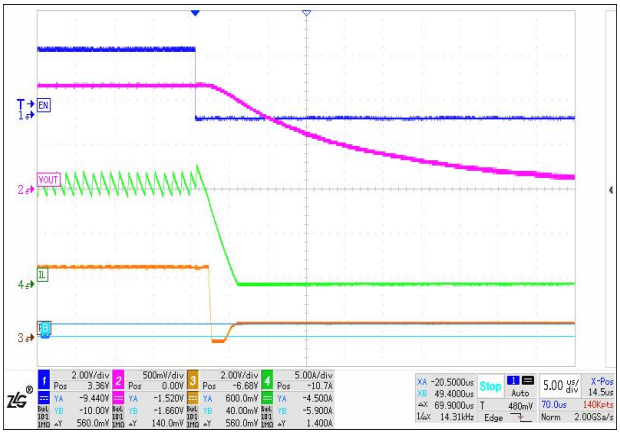
Power Up through EN
I_{OUT}=12A, Forced CCM



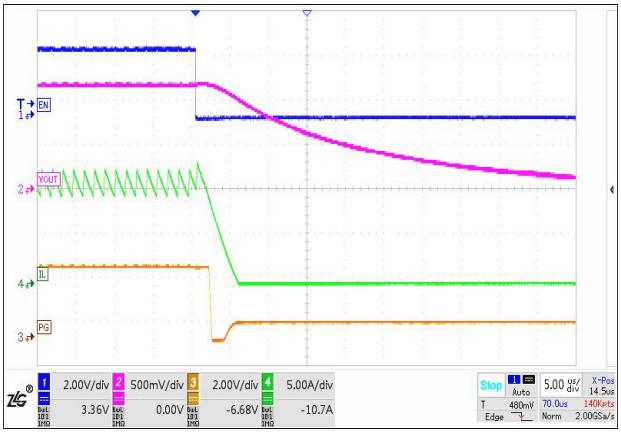
Power Up through EN
I_{OUT}=12A, Pulse Skip



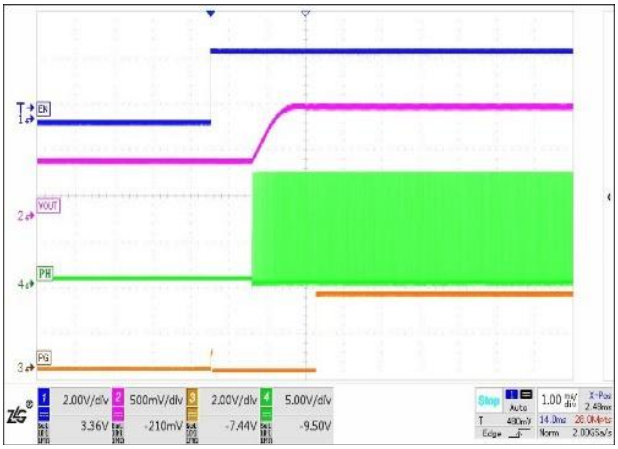
Power Down through EN
I_{OUT}=12A, Forced CCM



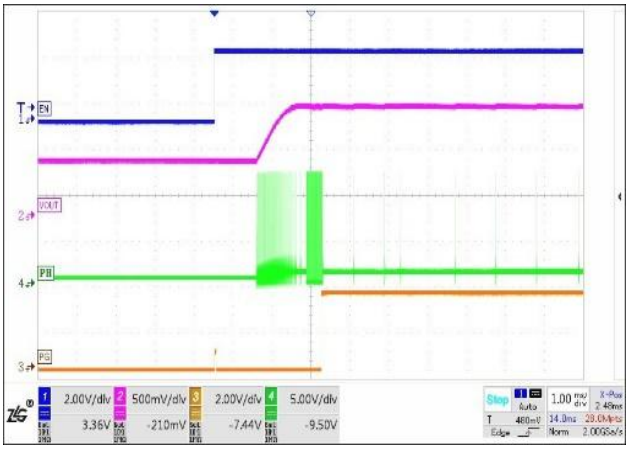
Power Down through EN
I_{OUT}=12A, Pulse Skip



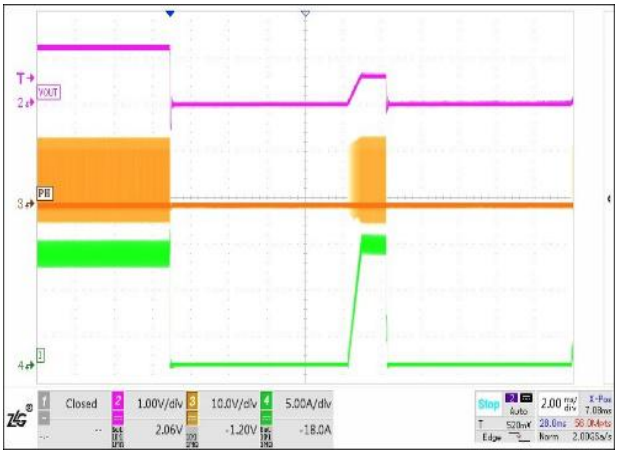
Pre-bias Start-Up
Forced CCM



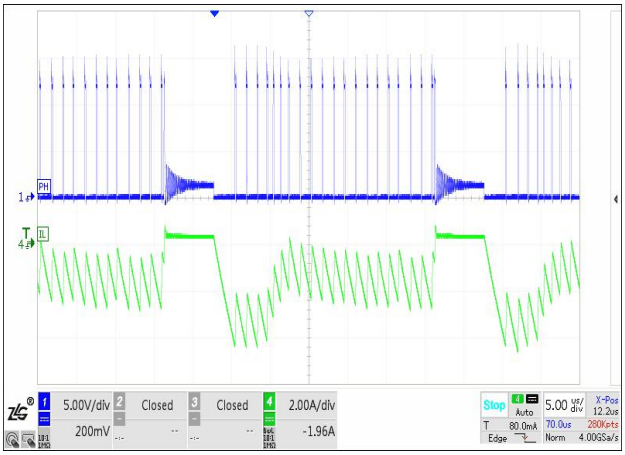
Pre-bias Start-Up
Pulse Skip



Over-Current Protection



OSM Operation
Pulse Skip



FUNCTIONAL INFORMATION

Product Overview

The IS66066 device is a high-efficiency, single channel, FET-integrated, synchronous buck converter. It is suitable for point-of-load applications with up to 12 A or lower output current in server, telecom, and similar digital applications. The device features proprietary Turbo Constant-On Time (TCOT™) (patent pending) to implement the transient algorithm with fast transient response. This patented architecture is built upon the adaptive constant on-time structure. The combination is ideal for building modern high/low duty ratio, ultra-fast load step response point of load DC-DC converters.

The IS66066 device has integrated MOSFETs rated at 12 A TDC.

The converter input voltage range is from 2.4 V up to 16 V. The output voltage ranges from 0.6 V to 5.5 V.

Stable operation with all ceramic output capacitors is supported, since the IS66066 uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require phase compensation network outside of the device which makes it easy to use and also enables low external component count. The designer may select the switching frequency from 3 preset values via resistor by MODE pin. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

FETs

The IS66066 device is a high-performance, integrated FET converter supporting current rating up to 20 A thermally. It integrates two N-channel FETs enabling high power density and small PCB layout area. The typical on-resistance, $R_{DS(on)}$, for the high-side MOSFET is 13.2 mΩ and typical on-resistance for the low-side MOSFET is 4.5 mΩ with a nominal gate voltage (V_{GS}) of 5 V.

Mode Selection

The IS66066 provides two modes of forced CCM operation and pulse skip under light load conditions. By switching the resistance of the resistor connected between MODE and RTN or VCC, 3 different switching frequencies and 2 light load modes can be achieved.

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243 kΩ (±20%) to GND	Pulse skip	800 kHz
121 kΩ (±20%) to GND	Pulse skip	1MHz
GND	Forced CCM	600 kHz
30.1 kΩ (±20%) to GND	Forced CCM	800 kHz
60.4 kΩ (±20%) to GND	Forced CCM	1MHz

Soft Start (SS)

The IS66066 device uses soft-start time to control the inrush current required to charge the output capacitor bank during startup. The minimum SS time is designed to be 1 msec. The SS time can be extended by adding a capacitor between REF pin and RTN pin. The soft start time can be determined by the following equation:

$$T_{SS}(ms) = \frac{C_{REF}(nF) \times 0.6(V)}{36(\mu A)}$$

Over-Current Protection (OCP)

The IS66066 device performs both positive and negative inductor current limiting functions. The current sense is done by on-die sensing and is cycle by cycle. The positive current limit is used to protect the inductor from saturation that might cause damage to the high side and low side FETs. The negative current limit protects the low side FET during OVP discharge. For IS66066, the negative current limit is fixed at 4

A where the low side FET is turned off for 200 nsec to limit the current.
During the low side FET ON state, the inductor current is sensed at PHASE node and mirrored to CS pin at a ratio of Gcs. By connecting a resistor (Rcs) from CS pin to AGND pin, the current limit value can be established. Please refer to the following equation to calculate the positive current limit threshold.

$$I_{LIM}(A) = \frac{V_{OCP}}{R_{CS} \times G_{CS}} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}}$$

Where, V_{OCP} = 0.6 V,
G_{CS} = 10 µA / A,
I_{LIM} = required output current limit (A).

The OCP hiccup operation is valid 3msec after IS66066 is enabled. Once OCP hiccup is enabled, if the IS66066 detects over-current condition for 31 consecutive cycles, or the FB falls below the under-voltage protection (UVP) threshold, it enters HICCUP mode. In HICCUP mode, the IS66066 immediately latches off the high side FET and latches off the LS-FET after detecting the zero crossing. At the same time, the REF capacitor is also being discharged. After about 11 msec, the IS66066 will attempt an automatic re-startup. If the over-current condition still exists after 3 msec operation, the IS66066 repeats this operation until the over-current condition disappears and the output voltage returns to the regulation level.

Feedback (FB)

FB and RTN pins are used for remote sensing purpose. Where feedback resistors are required for output voltage programming, the FB pin must be connected to the mid-point of the resistor divider, and the RTN pin must always be connected to the load return. FB and RTN pins are high-impedance input terminals of the differential remote sense amplifier. The feedback resistor divider should use resistor values much less than 100 kΩ. The output voltage of IS66066 can be adjusted by changing the resistor divider, R_{top} and R_{bot}. Calculate output voltage from R_{top} and R_{bot} using the formula below:

$$V_{OUT} = \frac{R_{top} + R_{bot}}{R_{bot}} \times 0.6V$$

Resistor Selection for Common Output Voltages is listed in the following table. The accuracy should be 1% or better to ensure voltage setpoint accuracy is satisfied.

$V_{OUT}(V)$	$R_{\text{top}}(\text{k}\Omega)$	$R_{bot}(\text{k}\Omega)$
1.0	2	3
1.2	4.02	4.02
1.8	4.02	2
3.3	8.2	1.8
5	8.2	1.1

Fault Protections

This section describes overvoltage protection, OSO limits, undervoltage protections and over temperature protections.

Undervoltage Protection and Overvoltage Protection

The IS66066 device monitors a feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 80% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 msec, the device latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 116% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off for 200 nsec before turning on again. The IS66066 device operates in this cycle until the output voltage is pulled down below 50% of the set point value. When OVP fault happens, PGOOD is latched off and will remain low until a reset of VCC or by re-toggling the EN pin.

Output Sinking Operation

The device has an output sinking operation (OSO) during overvoltage protection that protects the output load at a much lower overvoltage threshold of 4% above the target voltage. OSO protection does not trigger an

overvoltage fault, so the device is not latched off after an OSO event. OSO protection operates as an early no-fault overvoltage-protection mechanism. During the OSO operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. Once the negative current limit is reached, the low side FET is turned off for 200 nsec before turning on again. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs. The operation repeats itself until the FB voltage drops below 102% x setpoint value. The IS66066 exists OSO after 15 consecutive cycles of forced CCM.

Over Temperature Protection

The IS66066 device has overtemperature protection (OTP) by monitoring the die temperature. If the temperature exceeds the threshold value (default value 160°C), IS66066 device is shut off and discharges REF capacitor. When the temperature falls about 30°C below the threshold value, the device turns on with a soft start sequence. The OTP is a non-latch protection.

POWER GOOD (PGOOD)

The IS66066 device has a power-good output that registers high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within ±7.5% of the target value, internal comparators detect power-good state and the power good signal becomes high after an 0.8 msec delay. If the output voltage falls below 80% of the target value, exceeds 116% of the target value, the power good signal latches off low. The open-drain power-good output must be pulled up externally to VCC or another voltage source of less than 3.6 V via a pull up resistor (10 kohm is recommended). The internal N-channel MOSFET does not pull down until the input voltage is applied. Once power-good is latched off, it can only be pulled high after a new soft-start sequence and output voltage is within the power-good window.

Application Implementation

The IS66066 device is a highly-integrated synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 12 A. Use the following design procedure to select key component values for this family of devices.

Design Input:

Vin = 12 V

Vin_max = 13.2 V, Vin_min = 10.8 V

Vout = 1 V +/- 5% (1% DC, 1% ripple, 3% transient)

Design Requirements:

$Iout_{max}$ = 12 A

Iocl = 15 A

Load Step ΔI_{LOAD} = 60% x Imax

di/dt = 10 A/μsec

Fsw = 600 kHz

Tss = 1 msec

Forced CCM Operation

Design Procedure:

1. Switching Frequency Selection

Select a switching frequency for the regulator. There is a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 600 kHz achieves both a small solution size and a high-efficiency operation with the frequency selected.

Select one of 3 switching frequencies from the MODE table below. In addition to serving the frequency select purpose, the MODE pin can also be used to program light-load conduction mode. For IS66066, there are two light load operations to choose. One is Pulse Skip mode and the other is Continue Conduction mode.

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243 kΩ(±20%) to GND	Pulse skip	800 kHz
121 kΩ(±20%) to GND	Pulse skip	1MHz
GND	Forced CCM	600 kHz
30.1 kΩ(±20%) to GND	Forced CCM	800 kHz
60.4 kΩ(±20%) to GND	Forced CCM	1MHz

2. Inductor Selection

To calculate the value of the output inductor, use the following equation.

$$\text{Lout} = \frac{\text{Vout}}{(\text{Vin}_{\max} \times \text{fsw})} \times \frac{\text{Vin}_{\max} - \text{Vout}}{\text{Iout}_{\max} \times \text{Kind}}$$

The coefficient K_{ind} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, maintain a K_{ind} coefficient between 0 and 0.50 for balanced performance. Using this target ripple current, the required inductor size can be calculated using the equation provided above.

Selecting a K_{ind} of 0.25, the target inductance L_{out} = 0.5 μH. Using the standard value, the 0.5 μH is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using the following 3 equations. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{\text{Vout}}{(\text{Vin}_{\max} \times \text{fsw})} \times \frac{\text{Vin}_{\max} - \text{Vout}}{L_{OUT}}$$

$$IL_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times {I_{RIPPLE}}^2}$$

$$IL_{PEAK} = I_{OUT} + \frac{1}{2} \times I_{RIPPLE}$$

Choose an inductor that does not saturate under the maximum peak inductor current. Also, choose an inductor that gives the best thermal performance under the above calculated RMS current.

3. *Output Capacitor Selection*

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

Minimum Output Capacitance to Ensure Stability

To prevent sub-harmonic multiple pulsing behavior, IS66066 application designs must strictly follow the small signal stability considerations describe in the following equation.

$$C_{OUT\_\min} > \frac{t_{ON}}{2} \times \frac{8\tau}{L_{OUT}} \times \frac{V_{REF}}{V_{out}}$$

where

- $C_{OUT(min)}$ is the minimum output capacitance needed to meet the stability requirement of the design
- t_{ON} is the on-time information based on the switching frequency and duty cycle (in this design, 100 ns)
- τ is the ramp compensation time constant of the design based on the switching frequency and duty cycle (in this design, 1 µsec)
- L_{OUT} is the output inductance (in the design, 0.39 µH)
- V_{REF} is the reference voltage level (in this design, 0.6 V)
- V_{OUT} is the output voltage (1 V)

The stability is ensured when the amount of the output capacitance is greater than the minimum required value. And when all MLCCs (multi-layer ceramic capacitors) are used, both DC and AC derating effects must be considered to ensure that the minimum output capacitance requirement is met with sufficient margin.

For Constant on time topology, the minimum capacitance required by the stability is much smaller than that is required by the load transient.

Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

For normal applications with less than 10% duty cycle, the output voltage deviation during a dynamic load release determines how much output capacitance is needed.

Use the next equation to estimate the amount of capacitance needed for a given dynamic load release.

$$C_{OUT\_\text{LoadRelease}} = \frac{L_{OUT} \times {\Delta I_{LOAD}}^2}{2 \times \Delta V_{Load\_Release} \times V_{OUT}}$$

In general applications where the overall output voltage tolerance is +/-5%, the allowed transient voltage deviation during the worst case load release can be set at around 3% depending on how much output voltage setpoint accuracy (1% in this design) and the ripple voltage requirement (1% in this design). The minimum output capacitance to meet the overshoot requirement can be calculated using the above equation. This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.

- POSCAP bank #1: 2 x 330 µF, 2.5 V, 6 mΩ per capacitor

- MLCC bank #2: 3 × 47 µF, 2.5 V, 1 mΩ per capacitor with DC+AC derating factor of 50%

Recalculating the worst case overshoot using the described capacitor bank design, the overshoot needs to be 30 mV or less which meets the 3% overshoot transient specification requirement.

Output Voltage Ripple

The output voltage ripple is another important design consideration. The following equation calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$Cout_{\min\_Ripple} = \frac{I_{RIPPLE}}{8 \times F_{SW} \times V_{OUT\_RIPPLE}}$$

In this example, the maximum output voltage ripple is 9.7 mV. Because this capacitance value is significantly lower compared to that of transient load release, determining the output capacitance bank using the worst case load release requirement is generally adequate. Because the output capacitor bank consists of both POSCAP and MLCC type capacitors, it is important to consider the ripple effect at the switching frequency due to effective ESR.

For detailed calculations, please contact the factory to obtain a user-friendly Excel based design tool.

4. Input Capacitor Selection

The IS66066 devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the VCC pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the VIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using the equation below.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into consideration. For this design example, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. For this design, allow 0.1 V input ripple for $V_{RIPPLE(cap)}$, and 0.3 V input ripple for $V_{RIPPLE(esr)}$. the minimum input capacitance for this design is 38.5 µF, and the maximum ESR is 9.4 mΩ. For this example, four 22 µF, 25 V low-ESR polymer capacitors in parallel were selected for the power stage.

Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

5. R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the IS66066 within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the PHASE area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this design twin 2.2 nF, 25 V, 0603 sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness. Its ideal placement is shown in PCB layout guidelines.

PCB Layout Guidelines

Efficient PCB layout is crucial to the stable operation of the circuit. For best performance, refer to the figure in the PCB layout column and follow the PCB layout recommendations below.

1. The input MLCC capacitor shall be as close as possible to the VIN and PGND pins and the main MLCC capacitor shall be placed on the same wiring layer as IS66066. The copper plane of VIN and PGND can be maximized to minimize the parasitic impedance.

2. A capacitor with a minimum capacitance of 0.1 μF must be close to pin 10 which is the VIN pin. At least two 20/10 mil vias are required to connect the grounding end of the capacitor to the ground plane of the PCB board.

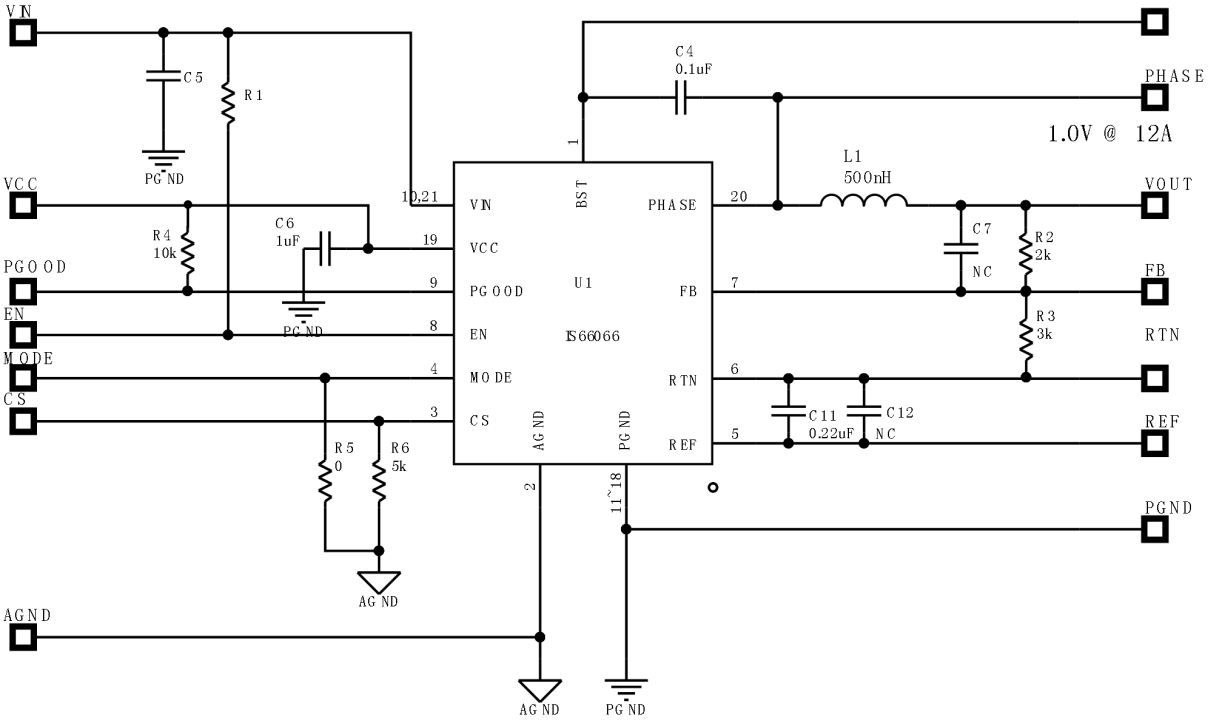
3. Place as many PGND holes as possible nearest to the PGND pin to minimize parasitic impedance and thermal resistance.

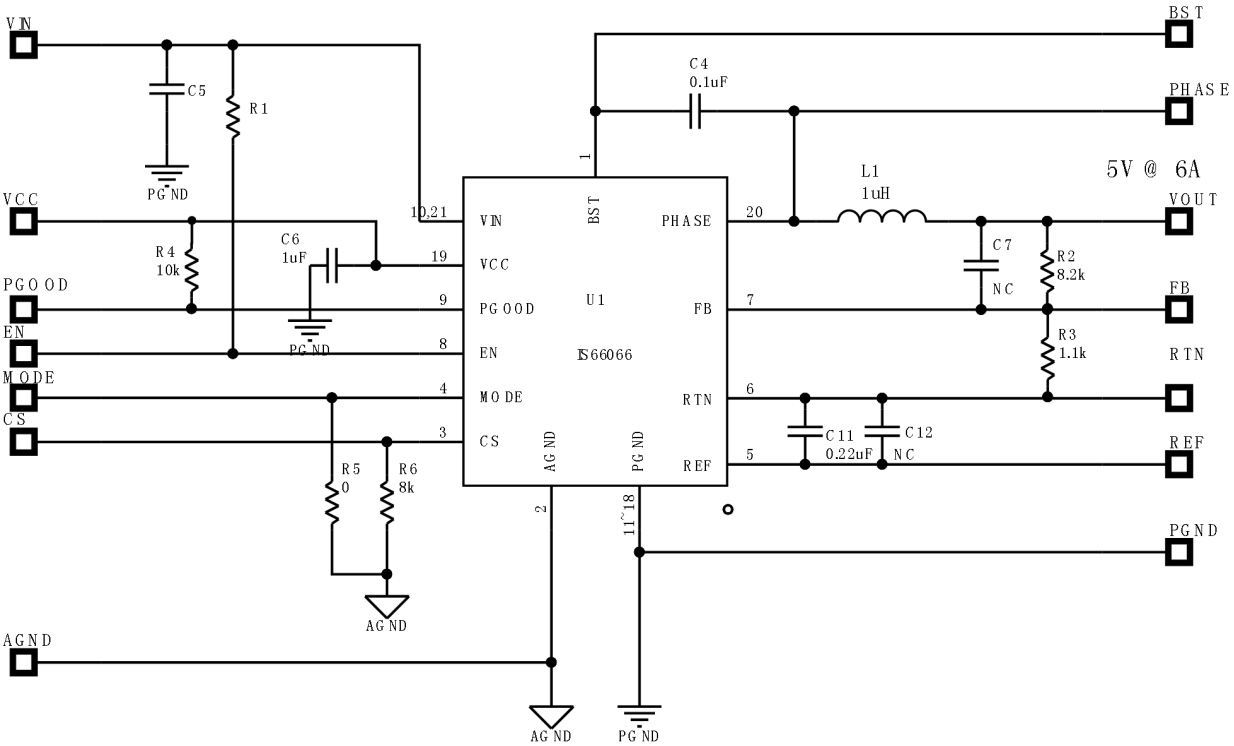
4. VCC capacitor should be placed as close to the IS66066 as possible. Connect AGND and PGND at VCC capacitor's grounding point.

5. Place the BST capacitor as close as possible to BST and SW. Routing widths should be greater than 20 mm. It is recommended to use a 0.1 μF to 1 μF bootstrap capacitor. Place the BST resistance between the IC and the BST capacitor to achieve Damping effect. It is recommended to use a 3.3 Ω resistance.

6. Place the REF capacitor close to REF and connected to the RTN. It is recommended to use a 22 nF capacitor.

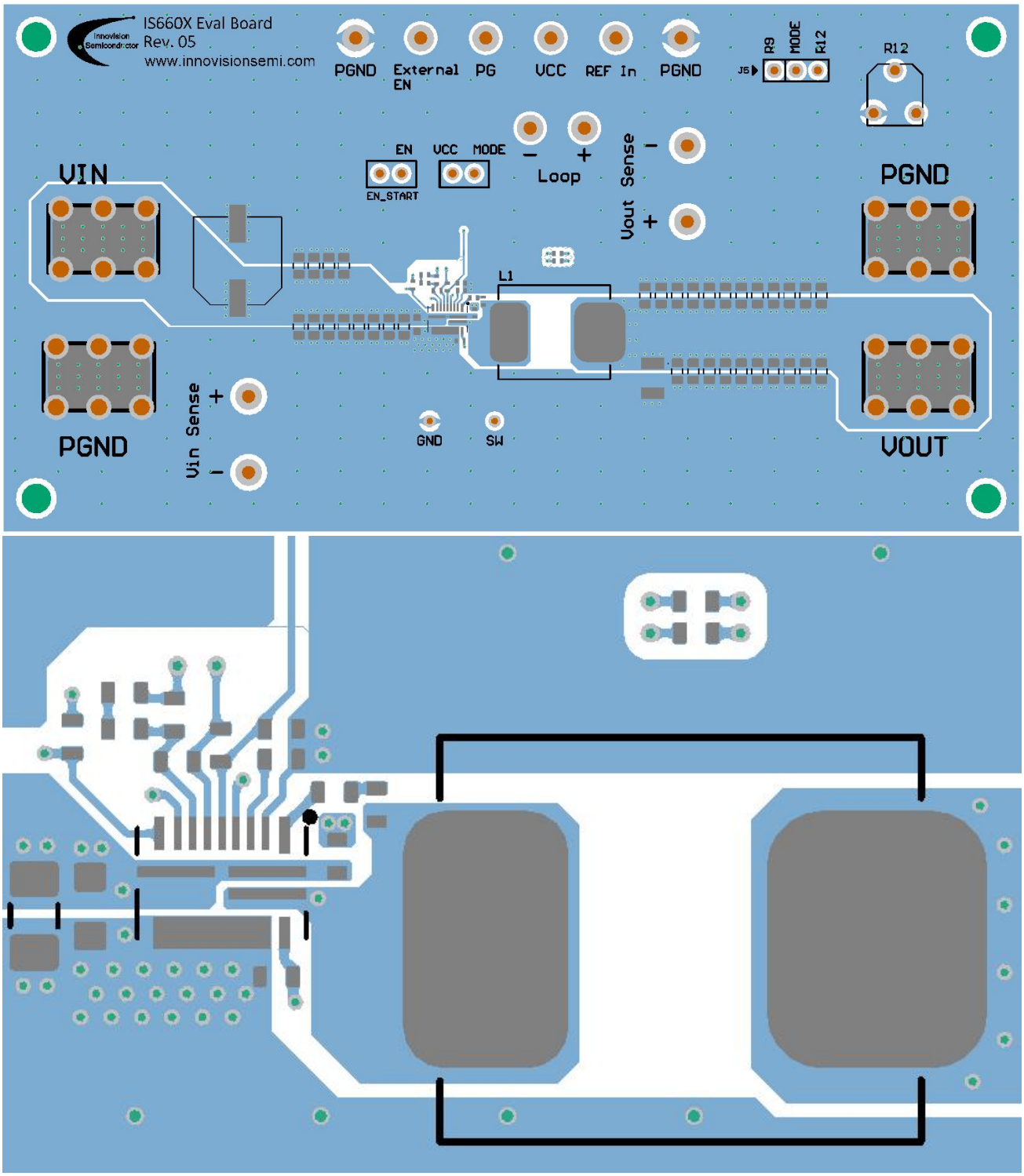
Typical Application Circuits



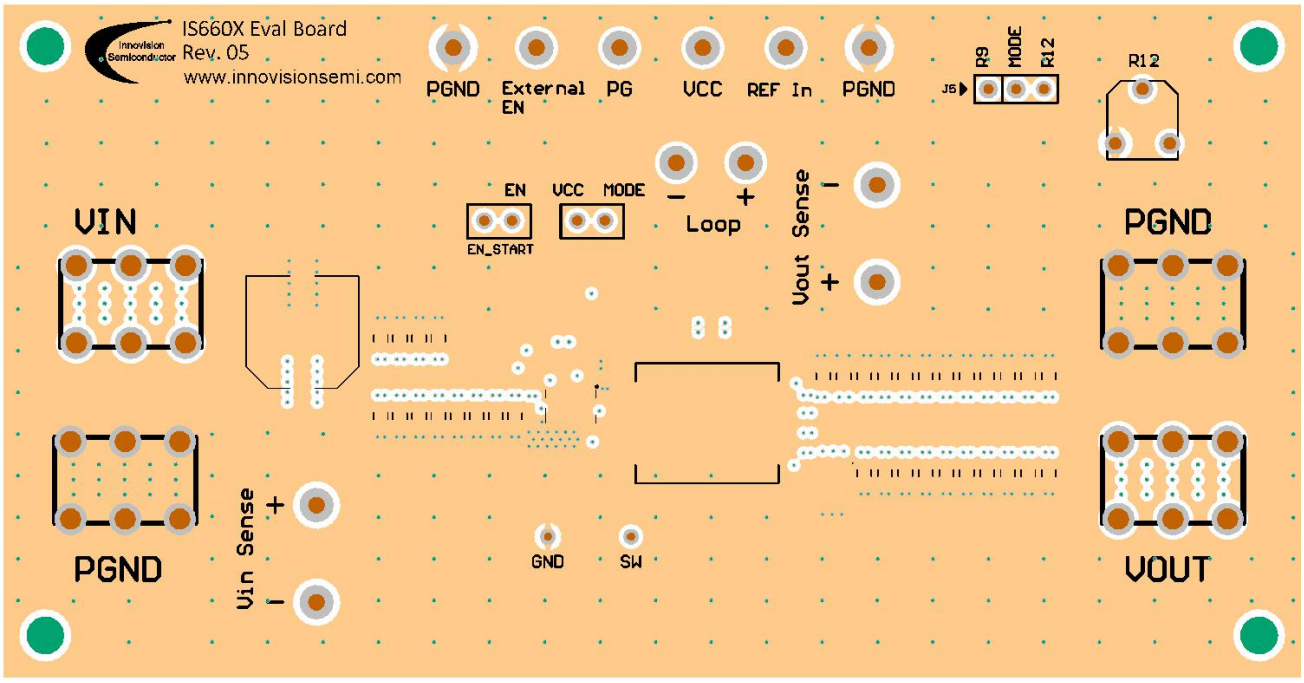


PCB layout

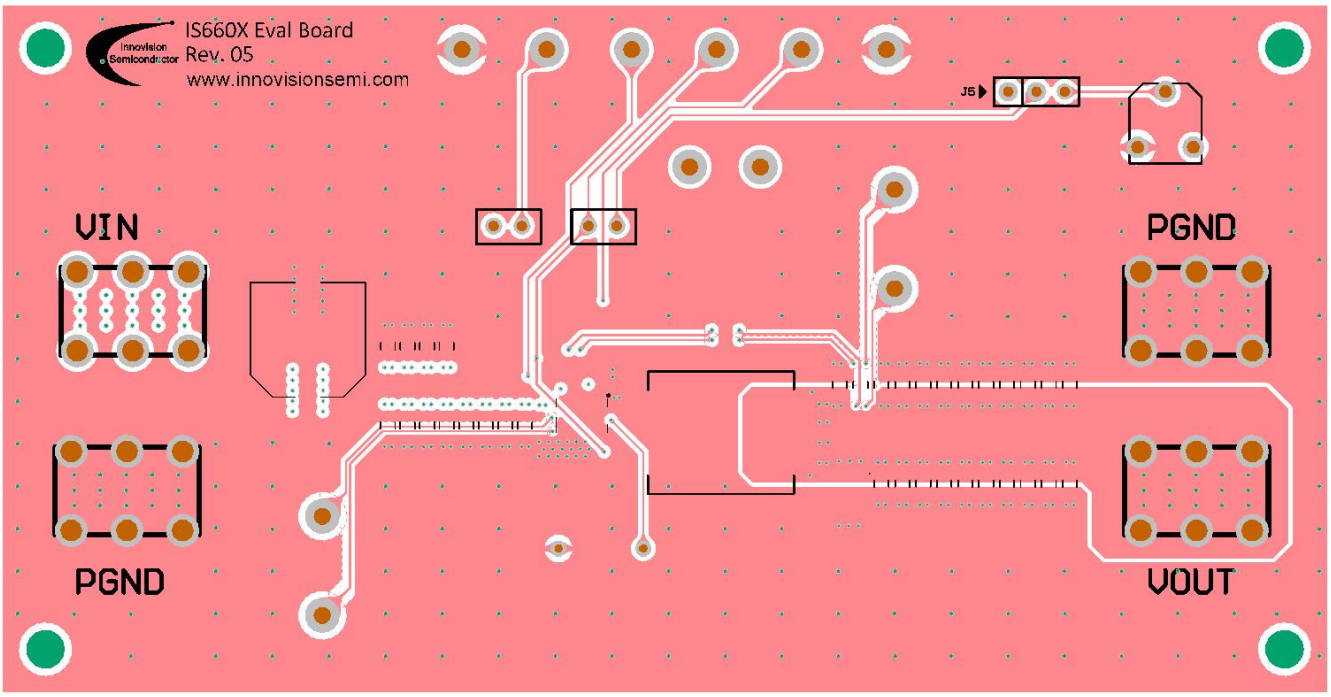
(1) Top Layer



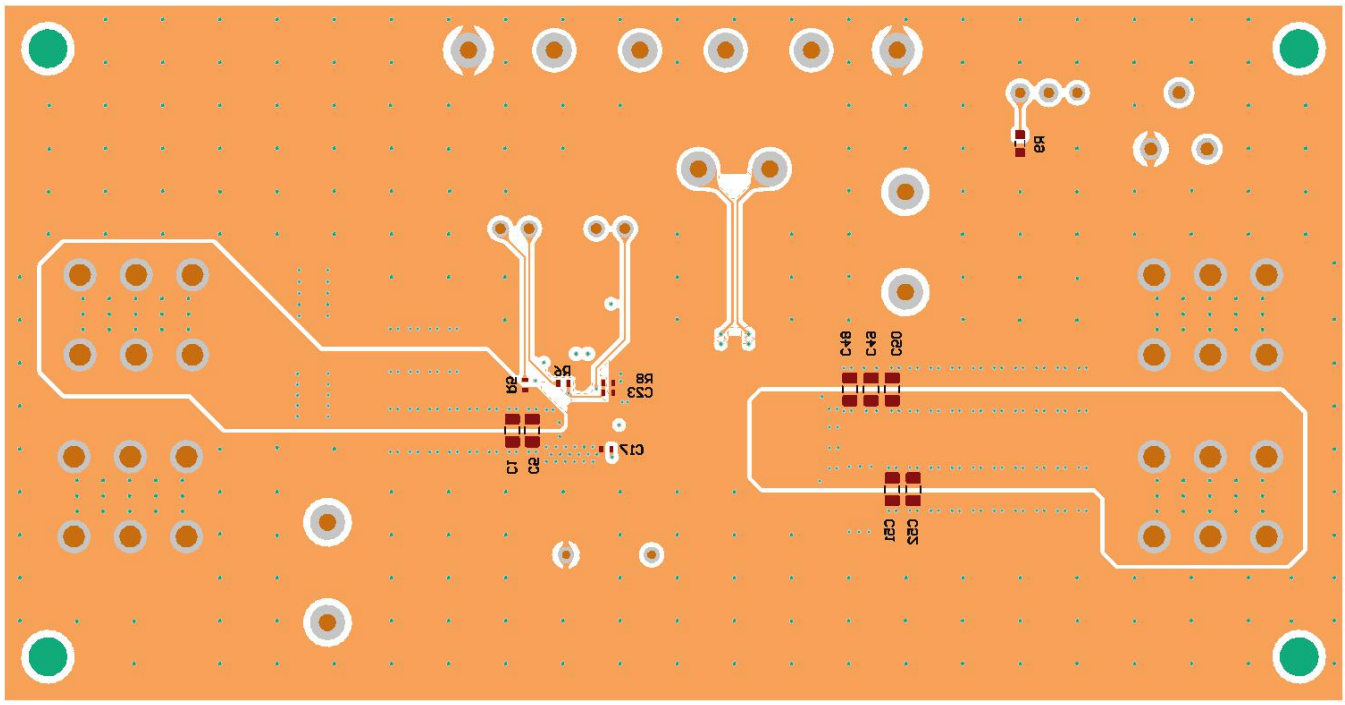
(2) Layer 2



(3) Layer 3

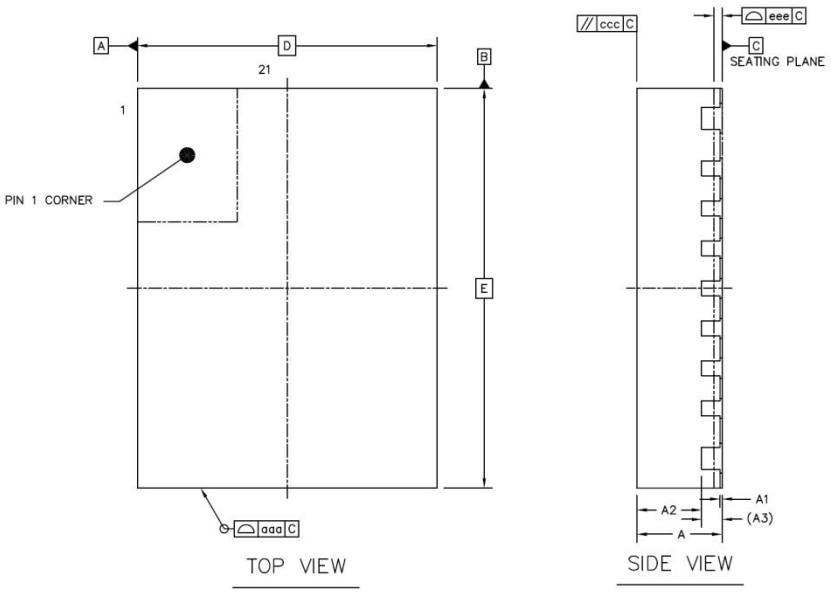


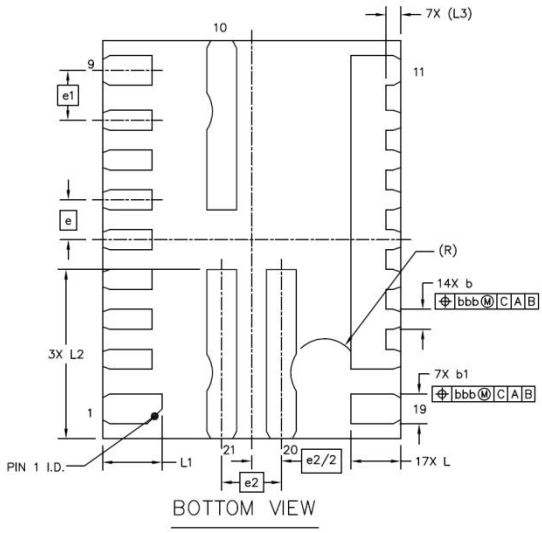
(4) Bottom Layer



Package Dimension

QFN-21(3mm X 4mm)

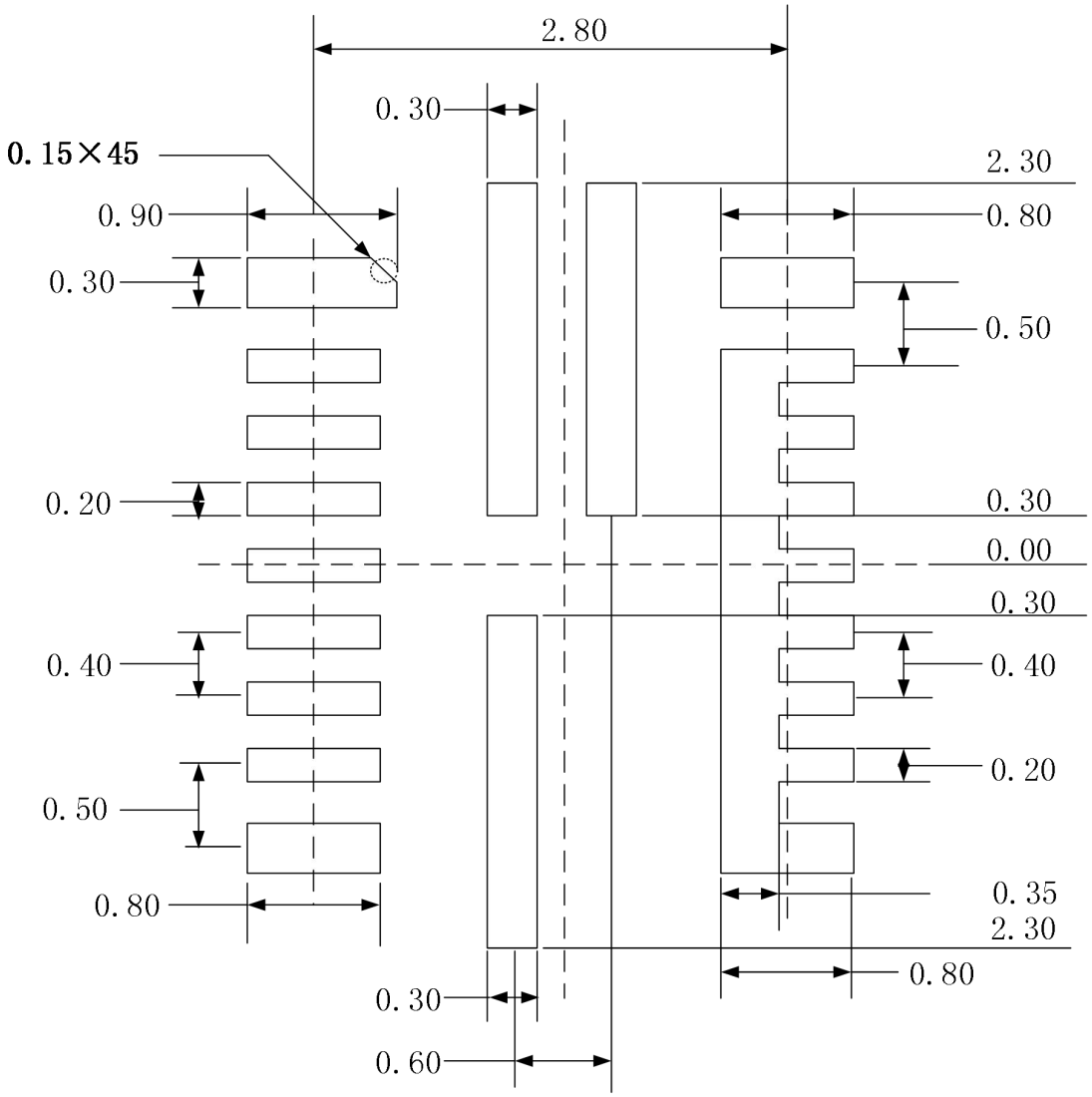




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
		b1	0.25	0.3	0.35
RADIUS		R		0.34 REF	
BODY SIZE	X	D		3 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
		e1		0.5 BSC	
		e2		0.6 BSC	
LEAD LENGTH		L	0.4	0.5	0.6
		L1	0.5	0.6	0.7
		L2	1.6	1.7	1.8
LEAD EDGE TO PKG EDGE		L3		0.15 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	

Unit: mm

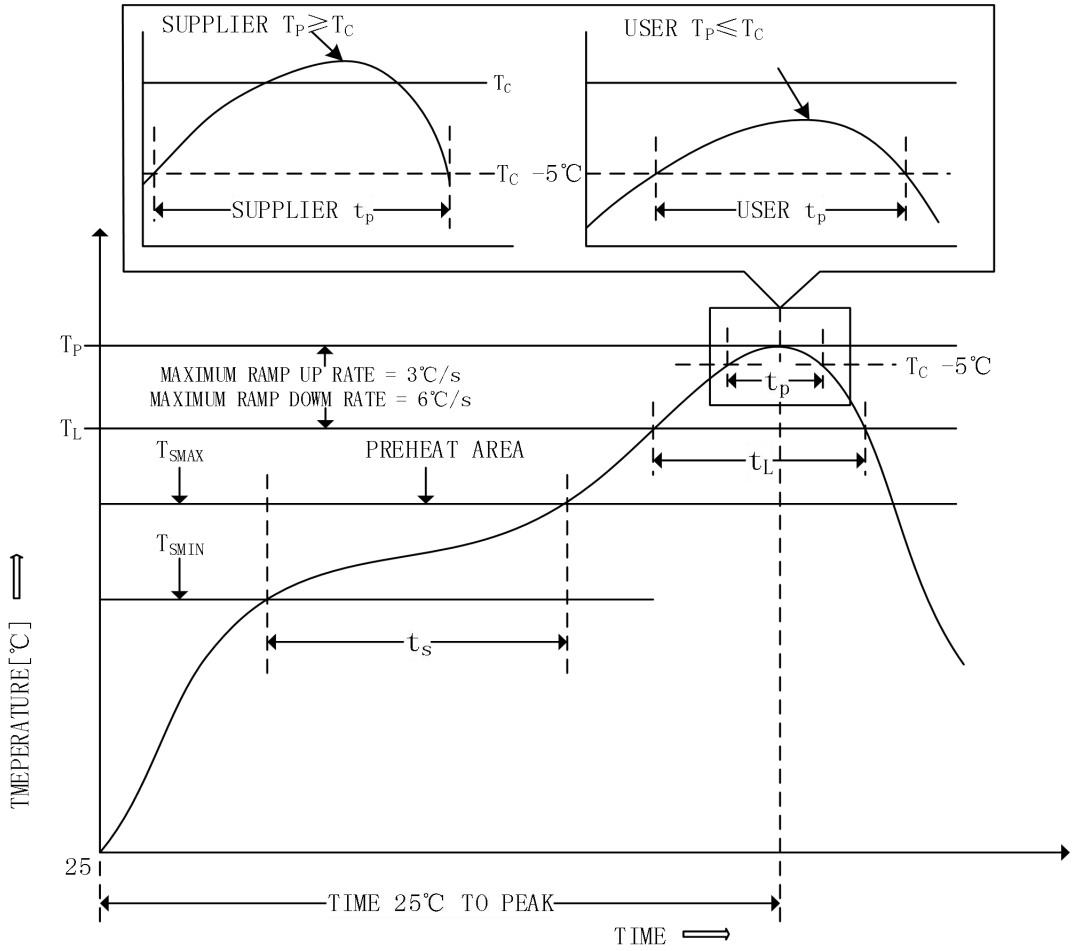
RECOMMENDED LAND PATTERN



Reflow Specification

Qualification Reflow: The IS6606 was qualified in accordance with IPC/JEDEC J-STD-020D.01. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder reflow attachment phase of PCB assembly.

The qualification preconditioning process specifies a sequence consisting of a bake cycle, moisture soak cycle (in a temperature humidity oven), and three consecutive solder reflow cycles, followed by functional device testing.



Production Reflow:

PROFILE FEATURE	SN - PB EUTECTIC ASSEMBLY	PB-FREE ASSEMBLY
Peak package body temperature (TP)	For users, TP must not exceed T_C(235℃).For suppliers, TP must equal or exceed T_C(235℃).	For users, TP must not exceed T_C(260℃).For suppliers, TP must equal or exceed T_C(260℃).

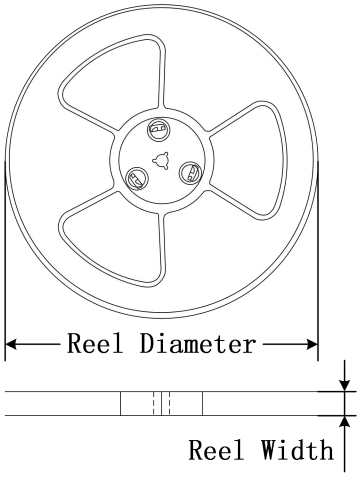
Storage Specifications

The storage specification of the IS6606 conforms to IPC/JEDEC J-STD-020D.01 Moisture Sensitivity Level (MSL) 3.

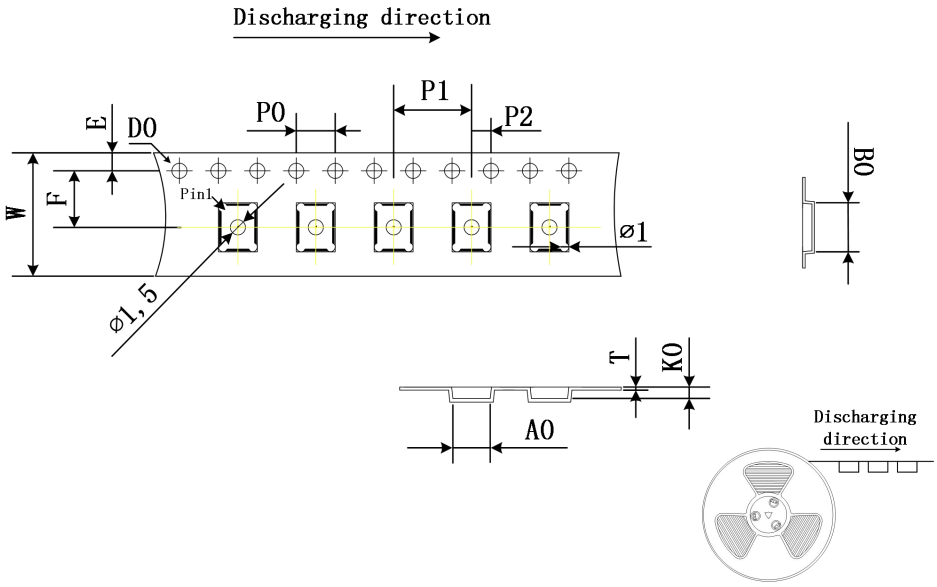
After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60%RH

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter (inch)	Reel Width （mm）
QFN-21(3 x 4)	13″	

NOTE:

1). The cumulative error of any 10 ratchet holes shall not exceed ±0.2mm

2). The non-parallelism of 100mm long carrier band in the carrier band length direction shall not exceed 1mm.

3). All dimensions are in accordance with EIA-481-3

4). Material: black, PS material, thickness 0.3±0.05mm.

5). The picture is only for reference. Please make the object as the standard.

Unit(mm)

ITEM	W	A0	B0	K0	P0	P1	P2	F	S	E	D0	T
DIM	12 ±0.30	3.20 ±0.1	4.20 ±0.1	0.85 +0.1 -0.05	4.00 ±0.1	8.00 ±0.1	2 ±0.1	5.5 ±0.1	0.0 ±0.1	1.75 ±0.1	1.5 +0.10 -0.00	0.3 ±0.05