IS6605A

4V to 16V Input, 6A Sync Step-Down Converter W/ Light Load Mode, Programmable Switching Frequency and Over Current Limit

Rev2.0 6/2020

Innovision Semiconductor

Part Number	Input Voltage	Output Voltage	Current Rating
IS6605A	4V~16V	0.6V~5.5V	6A

Description

The IS6605A is a fully integrated, high-frequency, synchronous, step-down converter. It provides a very compact solution that achieves up to 6A output current with excellent load and line regulation over wide input voltage range. IS6605A has high working efficiency over its output current load range.

IS6606 uses proprietary Turbo Constant-On-Time (TCOT^{TM}) control with internal compensation to provide fast transient response and simplified loop stability.

The switching frequency can be easily set to 600kHz, 1.1MHz, 1.5MHz or 2MHz. The switching frequency of IS6605A remains constant regardless of input and output voltages.

The soft start process is controlled by an internal 1.5msec timer, which can be increased by adding a capacitor from TRK / REF to GND. The open-drain power good (PGOOD) signal indicates whether the output is within its nominal voltage range. When the input power fails to power the IS6605A, PGOOD is clamped at about 0.7V by an external pull-up voltage.

The IS6605A is equipped with full suites of protection functions which includes over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The IS6605A is available in a 14-pin QFN (2mmx3mm) package.

Moisture Sensitivity Leve 3.

Features

- Turbo Constant-On-Time (TCOT^{TM}) Control with Fast Transient Response.
- VIN Input Voltage Range: 2.7 V to 16V with External Bias VCC voltage, or 4V to 16V with Internal Bias VCC.
- Output Voltage Range: 0.6V to 5.5V, and 90% max duty cycle.
- 6A Continuous Output Current.
- Excellent Load and Line Regulations with 0.5% Voltage Accuracy.
- Up to 90% Efficiency at V_{IN}=12V, V_{OUT}=1.8V
- Mode Selection between Pulse Skip and CCM at Light Load
- PGOOD Active Clamp at Low Level during a Power Outage
- Programmable Soft-Start time
- 1.0µA Current into VIN Pin during Shutdown
- Programmable Switch Valley Current Limit
- Adjustable Switching Frequency: 600kHz, 1.1MHz, 1.5MHz and 2MHz
- OCP, NOCP, OVP, UVLO and OTP
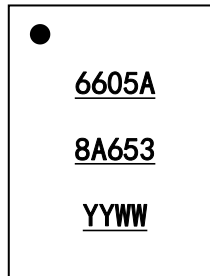- QFN 2mm x 3mm Package with 14-Pin

Applications

- Telecom/Datacom
- Computing and Servers
- Point of Load Module
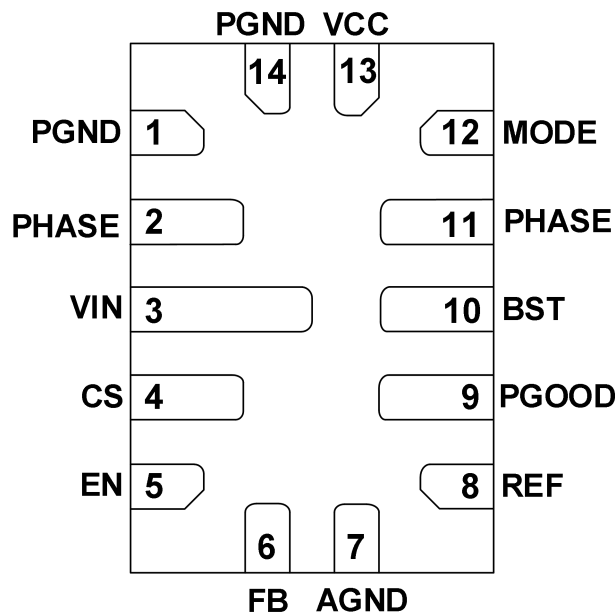- Computing and Servers

Typical Application Circuit
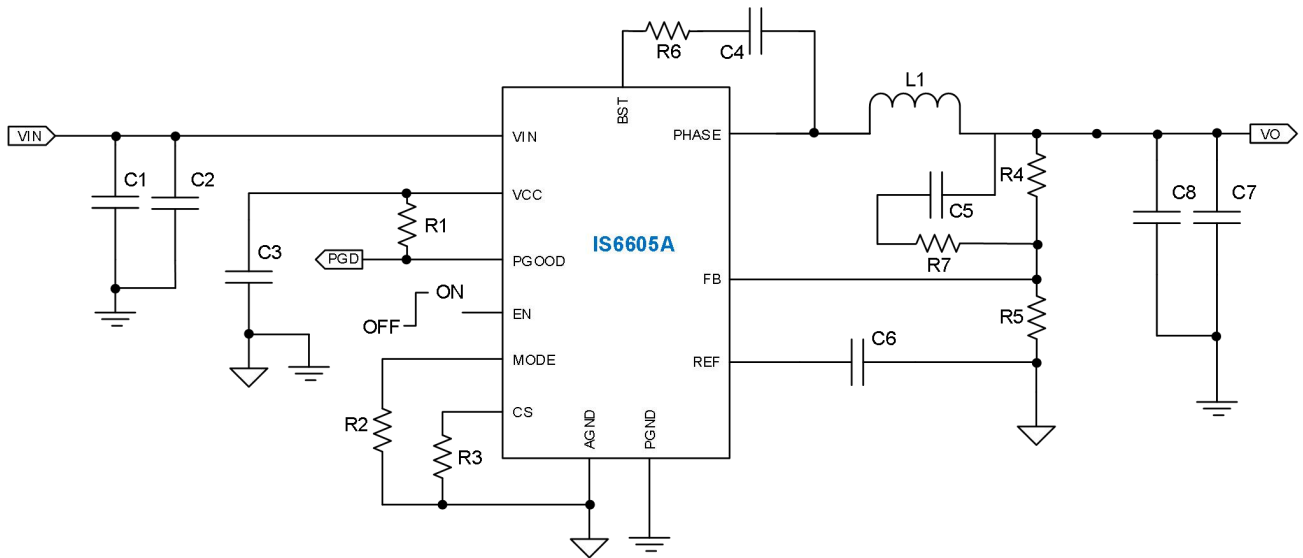
Order Information TOP MARKING (IS6605A)

Part Number	Package	Shipping Method	Package Marking
IS6605A	QFN-14(2mm x 3mm)	5000u Tape & Reel	6605A

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● 
  6605A

  8A653

  YYWW
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6605A: First five digits of the part number
8A653: Lot ID
YY: Year code
W:W Week code

Package Reference

Top View

Absolute Maximum Ratings

Supply Voltage (V_{in})………………….....-0.3V to 18V
V_{cc} Voltage (V_{cc})……………………….-0.3V to 5.5V
Switch Node Voltage (V_{PH}) DC……….-0.3V to 18.3V
Switch Node Voltage (V_{PH}) 25ns ……….-5V to 20V
BST Pin (V_{bst-sw}) 25ns…………………..-0.3V to 5.5V
All other pins……………………….....-0.3V to 5.5V
Junction Temperature (T_j)……………………150°C
Storage Temperature…………………-65°C to 150°C

Recommended Operating Conditions

Supply Voltage (V_{in})……………………2.7V to 16V
V_{cc} Voltage (V_{cc})……………………3.15V to 3.6V
Output Voltage (V_o)……………………0.6V to 5.5V
Max Output Current (I_{o_max})…………………………6A
Junction Temperature (T_j)……………-40°C to 125°C

Thermal Ratings

Θ_{JC} Max…………………………………………17.5°C/W
Θ_{JB} Typ (Still Air, No Heatsink)……………7°C/W

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

| Electrostatic Discharge	Standard	Value
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	1500V
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101F	2000V

1). JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2). JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Pin Out and Package

IS6605A(QFN-14)

Pin Number	Name	Description
1,14	PGND	System Ground. Power ground of the power stage.
2,11	PHASE	Switch Output. Switch node of power stage.
3	VIN	Supply voltage. Input to the power stage and internal LDO.
4	CS	Current limit and inductor current report. Connect a resistor to AGND to set the valley current limit trip point. A voltage indicating the inductor current during operating.
5	EN	Enable pin. An input signal turns the regulator on or off. Connect EN to VIN through a pull-up resistor. Do not float this pin.
6	FB	An external resistor divider from output to AGND is tapped to FB to set the output voltage. It is recommended to place the resistor divider as close as possible to FB. Avoid vias on FB traces.
7	AGND	Signal logic ground. A Kelvin connection to PGND is required.
8	REF	External tracking voltage input. The output voltage tracks this input signal. REF is decoupled as close as possible to the ceramic capacitor
9	PGOOD	Power good output with open drain. If the output voltage is within the regulation range, a pull-up resistor connected to the DC voltage is required to indicate a logic high signal.
10	BST	Bootstrap connection. A capacitor connected between PHASE and BST is required to form a floating supply across the high-side switch driver.
12	MODE	Operation mode selection. Connect a resistor to AGND to set switching frequency and select PLUSE SKIP/FCCM Mode.
13	VCC	Internal 3.3V LDO output. The driver and control circuit are powered by VCC. Decouple VCC with a minimum 1uF ceramic capacitor as close as possible.

FUNCTIONAL BLOCK DIAGRAM
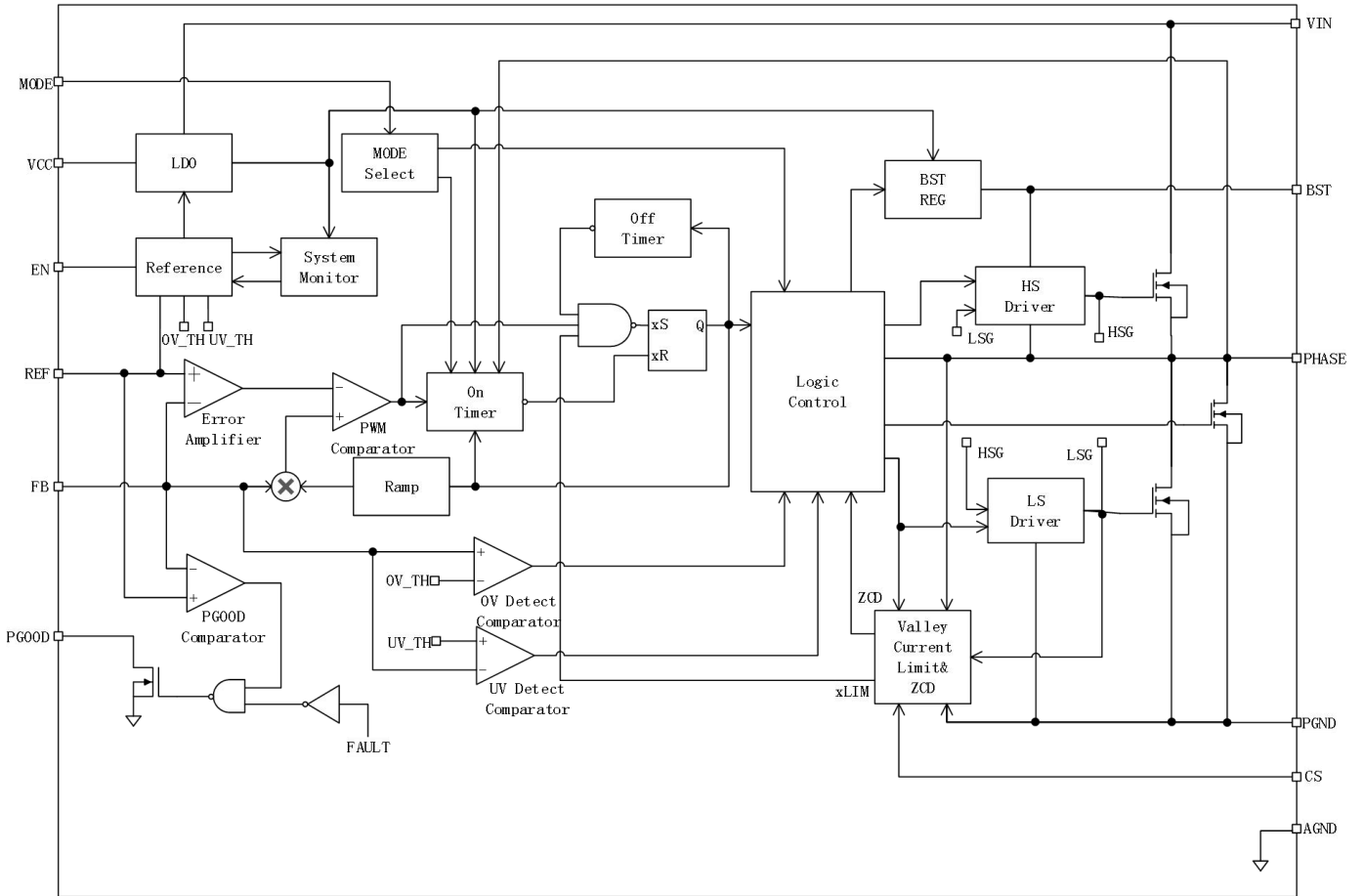
ELECTRICAL CHARACTERISTICS

Vin = 12V, $T_j = -40°C$ to $125°C$, unless otherwise noted.

Parameters		Definition/Datasheet			Units
		Min	**Typ**	**Max**	
Supply Voltage & Current					
VIN Supply Voltage (with internal LDO)		4.0		16	V
VIN Supply Voltage (with external bias)		2.85		16	V
VIN Supply Current (Quiescent)	EN=2V, V_{FB} = 0.62V		1500		µA
VIN Shutdown Current	EN="Lo"		0	2	µA
VCC Supply					
VCC Output Voltage (6V<VIN<16V)		3.12	3.3	3.42	V
VCC Output Current limit		25			mA
Load Regulation	Ivcc=25mA			2.2	%
Duty Cycle and Frequency Control					
Switching Frequency (Vin=12V, Vo=1V)	Mode=GND, CCM		1100		kHz
	Mode=30.1K, CCM		2000		kHz
	Mode=60.4K, CCM		600		kHz
	Mode=VCC, DCM		1100		kHz
	Mode=243K, DCM		2000		kHz
	Mode=121K, DCM		600		kHz
	Mode=15K, DCM		1500		kHz
	Mode=7.5K, FCCM		1500		kHz
Minimum On-Time			40		ns
Minimum Off-Time			100		ns
On-time at DCM(for DCM/CCM HYS)			110		%
Discharge					
Soft Discharge Transistor Resistance			110		Ω
MOSFET					
HFET R_{ds_on} (3.3V VCC)			22.5		mΩ
LFET R_{ds_on} (3.3V VCC)			8.5		mΩ
Switch Leakage				10	µA
Soft Start & FB					
VOUT=0% to VOUT=95%	C_{REFIN}=1nF		1.4		ms
Soft Start Delay Time			400		us
FB Voltage	Tj=-40 to 125°C		600		mV
	Tj=-0 to 70°C		600		mV
REF Sourcing Current			12		µA
REF Sinking Current			6		µA

| Power Good					
PGOOD Lower Threshold (rising edge) VOUT< Target		89	92.5	95	%
PGOOD Lower Threshold (falling edge) VOUT< Target		77	80	83	%
PGOOD Lower Threshold (rising edge) VOUT > Target		113	116	119	%
PGOOD Low to High Delay			0.9		ms
PGOOD Low Sink Current Capability @ 10mA				0.4	V
PGOOD Leakage Current VPG=3.3V				2.66	µA
PGOOD Low-Level Output Voltage	VIN=0V, 10KΩ Pull up		0.8	1	V
Current Limit					
Vcs Limit Voltage			1.2		V
Ics to Iout Ratio			40		µA/A
LS Negative Current Limit			-9		A
OSM(Output Sinking Mode)					
OSM Threshold (rising edge) VOUT< Target			105		%
OSM Threshold (falling edge) VOUT< Target			102		%
OSM Negative Current Limit			-4.5		A
OVP & UVP					
Output Over voltage (OVP)	Trip Threshold	113	116	119	%
	LS OFF threshold		50		%
Output Under voltage (UVP)	Trip Threshold	77	80	83	%
UVLO					
VCC UVLO	VCC rising		3.1		V
	Hysteresis		0.3		V
VIN UVLO	VIN rising		2.7		V
	Hysteresis		0.6		V
Enable					
EN Threshold Voltage	EN rising	1.15	1.22	1.25	V
EN Threshold Hysteresis			0.2		V
EN Input Current	EN=2V		0		µA
Thermal Protection					
Over Temperature (OTP)	Shutdown Temperature		160		˚C
	Hysteresis		30		˚C

TYPICAL PERFORMANCE

V_{IN} =12 V, T_A= 25°C, V_{OUT}= 1.8 V, F_S = 1.1MHz , L=1uH unless otherwise noted.
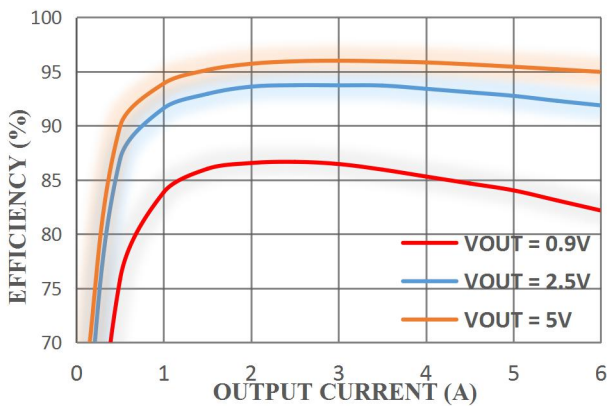
Efficiency
Pulse Skip, 1.0uH, VOUT=1.8V
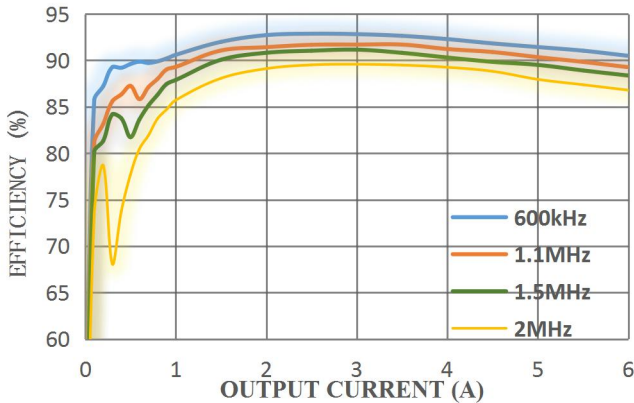
Efficiency
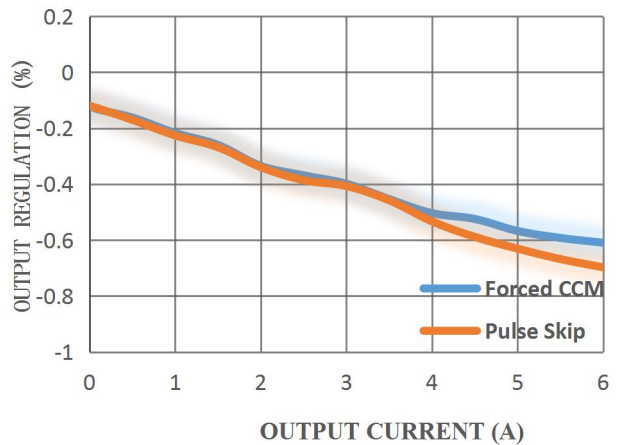Forced CCM, 1.0uH, VOUT=1.8V
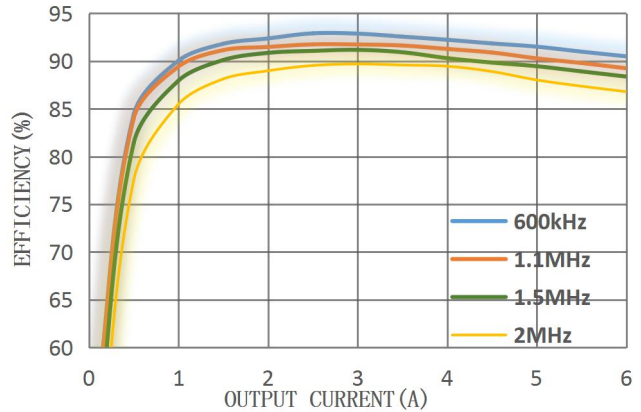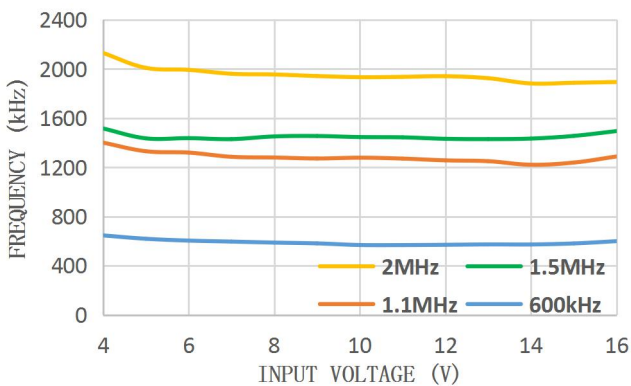
Efficiency
Forced CCM, 1.0uH, 1.1MHz
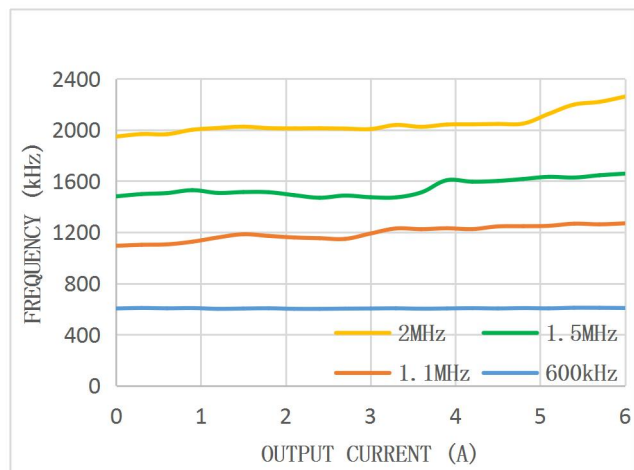
Load Regulation
Forced CCM,1.0uH, 1.1MHz

Switching Frequency vs Input Voltage
Forced CCM, 1uH, VOUT = 1.8V, Load = 2A

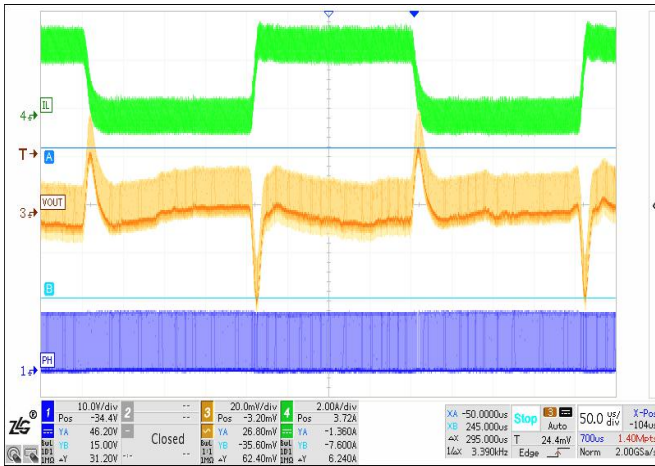### Switching Frequency vs Output Current
Pulse Skip,600kHz

TYPICAL PERFORMANCE
VIN=12V,VOUT=1.8V,L=1μH,TA=+25°C,unless otherwise noted.

Load Transient
Load=0A-3A，Forced Fccm
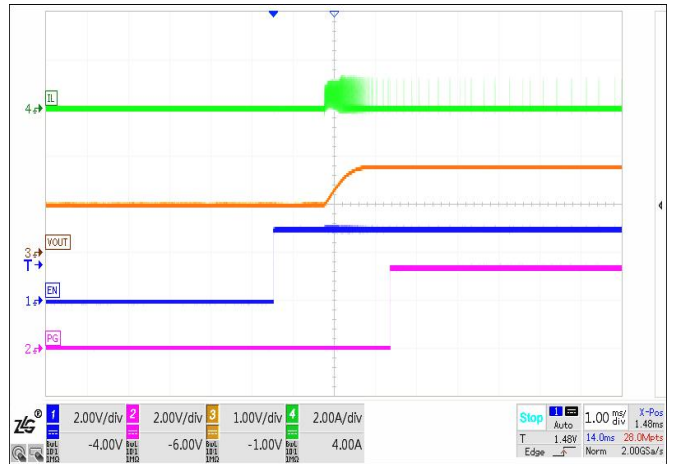

Load Transient
I_{OUT}=0-3A, Pulse Skip
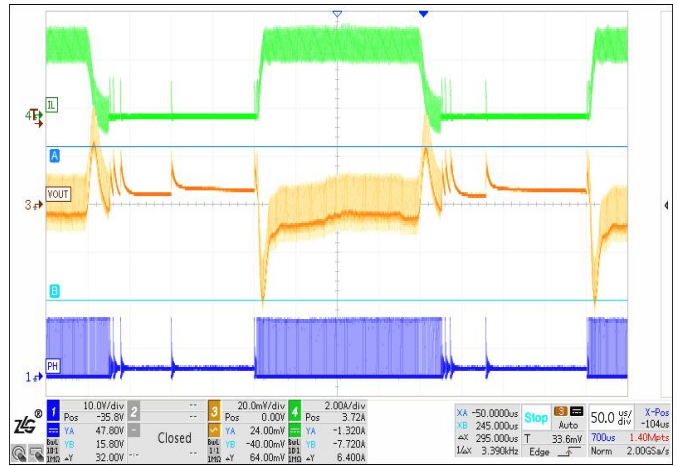
Pre-bias Start-Up
Forced CCM
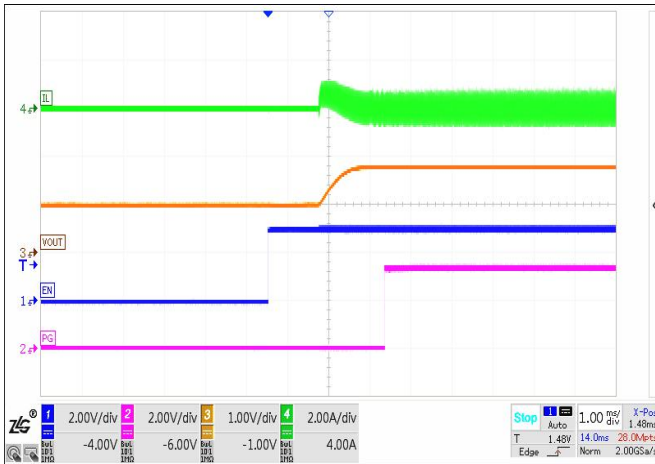
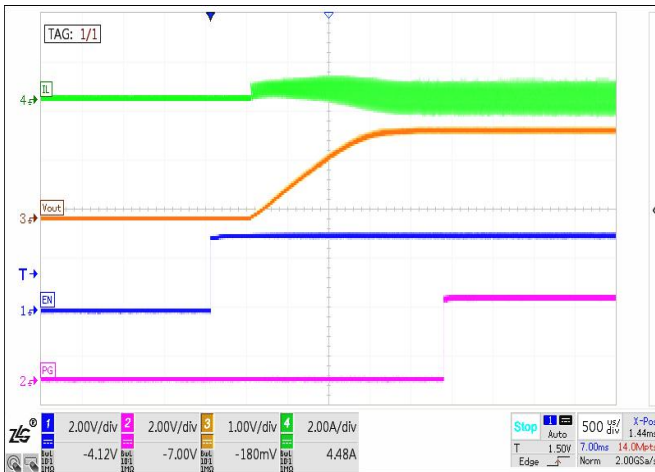**Pre-bias Start-Up**
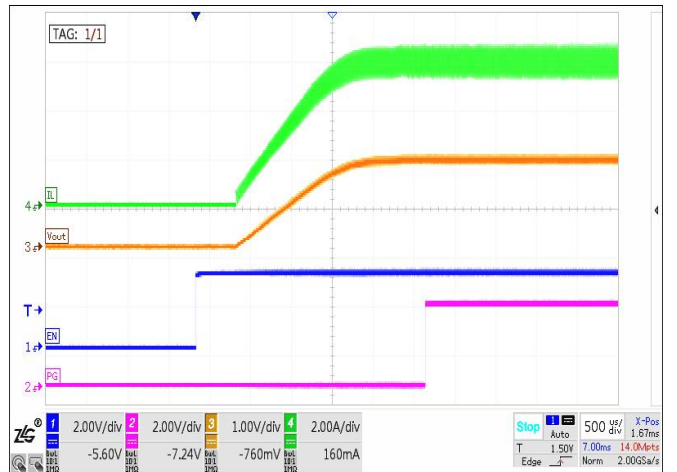Pulse Skip

Power Up through EN
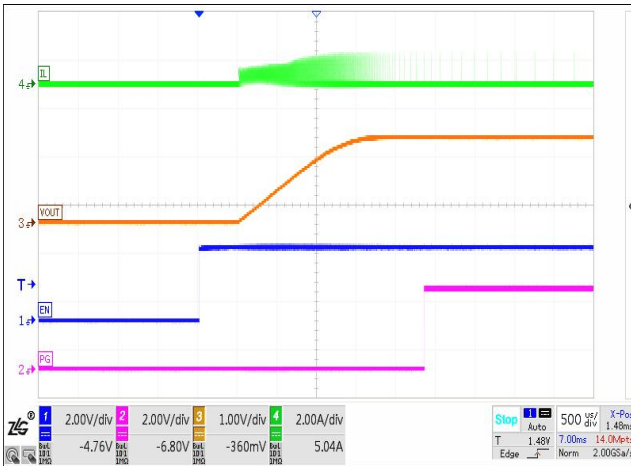I_{OUT}=0A, Forced CCM

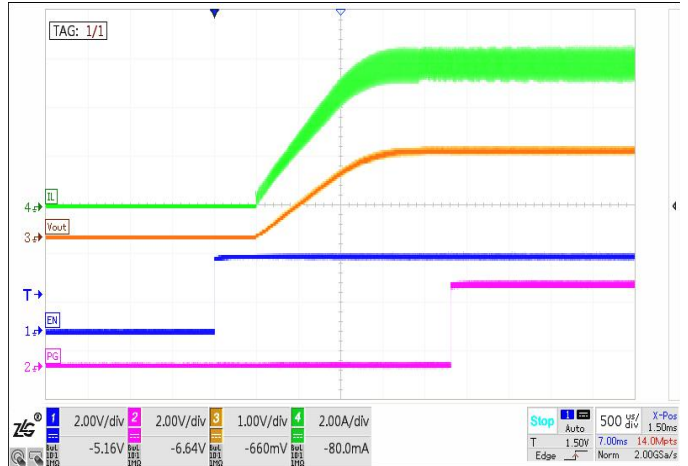**Power Up through EN**
I_{OUT}=6A, Forced CCM
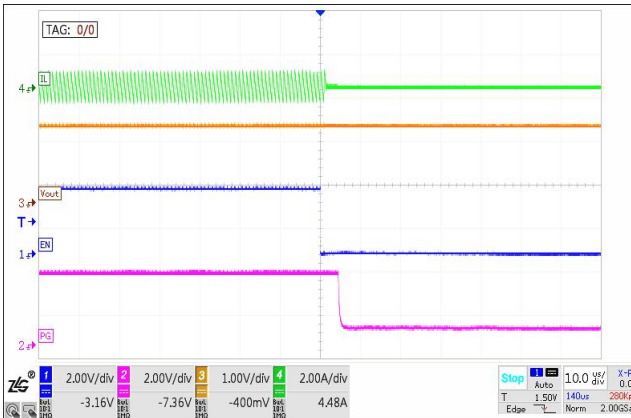
Power Up through EN
I_OUT=0A, Pulse Skip
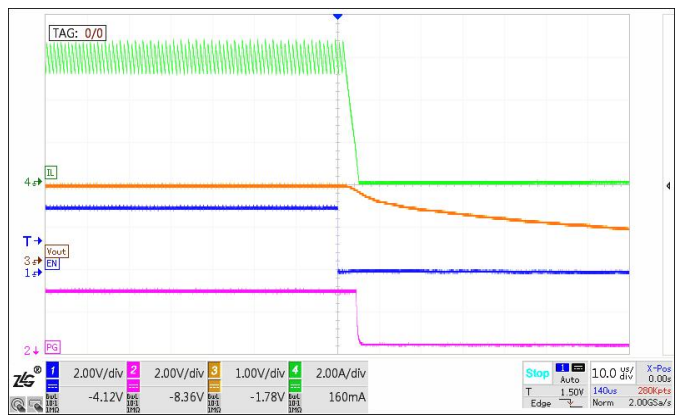

Power Up through EN
I_OUT=6A, Pulse Skip

Power Down through EN
I_OUT=0A, Forced CCM

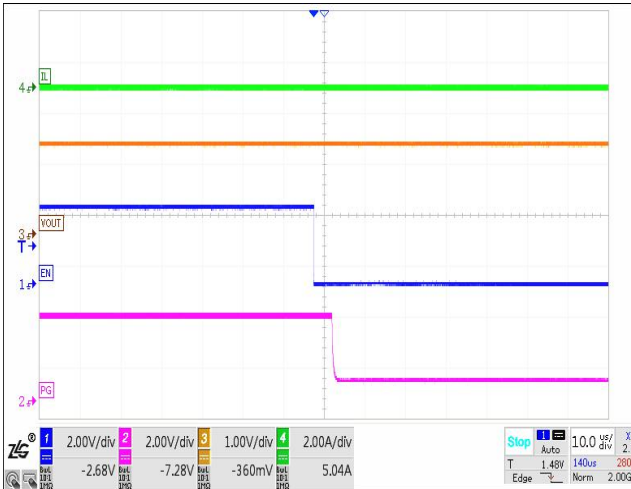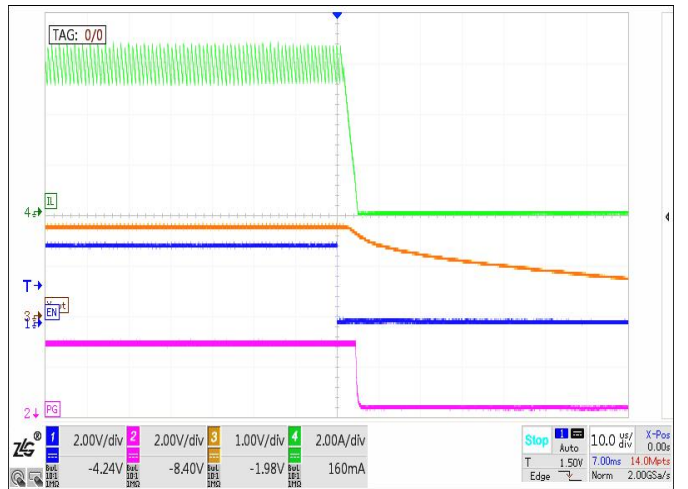## Power Down through EN
I_OUT=6A, Forced CCM
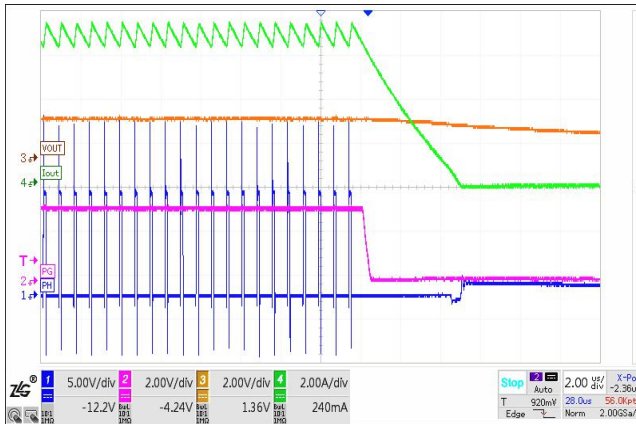

Power Down through EN
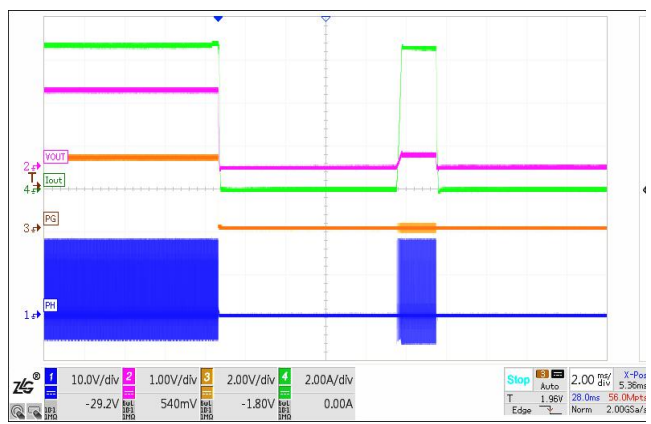I_OUT=0A, Pulse Skip

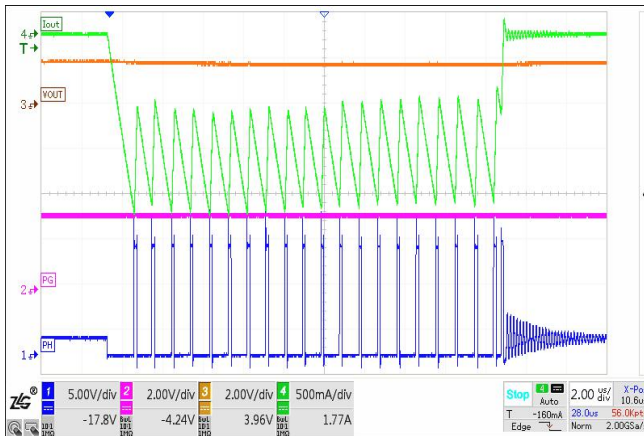## Power Down through EN
I_OUT=6A, Pulse Skip

Over-Current
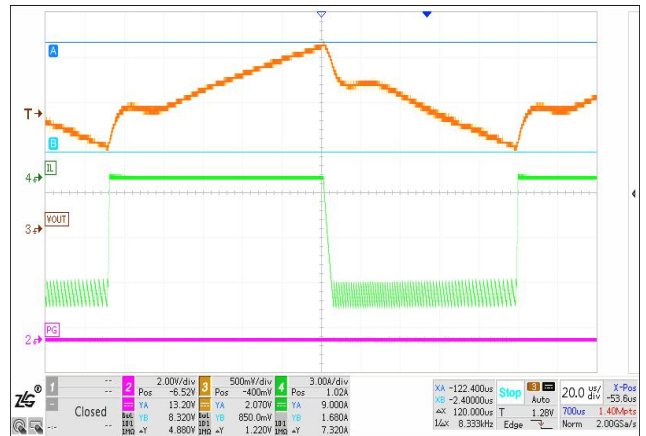Protection Entry

Hiccup
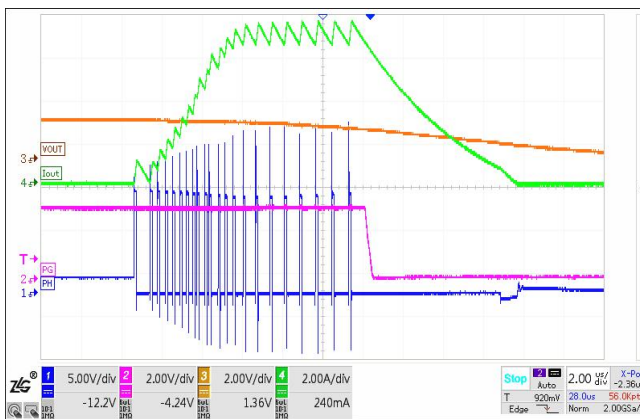Protection Recovery

OSM Operation
Forced CCM

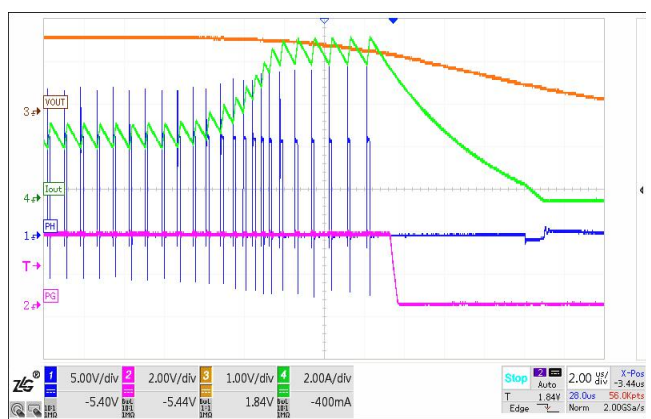## Over-voltage Protection
Pulse Skip Mode/ Forced CCM

VOUT short
Pulse Skip Mode

VOUT short
Forced CCM \ Start Load 3A

FUNCTIONAL INFORMATION

Product Overview

The IS6605A device is a high-efficiency, single channel, FET-integrated, synchronous buck converter. It is suitable for point-of-load applications with up to 6 A or lower output current in server, telecom, and similar digital applications. The device features proprietary Turbo Constant-On Time (TCOT™) (patent pending) to implement the transient algorithm with fast transient response. This patented architecture is built upon the adaptive constant on-time structure. The combination is ideal for building modern high/low duty ratio, ultra-fast load step response point of load DC-DC converters.

The IS6605A device has integrated MOSFETs rated at 6 A TDC.

The converter input voltage range is from 2.7 V up to 16 V. The output voltage ranges from 0.6 V to 5.5 V.

Stable operation with all ceramic output capacitors is supported, since the IS6605A uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require phase compensation network outside of the device which makes it easy to use and also enables low external component count. The designer may select the switching frequency from 3 preset values via resistor by MODE pin. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

FETs

The IS6605A device is a high-performance, integrated FET converter supporting current rating up to 6 A thermally. It integrates two N-channel FETs enabling high power density and small PCB layout area. The typical on-resistance, $R_{DS(on)}$, for the high-side MOSFET is 22.5 mΩ and typical on-resistance for the low-side MOSFET is 8.5 mΩ with a nominal gate voltage (V_{GS}) of 5 V.

Mode Selection

The IS6605A provides two modes of forced CCM operation and pulse skip under light load conditions. By switching the resistance of the resistor connected between MODE and RTN or VCC, 3 different switching frequencies and 2 light load modes can be achieved.

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	1100 kHz
243 kΩ (±20%) to GND	Pulse skip	2 MHz
121 kΩ (±20%) to GND	Pulse skip	600 kHz
GND	Forced CCM	1100 kHz
30.1 kΩ (±20%) to GND	Forced CCM	2 MHz
60.4 kΩ (±20%) to GND	Forced CCM	600 KHz

Soft Start (SS)

The IS6605A device uses soft-start time to control the inrush current required to charge the output capacitor bank during startup. The minimum SS time is designed to be 1 msec. The SS time can be extended by adding a capacitor between REF pin and RTN pin. The soft start time can be determined by the following equation:

$$T_{SS}(ms) = \frac{C_{REF}(nF) \times 0.6(V)}{36(\mu A)}$$

Over-Current Protection (OCP)

The IS6605A device performs both positive and negative inductor current limiting functions. The current sense is done by on-die sensing and is cycle by cycle. The positive current limit is used to protect the inductor from saturation that might cause damage to the high side and low side FETs. The negative current limit protects the low side FET during OVP discharge. For IS6605A, the negative current limit is fixed at 4.5 A where

the low side FET is turned off for 200 nsec to limit the current.

During the low side FET ON state, the inductor current is sensed at PHASE node and mirrored to CS pin at a ratio of Gcs. By connecting a resistor (Rcs) from CS pin to AGND pin, the current limit value can be established. Please refer to the following equation to calculate the positive current limit threshold.

$$I_{LIM}(A) = \frac{V_{OCP}}{R_{CS} \times G_{CS}} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}}$$

Where, V_{OCP} = 1.2 V,
G_{CS} = 40 µA / A,
I_{LIM} = required output current limit (A).

The OCP hiccup operation is valid 3msec after IS6605A is enabled. Once OCP hiccup is enabled, if the IS6605A detects over-current condition for 31 consecutive cycles, or the FB falls below the under-voltage protection (UVP) threshold, it enters HICCUP mode. In HICCUP mode, the IS6605A immediately latches off the high side FET and latches off the LS-FET after detecting the zero crossing. At the same time, the REF capacitor is also being discharged. After about 11 msec, the IS6605A will attempt an automatic re-startup. If the over-current condition still exists after 3msec operation, the IS6605A repeats this operation until the over-current condition disappears and the output voltage returns to the regulation level.

Feedback (FB)

FB and RTN pins are used for remote sensing purpose. Where feedback resistors are required for output voltage programming, the FB pin must be connected to the mid-point of the resistor divider, and the RTN pin must always be connected to the load return. FB and RTN pins are high-impedance input terminals of the differential remote sense amplifier. The feedback resistor divider should use resistor values much less than 100 kΩ. The output voltage of IS6605A can be adjusted by changing the resistor divider, R_{top} and R_{bot}. Calculate output voltage from R_{top} and R_{bot} using the formula below:

$$V_{OUT} = \frac{R_{top} + R_{bot}}{R_{bot}} \times 0.6V$$

Resistor Selection for Common Output Voltages is listed in the following table. The accuracy should be 1% or better to ensure voltage setpoint accuracy is satisfied.

$V_{OUT}(V)$	$R_{top}(k\Omega)$	$R_{bot}(k\Omega)$
1.0	2	3
1.2	4.02	4.02
1.8	4.02	2
3.3	8.2	1.8
5	8.2	1.1

Fault Protections

This section describes overvoltage protection, OSO limits, undervoltage protections and over temperature protections.

Undervoltage Protection and Overvoltage Protection

The IS6605A device monitors a feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 80% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 msec, the device latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 116% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off for 200 nsec before turning on again. The IS6605A device operates in this cycle until the output voltage is pulled down below 50% of the set point value. When OVP fault happens, PGOOD is latched off and will remain low until a reset of VCC or by re-toggling the EN pin.

Output Sinking Operation

The device has an output sinking operation (OSO) during overvoltage protection that protects the output load at a much lower overvoltage threshold of 4% above the target voltage. OSO protection does not trigger an overvoltage fault, so the device is not latched off

after an OSO event. OSO protection operates as an early no-fault overvoltage-protection mechanism. During the OSO operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. Once the negative current limit is reached, the low side FET is turned off for 200 nsec before turning on again. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs. The operation repeats itself until the FB voltage drops below 102% x setpoint value. The IS6605A exists OSO after 15 consecutive cycles of forced CCM.

Over Temperature Protection

The IS6605A device has overtemperature protection (OTP) by monitoring the die temperature. If the temperature exceeds the threshold value (default value 160°C), IS6605A device is shut off and discharges REF capacitor. When the temperature falls about 30°C below the threshold value, the device turns on with a soft start sequence. The OTP is a non-latch protection.

POWER GOOD (PGOOD)

The IS6605A device has a power-good output that registers high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within ±7.5% of the target value, internal comparators detect power-good state and the power good signal becomes high after an 0.8 msec delay. If the output voltage falls below 80% of the target value, exceeds 116% of the target value, the power good signal latches off low. The open-drain power-good output must be pulled up externally to VCC or another voltage source of less than 3.6 V via a pull up resistor (10 kohm is recommended). The internal N-channel MOSFET does not pull down until the input voltage is applied. Once power-good is latched off, it can only be pulled high after a new soft-start sequence and output voltage is within the power-good window.

Application Implementation

The IS6605A device is a highly-integrated synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 6 A. Use the following design procedure to select key component values for this family of devices.

Design Input:

Vin = 12 V

Vin_max = 13.2 V, Vin_min = 10.8 V

Vout = 1 V +/- 5% (1% DC, 1% ripple, 3% transient)

Design Requirements:

$Iout_{max}$ = 6 A

Iocl = 8A

Load Step ΔI_{LOAD} = 60% x Imax

di/dt = 10 A/μsec

Fsw = 600 kHz

Tss = 1 msec

Forced CCM Operation

Design Procedure:

1. Switching Frequency Selection

Select a switching frequency for the regulator. There is a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 600 kHz achieves both a small solution size and a high-efficiency operation with the frequency selected.

Select one of 3 switching frequencies from the MODE table below. In addition to serving the frequency select purpose, the MODE pin can also be used to program light-load conduction mode. For IS6605A, there are two light load operations to choose. One is Pulse Skip mode and the other is Continue Conduction mode.

2. Inductor Selection

To calculate the value of the output inductor, use the following equation.

$$Lout = \frac{Vout}{(Vin_{max} \times fsw)} \times \frac{Vin_{max} - Vout}{Iout_{max} \times Kind}$$

The coefficient K_{ind} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, maintain a K_{ind} coefficient between 0 and 0.50 for balanced performance. Using this target ripple current, the required inductor size can be calculated using the equation provided above.

Selecting a K_{ind} of 0.25, the target inductance L_{out} = 1 μH. Using the standard value, the 1 μH is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using the following 3 equations. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{Vout}{(Vin_{max} \times fsw)} \times \frac{Vin_{max} - Vout}{L_{OUT}}$$

$$IL_{RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{RIPPLE}^2}$$

$$IL_{PEAK} = I_{OUT} + \frac{1}{2} \times I_{RIPPLE}$$

Choose an inductor that does not saturate under the maximum peak inductor current. Also, choose an inductor that gives the best thermal performance under the above calculated RMS current.

3. Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability

- Regulator response to a change in load current or load transient

- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

Minimum Output Capacitance to Ensure Stability

To prevent sub-harmonic multiple pulsing behavior, IS6605A application designs must strictly follow the small signal stability considerations describe in the following equation.

$$C_{OUT\_min} > \frac{t_{ON}}{2} \times \frac{8\tau}{L_{OUT}} \times \frac{V_{REF}}{V_{out}}$$

where

- $C_{OUT(min)}$ is the minimum output capacitance needed to meet the stability requirement of the design
- t_{ON} is the on-time information based on the switching frequency and duty cycle (in this design, 100 ns)
- τ is the ramp compensation time constant of the design based on the switching frequency and duty cycle (in this design, 1 μsec)
- L_{OUT} is the output inductance (in the design, 0.39 µH)
- V_{REF} is the reference voltage level (in this design, 0.6 V)
- V_{OUT} is the output voltage (1 V)

The stability is ensured when the amount of the output capacitance is greater than the minimum required value. And when all MLCCs (multi-layer ceramic capacitors) are used, both DC and AC derating effects must be considered to ensure that the minimum output capacitance requirement is met with sufficient margin.

For Constant on time topology, the minimum capacitance required by the stability is much smaller than that is required by the load transient.

Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

For normal applications with less than 10% duty cycle, the output voltage deviation during a dynamic load release determines how much output capacitance is needed.

Use the next equation to estimate the amount of capacitance needed for a given dynamic load release.

$$C_{OUT\_LoadRelease} = \frac{L_{OUT} \times \Delta I_{LOAD}^2}{2 \times \Delta V_{Load\_Release} \times V_{OUT}}$$

In general applications where the overall output voltage tolerance is +/-5%, the allowed transient voltage deviation during the worst case load release can be set at around 3% depending on how much output voltage setpoint accuracy (1% in this design) and the ripple voltage requirement (1% in this design). The minimum output capacitance to meet the overshoot requirement can be calculated using the above equation. This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.

- POSCAP bank #1: 1 x 330 µF, 2.5 V, 6 mΩ per capacitor

- MLCC bank #2: 1 × 10 µF, 2.5 V, 1 mΩ per capacitor with DC+AC derating factor of 50%

Recalculating the worst case overshoot using the described capacitor bank design, the overshoot needs to be 30 mV or less which meets the 3% overshoot transient specification requirement.

Output Voltage Ripple

The output voltage ripple is another important design consideration. The following equation calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement

when the impedance of the output capacitance is dominated by ESR.

$$Cout_{min\_Ripple} = \frac{I_{RIPPLE}}{8 \times F_{SW} \times V_{OUT\_RIPPLE}}$$

In this example, the maximum output voltage ripple is 9 mV. Because this capacitance value is significantly lower compared to that of transient load release, determining the output capacitance bank using the worst case load release requirement is generally adequate. Because the output capacitor bank consists of both POSCAP and MLCC type capacitors, it is important to consider the ripple effect at the switching frequency due to effective ESR.

For detailed calculations, please contact the factory to obtain a user-friendly Excel based design tool.

4. Input Capacitor Selection

The IS6605A devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 μF of effective capacitance on the VCC pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the VIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using the equation below.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into consideration. For this design example, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. For this design, allow 0.1 V input ripple for $V_{RIPPLE(cap)}$, and 0.3 V input ripple for $V_{RIPPLE(esr)}$. the minimum input capacitance for this design is 38.5 μF, and the maximum ESR is

9.4 mΩ. For this example, four 22 μF, 25 V low-ESR polymer capacitors in parallel were selected for the power stage.

Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 μF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

5. R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the IS6605A within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the PHASE area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this design twin 2.2 nF, 25 V, 0603 sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness. Its ideal placement is shown in PCB layout guidelines.

PCB Layout Guidelines

Efficient PCB layout is crucial to the stable operation of the circuit. For best performance, follow the PCB layout recommendations below.

1. The input MLCC capacitors shall be placed as close as possible to the VIN and PGND pins of IS6605A. The MLCC capacitor shall be placed on the same side as that of IS6605A. The copper plane of VIN and PGND shall be maximized to minimize the parasitic impedance.

3. Place as many PGND vias as possible nearest to the PGND pin to minimize parasitic impedance and thermal resistance.

4. VCC capacitor should be placed as close to the IS6605A as possible. Connecting AGND and PGND at VCC capacitor's grounding point is strongly recommended.

5. Place the BST capacitor as close as possible to BST and PH pins. Routing width should be greater than 20mil. It is recommended to use a 0.1 μF to 1 μF bootstrap capacitance value Place BST resistance between the IC and the BST capacitor to achieve damping effect by limiting the speed of the FET being turned on. It is recommended to use a 3.3 Ω resistor for bootstrapping purpose.

6. Place the REF capacitor close to AGND pin. It is recommended to use a 22 nF to 220 nF capacitor.
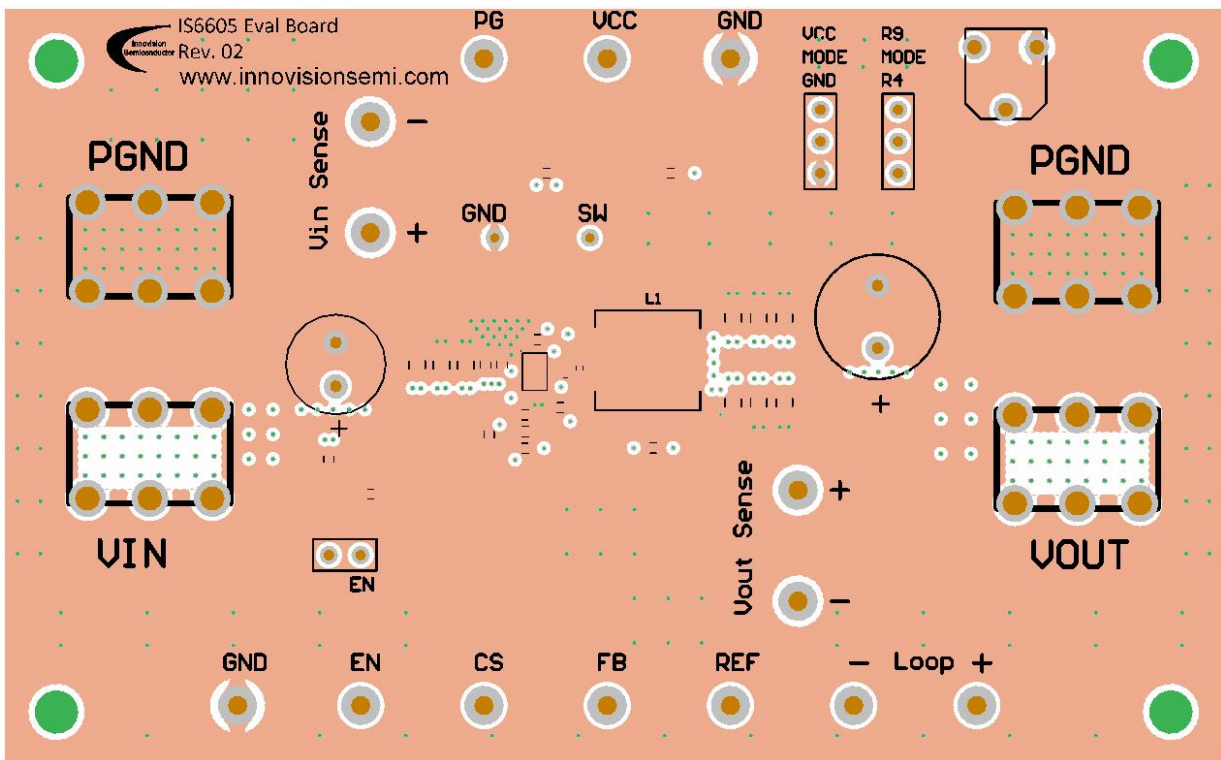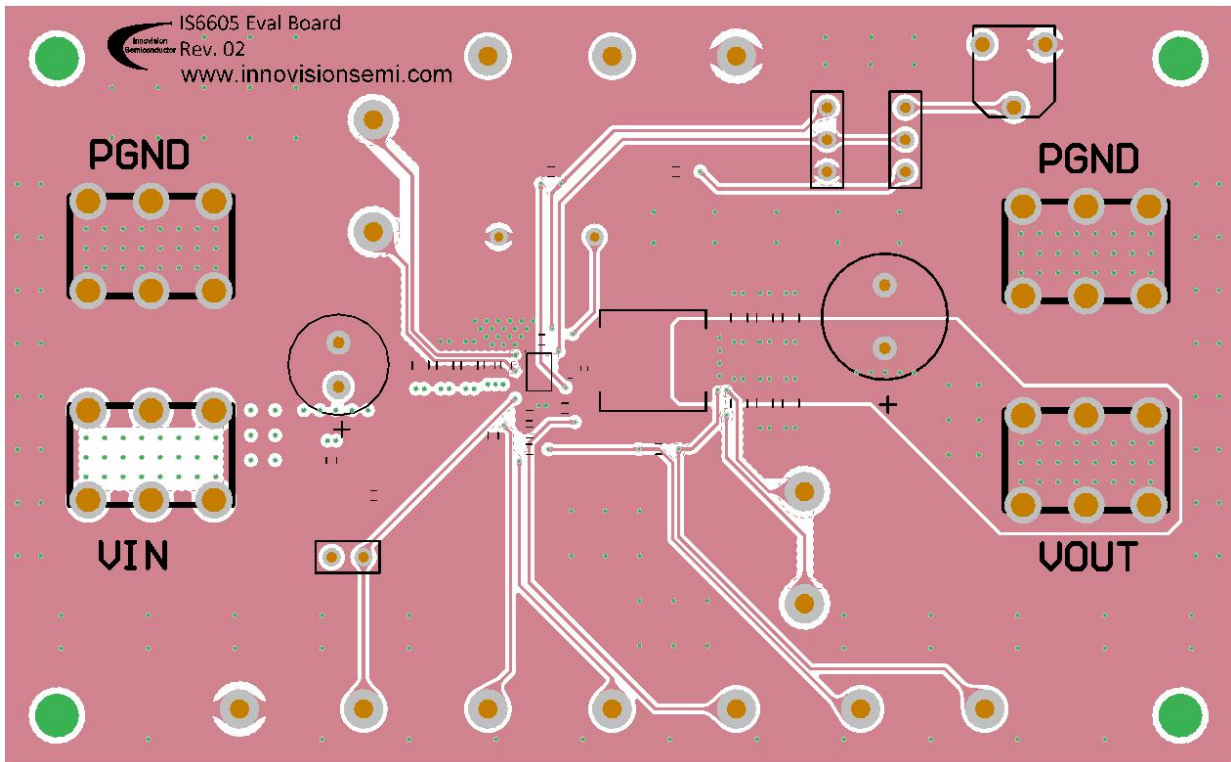
Typical Application Circuits
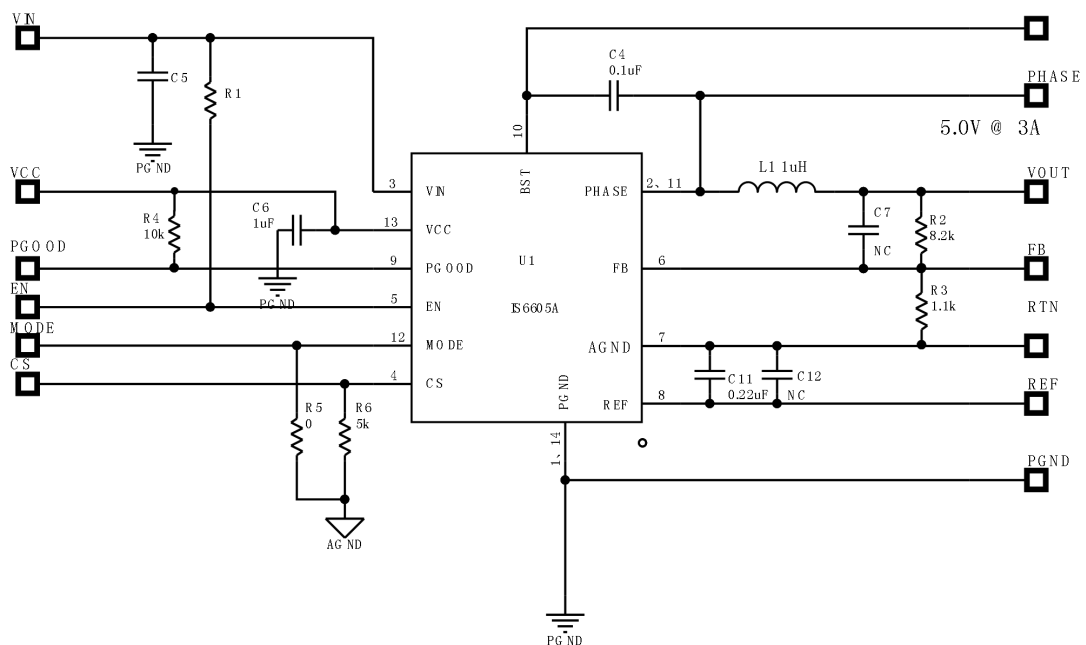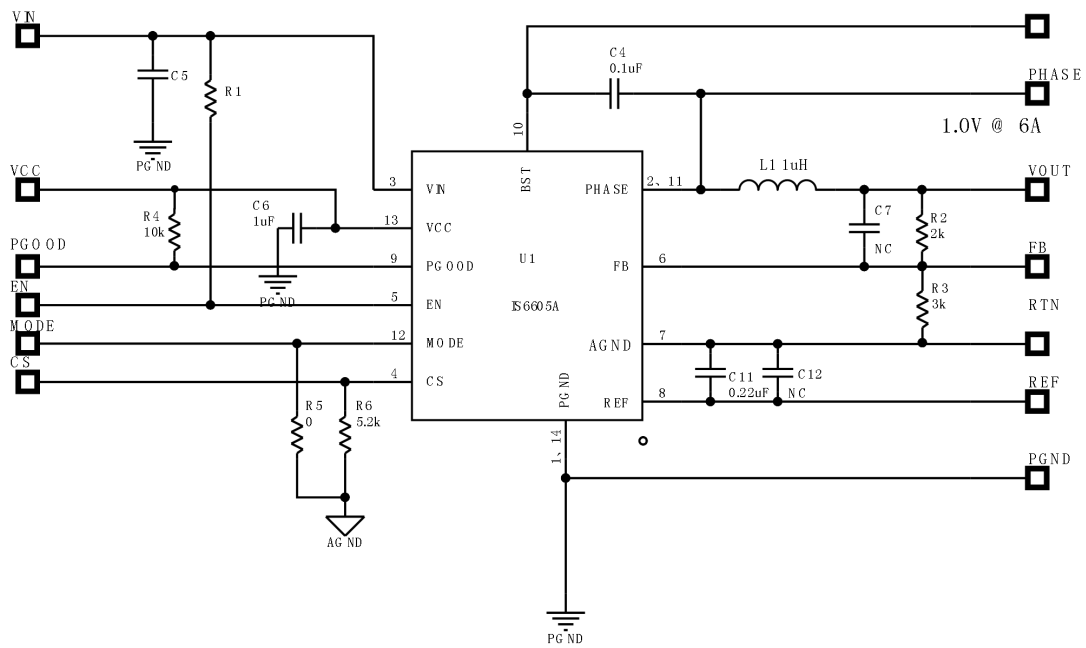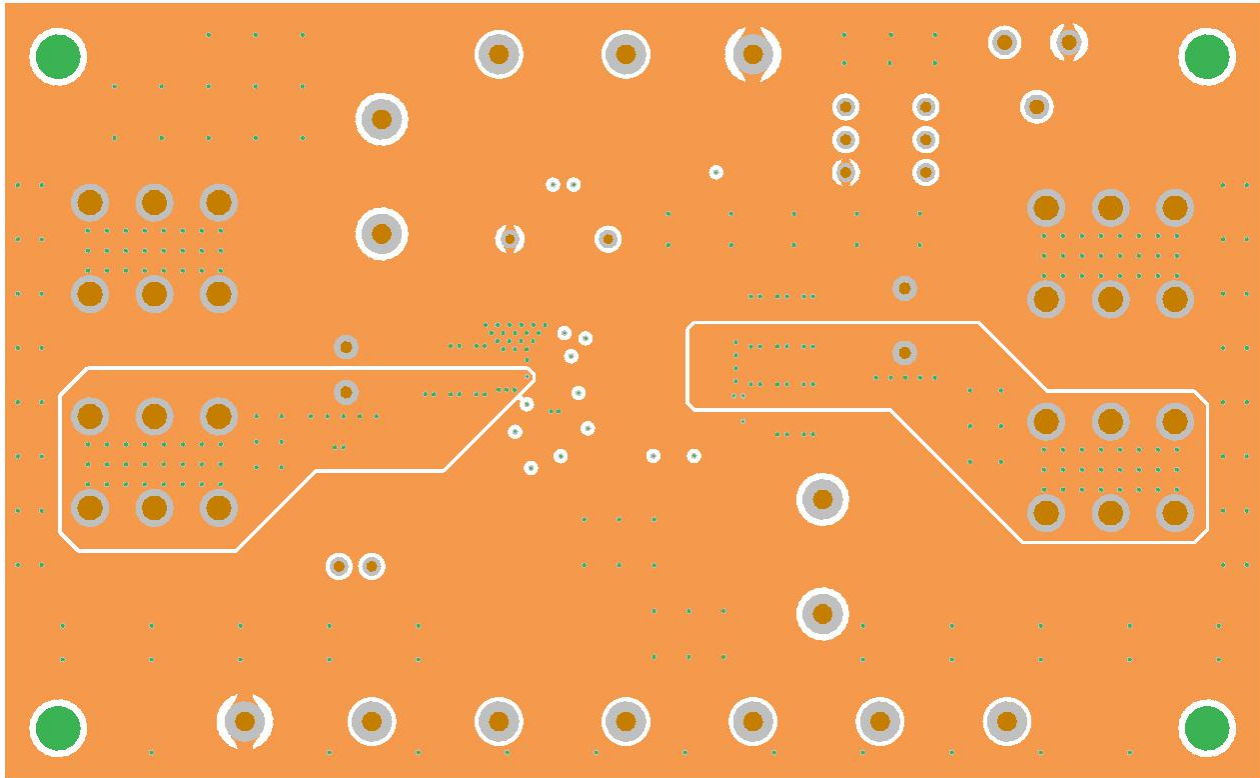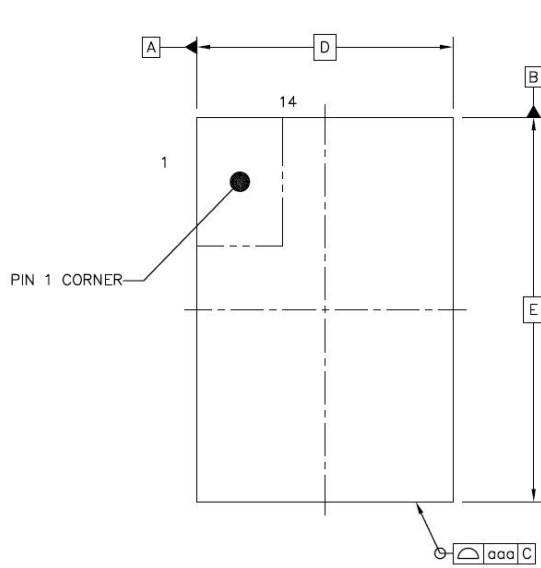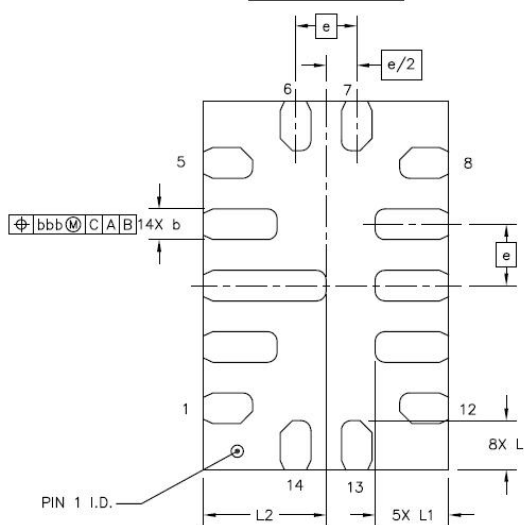
一、 PCB Layout

1) TOP Layer
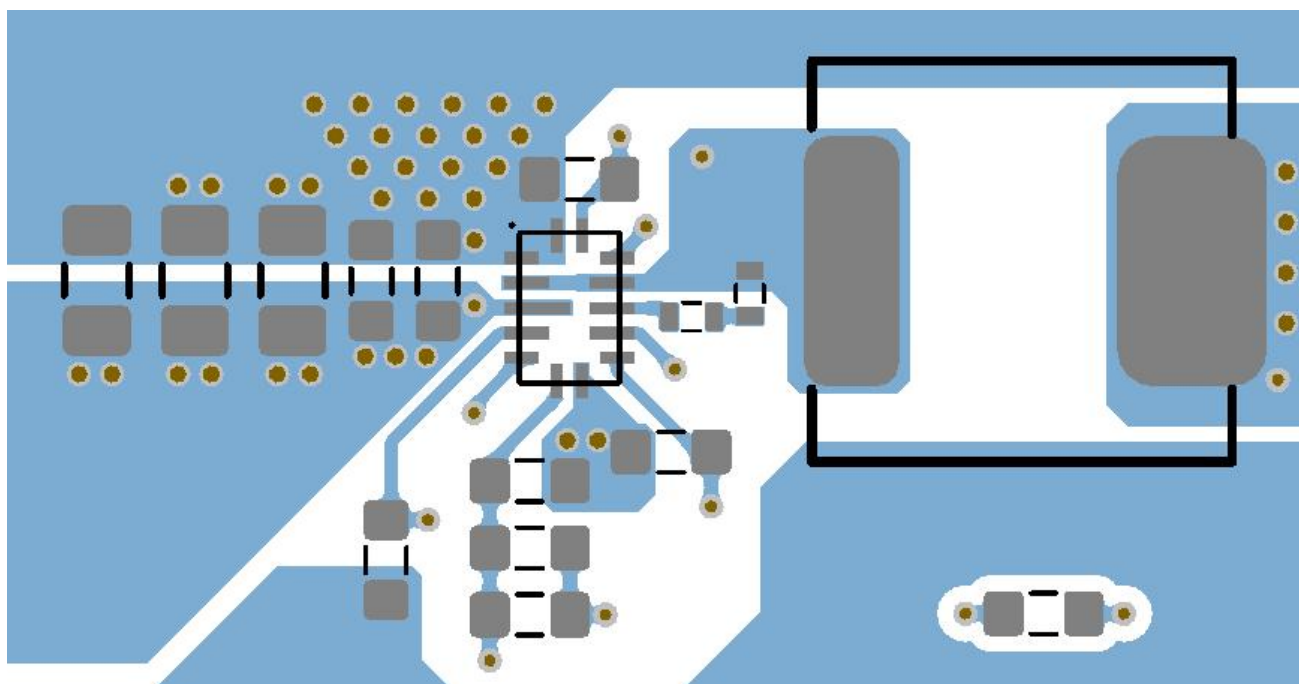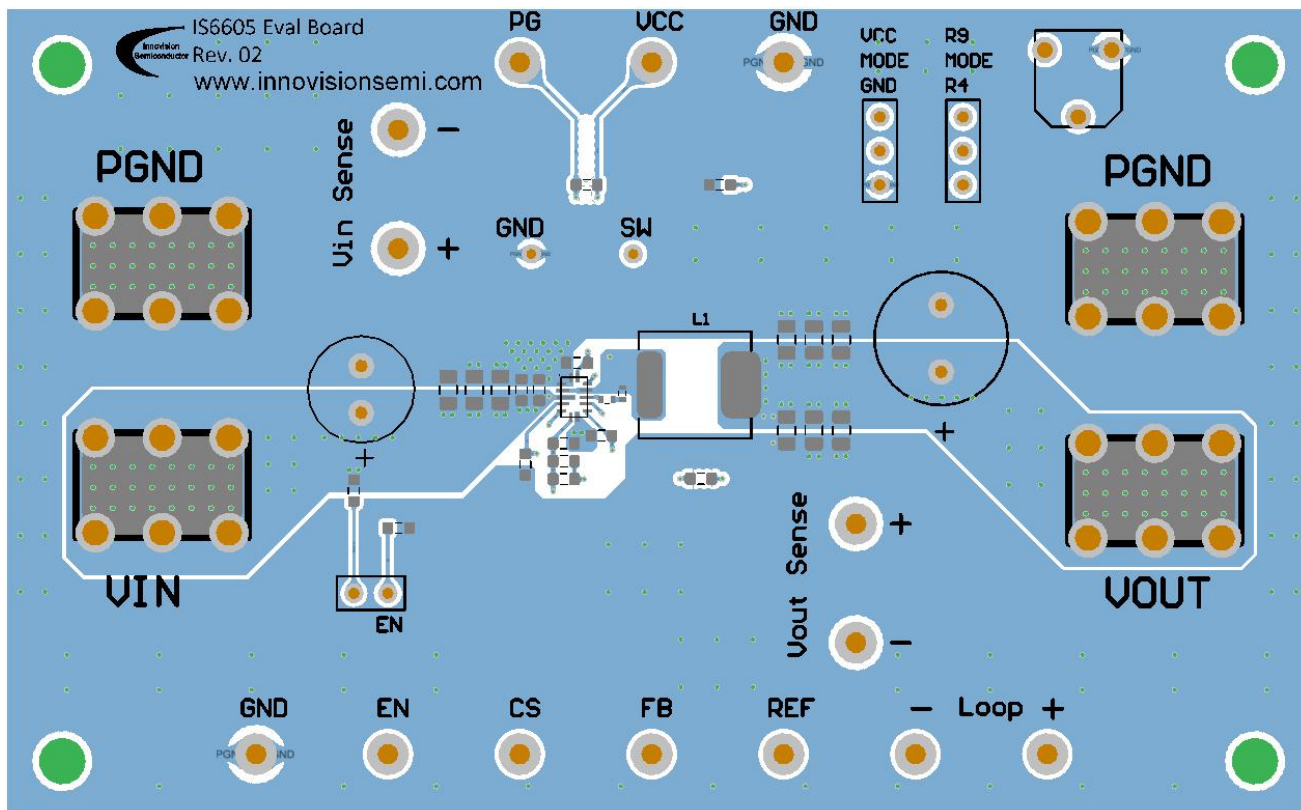
2) Layer 2

3) Layer 3

4)   Bottom Layer

Package Dimension

TOP VIEW
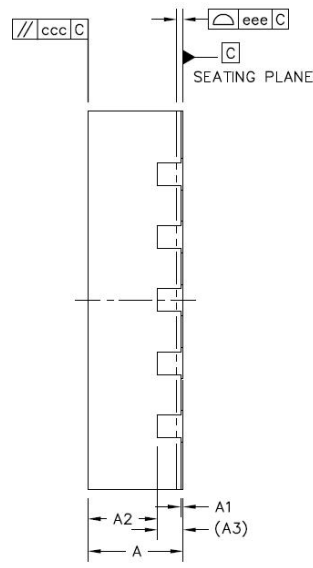
SIDE VIEW

BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		2 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.55	0.6	0.65
		L2	0.95	1	1.05
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	

Reflow Specification

Qualification Reflow: The IS6606 was qualified in accordance with IPC/JEDEC J-STD-020D.01. This standard classifies proper packaging, storage, and handling in order to avoid subsequent thermal and mechanical damage during the solder reflow attachment phase of PCB assembly.

The qualification preconditioning process specifies a sequence consisting of a bake cycle, moisture soak cycle (in a temperature humidity oven), and three consecutive solder reflow cycles, followed by functional device testing.
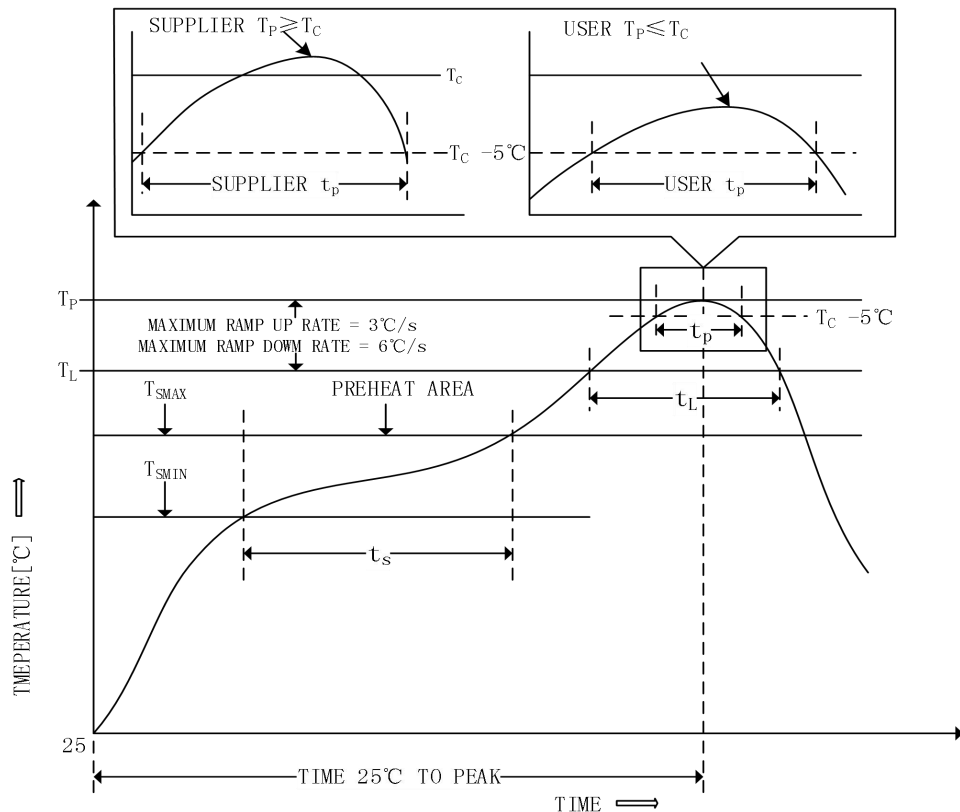
Production Reflow:

| PROFILE FEATURE	SN - PB EUTECTIC ASSEMBLY	PB-FREE ASSEMBLY
Peak package body temperature (TP)	For users, TP must not exceed T_C(235℃).For suppliers, TP must equal or exceed T_C(235℃).	For users, TP must not exceed T_C(260℃).For suppliers, TP must equal or exceed T_C(260℃).

Storage Specifications

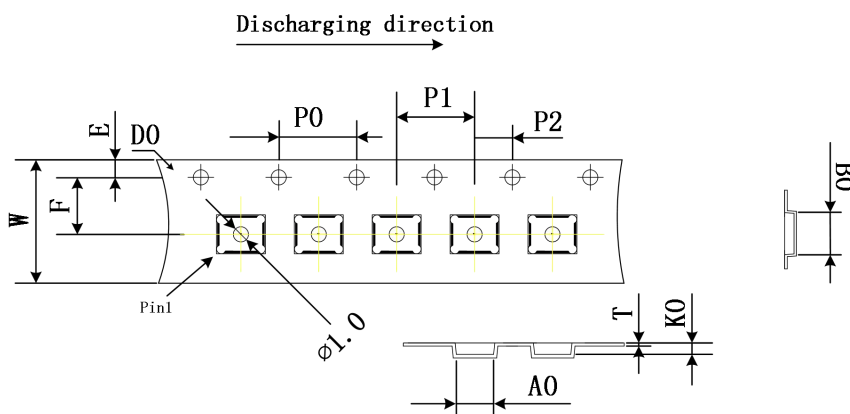The storage specification of the IS6606 conforms to IPC/JEDEC J-STD-020D.01 Moisture Sensitivity Level (MSL) 3.

After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60%RH

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Discharging direction

KEY PARAMETER LIST OF TAPE AND REEL
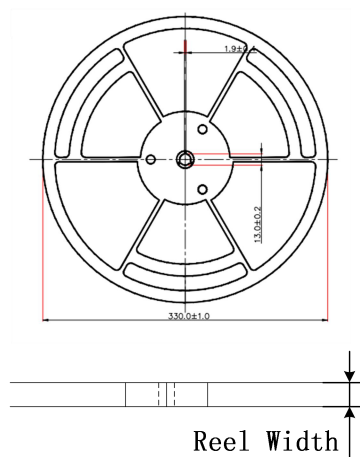
NOTE:

1、CARRIER TAPE COLOR:BLACK.

2、COVER TAPE WIDTH : 5.5±0.10.

3、COVER TAPE COLOR : TRANSPARENT.

4、10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20MAX.

5、CAMBER NOT TO EXCEED 1MM IN 100MM.

6、MOLD#2X3X0.75/0.85.

7、BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.

Package Type	Reel Diameter (inch)	Reel Width （mm）
QFN-14(2 x 3)	13″	$9.5^{+3.0}_{-1.0}$

Unit(mm)

ITEM	W	A0	B0	K0	P0	P1	P2	F	S	E	D0	T
DIM	8.00 +0.30 - 0.10	3.30 ±0.10	2.30 ±0.10	1.1 ±0.10	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	3.50 ±0.05	0.00 ±0.05	1.75 ±0.10	1.50 +0.10 - 0.00	0.20 ±0.02