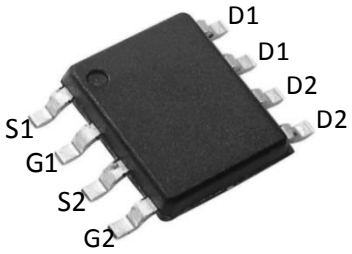
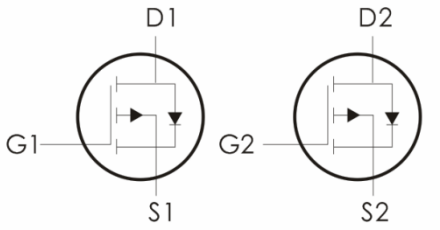
Description：

This Dual P-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.





Features：

1) V_{DS}=-30V,I_D=-5.1A,$R_{DS(ON)}$<55mΩ @V_{GS}=10V
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.

Absolute Maximum Ratings：(T_C=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current-[1]	-5.1	A
	Continuous Drain Current-TC=100℃	---	
	Pulsed Drain Current[2]	-20	
E_{AS}	Single Pulse Avalanche Energy[3]	---	mJ
P_D	Power Dissipation[4]	2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance,Junction to Case[1]	---	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient[1]	50	

Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=-0V,I_D=250μA	-30	-33	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=-24V	---	---	-1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	GATE-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	-1.	-1.6	-3	V
$R_{DS(ON)}$	Drain-Source On Resistance[2]	V_{GS}=-10V,I_D=-5.1A	---	43	55	mΩ
		V_{GS}=-4.5V,I_D=-4.2A	---	62	90	
G_{FS}	Forward Transconductance	$V_{DS=}$-15V, I_D=-4.5A	4	7	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V,V_{GS}=0V, f=1MHz	---	520	---	pF
C_{oss}	Output Capacitance		---	130	---	
C_{rss}	Reverse Transfer Capacitance		---	70	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, I_D=-1A, R_{GEN}=6Ω .V_{GS}=-10V	---	7	---	ns
t_r	Rise Time		---	13	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	14	---	ns
t_f	Fall Time		---	9	---	ns
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-5.1A	---	11	---	nC
Q_{gs}	Gate-Source Charge		---	2.2	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	3	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage[2]	V_{GS}=0V,I_S=-5.1A	---	---	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

Typical Characteristics: (T_C=25℃ unless otherwise noted)

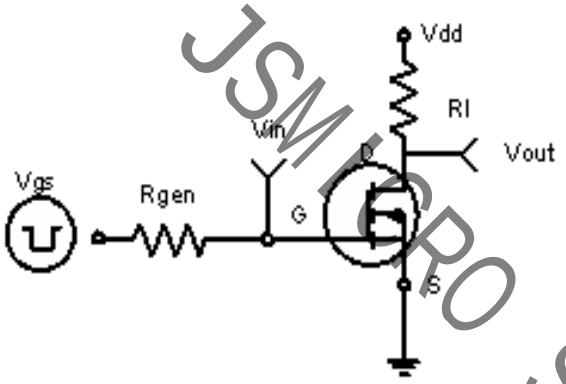


Figure 1:Switching Test Circuit

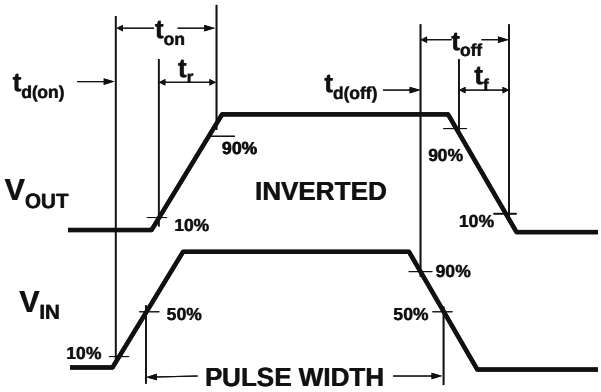


Figure 2:Switching Waveforms

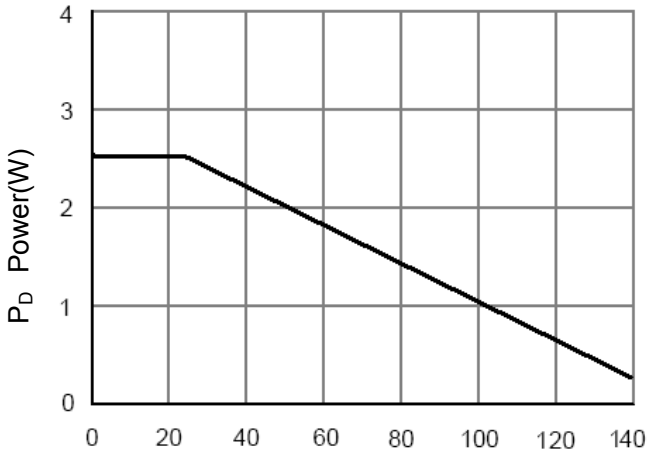


Figure 3 Power Dissipation

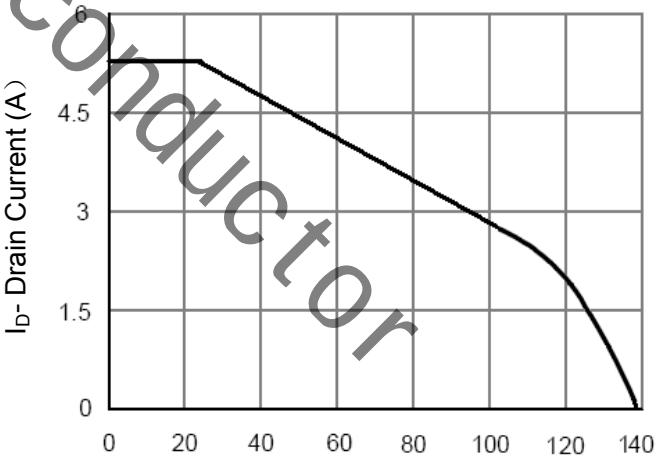


Figure 4 Drain Current

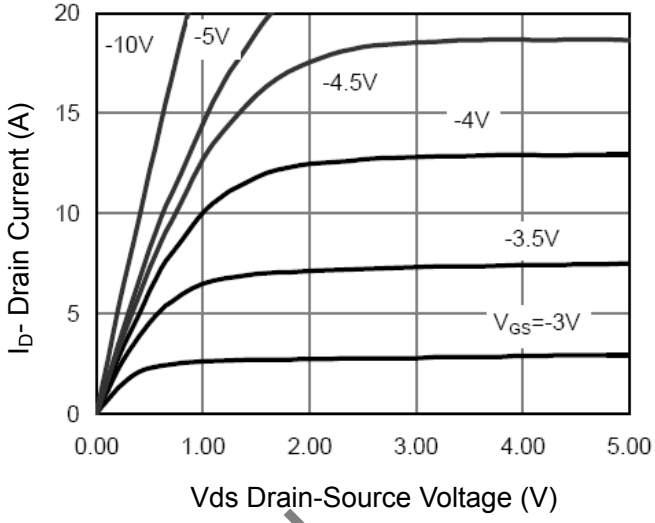


Figure 5 Output Characteristics

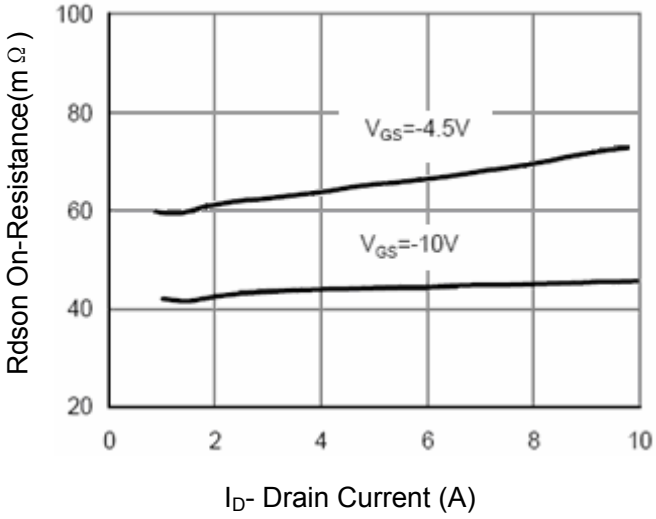


Figure 6 Drain-Source On-Resistance

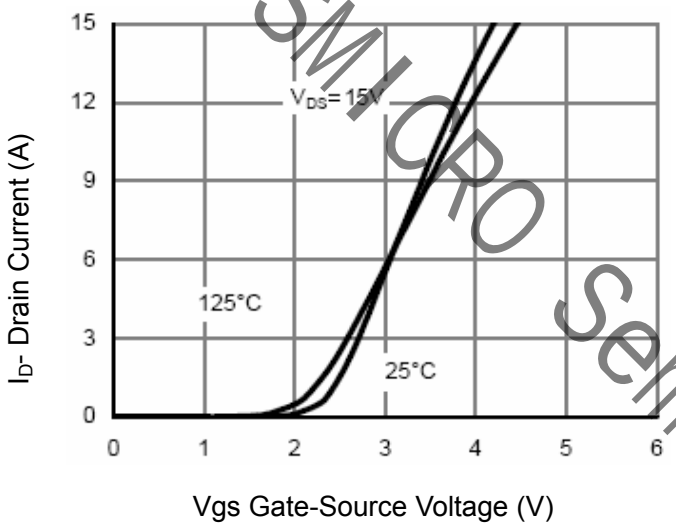


Figure 7 Transfer Characteristics

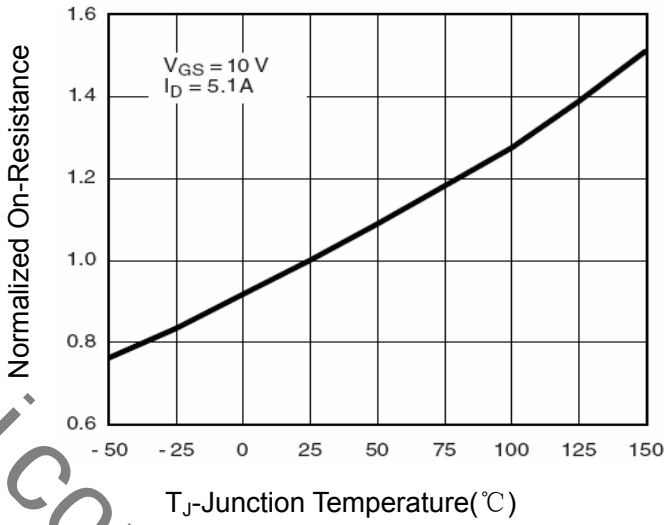


Figure 8 Drain-Source On-Resistance

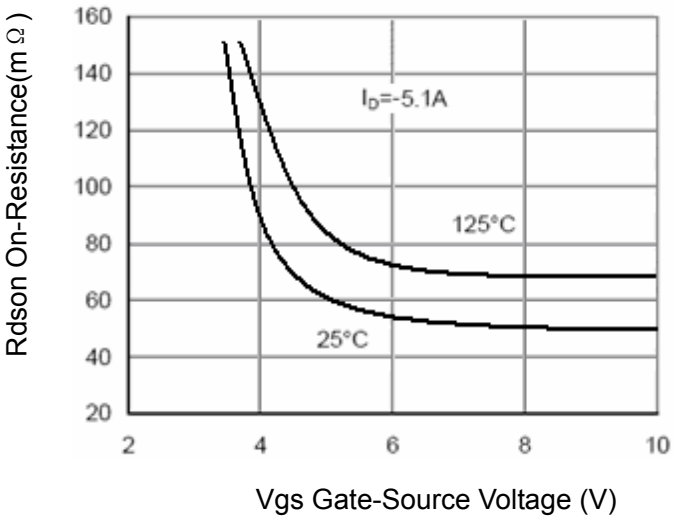


Figure 9 Rdson vs Vgs

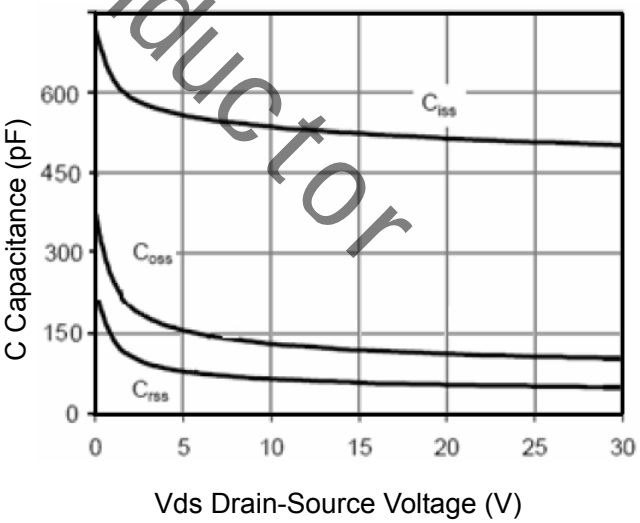


Figure 10 Capacitance vs Vds

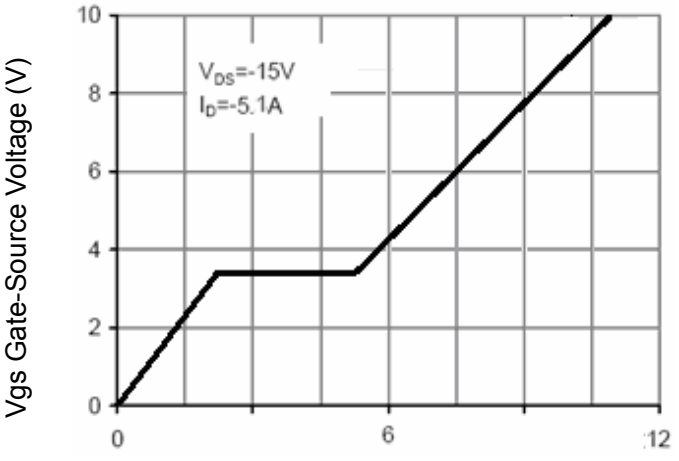


Figure 11 Gate Charge

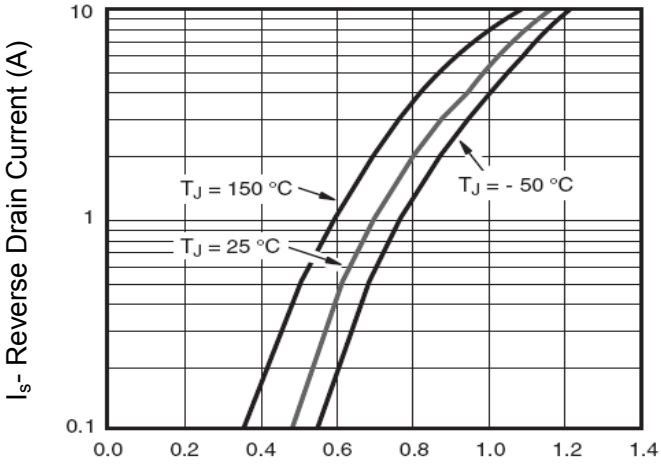


Figure 12 Source- Drain Diode Forward

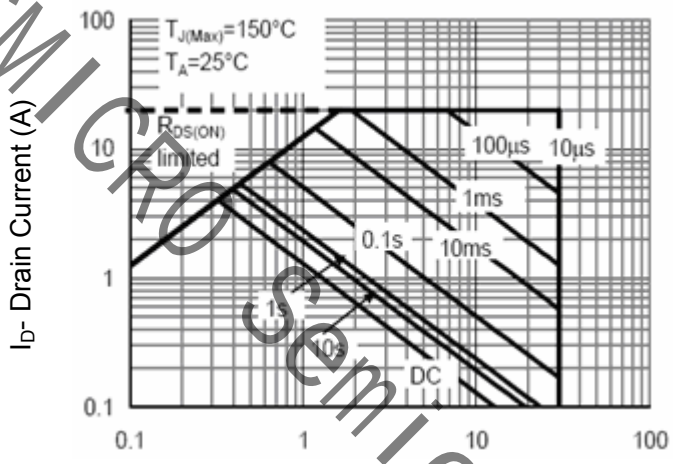


Figure 13 Safe Operation Area

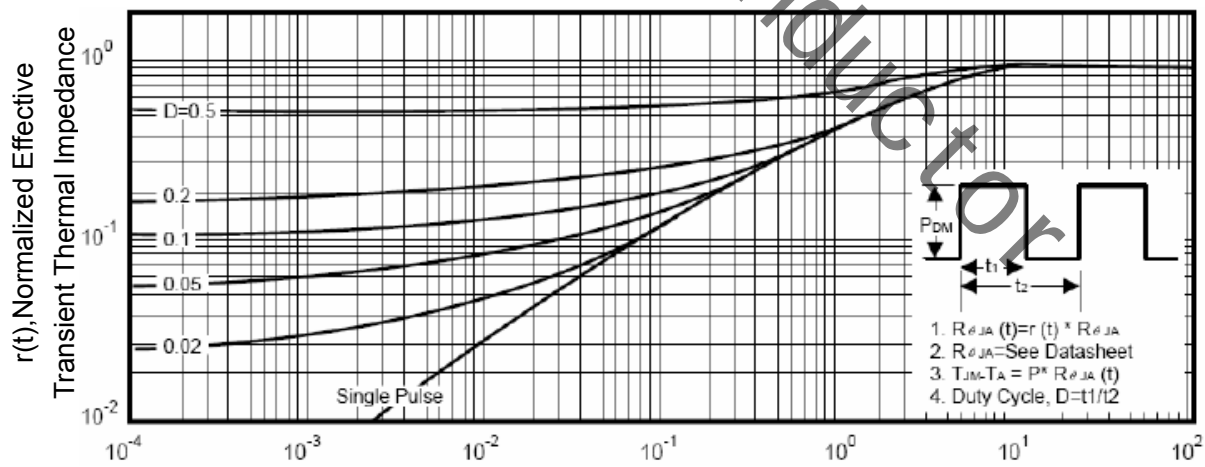
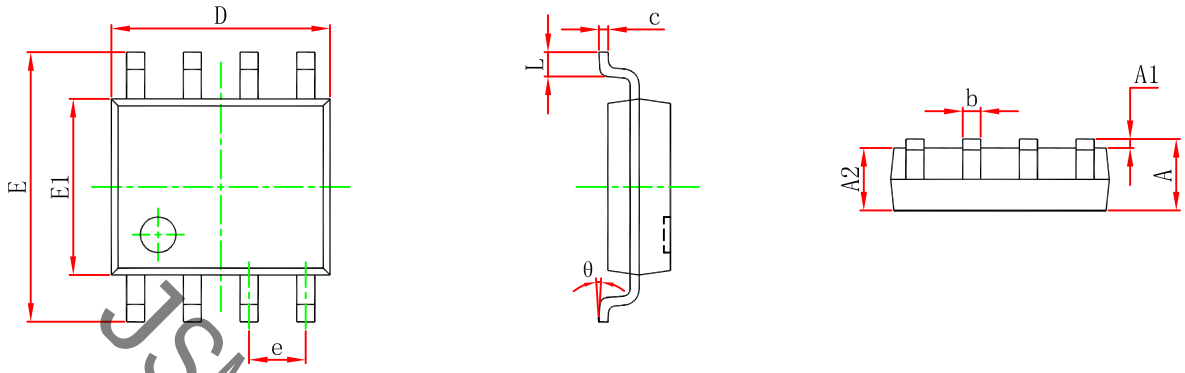


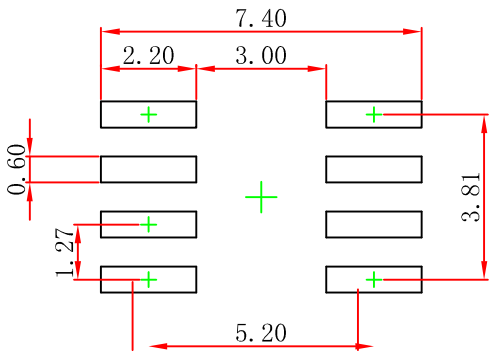
Figure 14 Normalized Maximum Transient Thermal Impedance

SOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.