

MMFTP84K

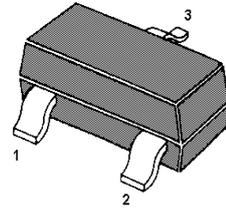
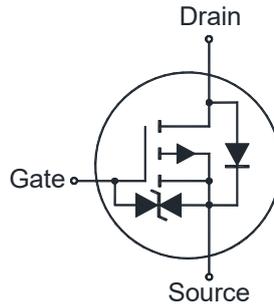
P-Channel Enhancement Mode MOSFET

Features

- ESD protection

Applications

- Portable appliances



1. Gate 2. Source 3. Drain
SOT-23 Plastic Package

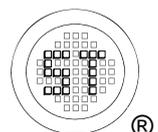
Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DS}$	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$-I_D$	180	mA
Peak Drain Current, Pulsed ¹⁾	$-I_{DM}$	700	mA
Power Dissipation ²⁾	P_D	225	mW
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	556 ²⁾ 265 ³⁾	$^\circ\text{C/W}$
Operating Junction Temperature Range	T_j	- 55 to + 150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to + 150	$^\circ\text{C}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{j(\text{MAX})} = 150^\circ\text{C}$.

²⁾ Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

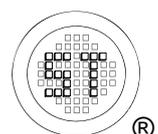
³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.



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Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $-I_D = 250 \mu\text{A}$	$-V_{(BR)DSS}$	60	-	-	V
Zero Gate Voltage Drain Current at $-V_{DS} = 25 \text{ V}$ at $-V_{DS} = 60 \text{ V}$	$-I_{DSS}$	-	-	0.1 1	μA
Gate-Source Leakage at $V_{GS} = \pm 20 \text{ V}$	I_{GSS}	-	-	± 10	μA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $-I_D = 250 \mu\text{A}$	$-V_{GS(th)}$	0.9	-	2	V
Drain-Source On-State Resistance at $-V_{GS} = 5 \text{ V}$, $-I_D = 0.1 \text{ A}$	$R_{DS(on)}$	-	2.6	10	Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $-V_{DS} = 25 \text{ V}$, $-I_D = 0.1 \text{ A}$, $f = 1 \text{ KHz}$	g_{fs}	50	-	-	mS
Input Capacitance at $V_{GS} = 0 \text{ V}$, $-V_{DS} = 30 \text{ V}$, $f = 1 \text{ MHz}$	C_{iss}	-	38	-	pF
Output Capacitance at $V_{GS} = 0 \text{ V}$, $-V_{DS} = 30 \text{ V}$, $f = 1 \text{ MHz}$	C_{oss}	-	9	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0 \text{ V}$, $-V_{DS} = 30 \text{ V}$, $f = 1 \text{ MHz}$	C_{rss}	-	6	-	pF
Total Gate Charge at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 4.5 \text{ V}$, $-I_D = 0.1 \text{ A}$	Q_g	-	1.1	-	nC
Gate Source Charge at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 4.5 \text{ V}$, $-I_D = 0.1 \text{ A}$	Q_{gs}	-	0.3	-	nC
Gate Drain Charge at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 4.5 \text{ V}$, $-I_D = 0.1 \text{ A}$	Q_{gd}	-	0.2	-	nC
Turn-On Rise Time at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 10 \text{ V}$, $-I_D = 0.1 \text{ A}$, $R_g = 6.8 \Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 10 \text{ V}$, $-I_D = 0.1 \text{ A}$, $R_g = 6.8 \Omega$	t_r	-	4	-	ns
Turn-Off Delay Time at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 10 \text{ V}$, $-I_D = 0.1 \text{ A}$, $R_g = 6.8 \Omega$	$t_{d(off)}$	-	15	-	ns
Turn-Off Fall Time at $-V_{DS} = 25 \text{ V}$, $-V_{GS} = 10 \text{ V}$, $-I_D = 0.1 \text{ A}$, $R_g = 6.8 \Omega$	t_f	-	77	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $-I_S = 0.5 \text{ A}$	$-V_{SD}$	-	-	1.2	V
Body Diode Reverse Recovery Time at $-I_F = 0.1 \text{ A}$, $di/dt = 100 \text{ A} / \mu\text{s}$	t_{rr}	-	60	-	ns
Body Diode Reverse Recovery Charge at $-I_F = 0.1 \text{ A}$, $di/dt = 100 \text{ A} / \mu\text{s}$	Q_{rr}	-	58	-	nC



Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

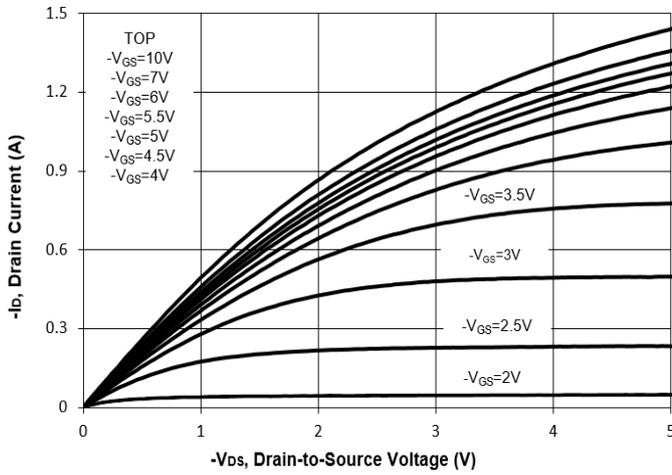


Fig. 2 Typical Transfer Characteristic

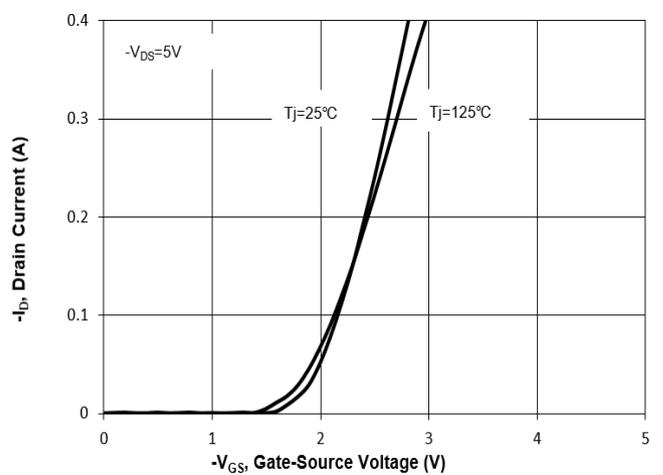


Fig. 3 on-Resistance vs. Gate Voltage

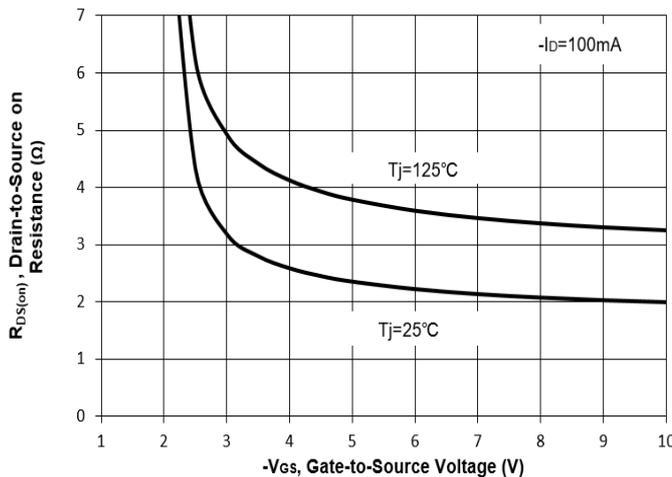


Fig. 4 on-Resistance vs. Tj

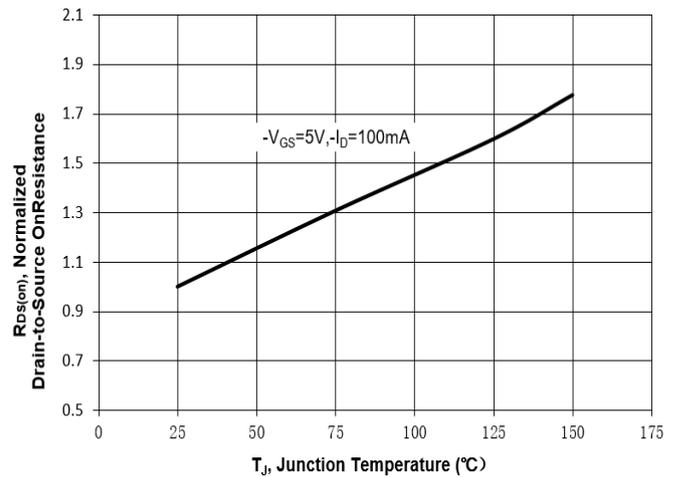


Fig. 5 On-Resistance vs. Drain Current

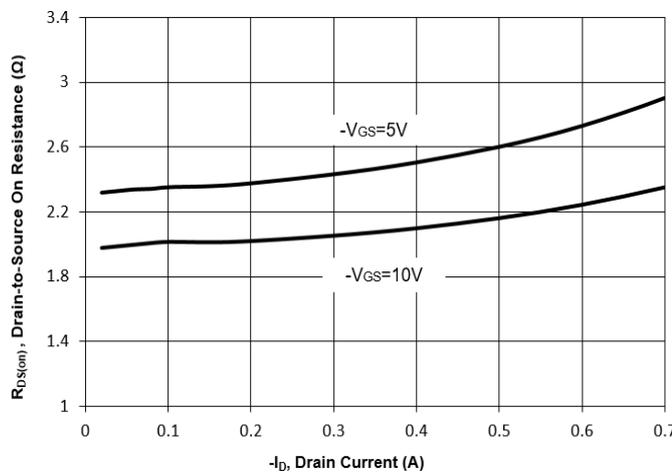
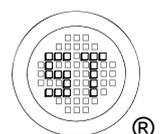
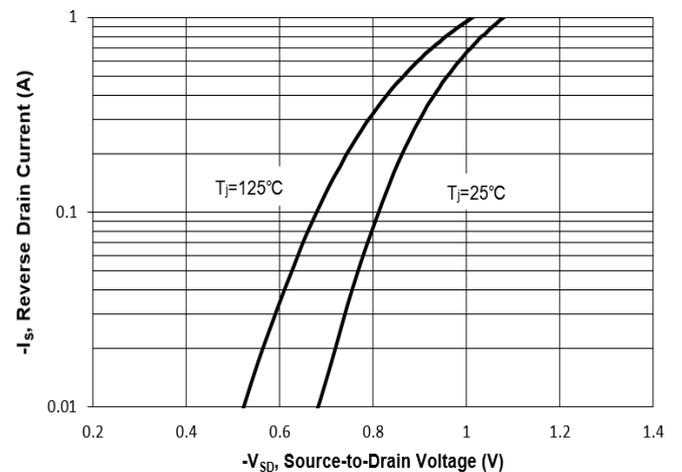


Fig. 6 Typical Forward Characteristic



Electrical Characteristics Curves

Fig. 7 $V_{(BR)DSS}$ vs. Junction Temperature

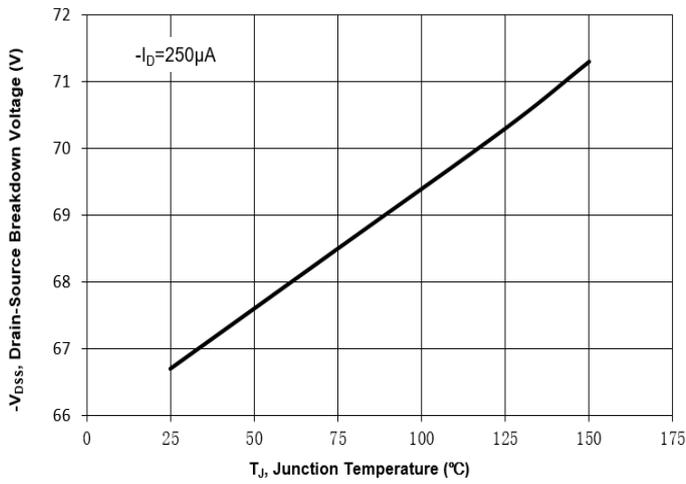


Fig. 8 Gate Threshold Variation vs. T_J

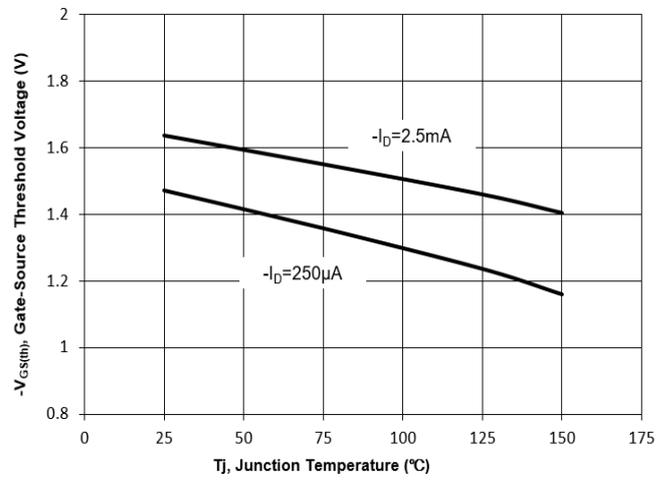


Fig. 9 Typical Junction Capacitance

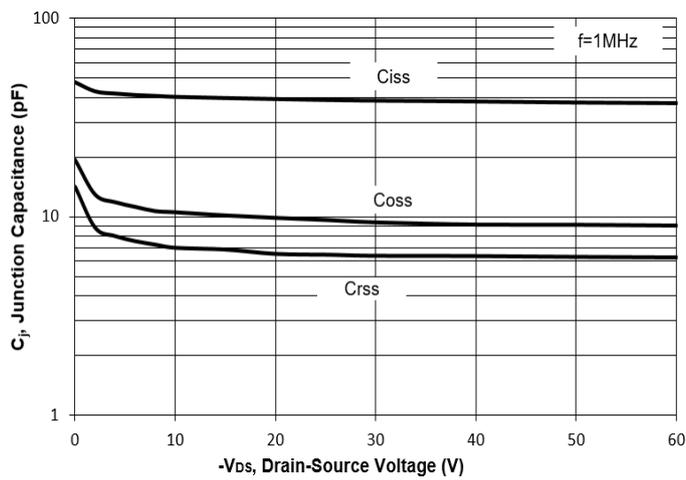


Fig. 10 Gate Charge

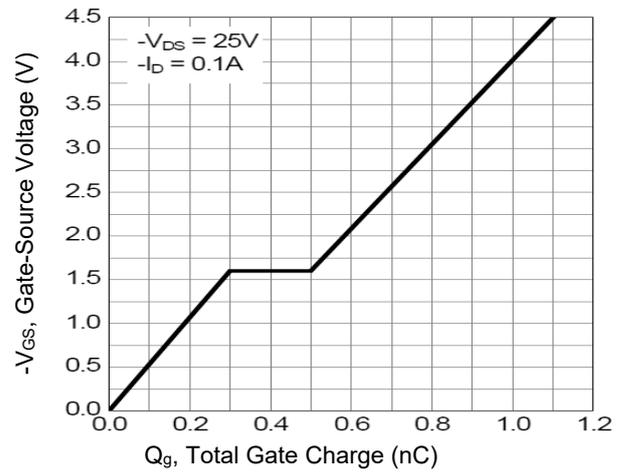
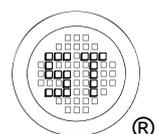
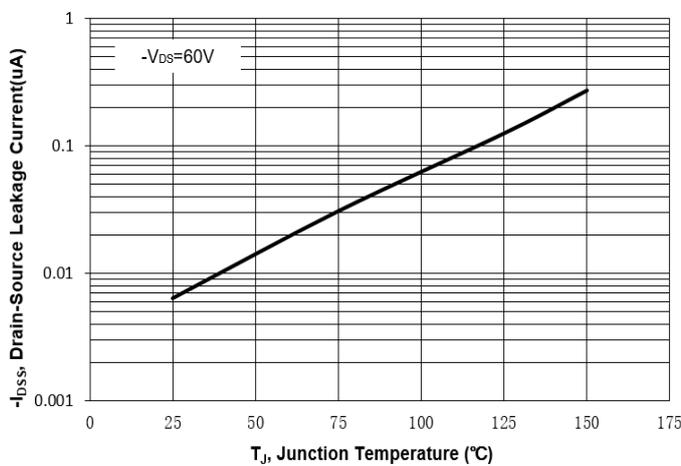


Fig. 11 Drain-Source Leakage Current vs. T_J



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Test Circuits

Fig.1-1 Switching times test circuit

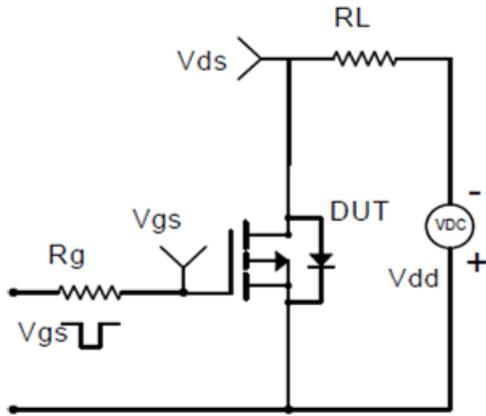


Fig.1-2 Switching Waveform

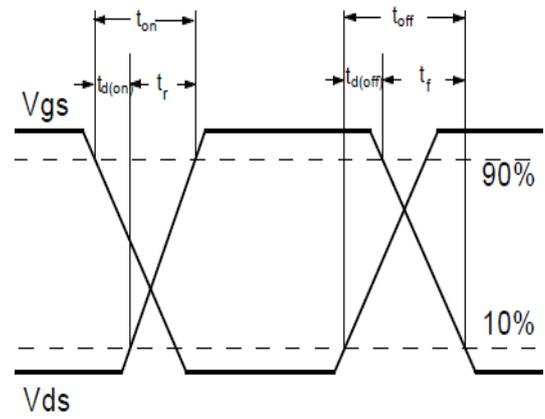


Fig.2-1 Gate charge test circuit

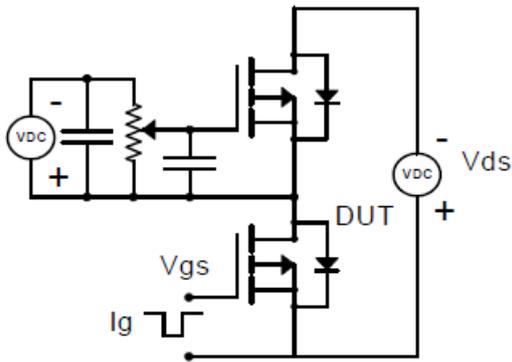
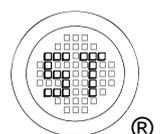
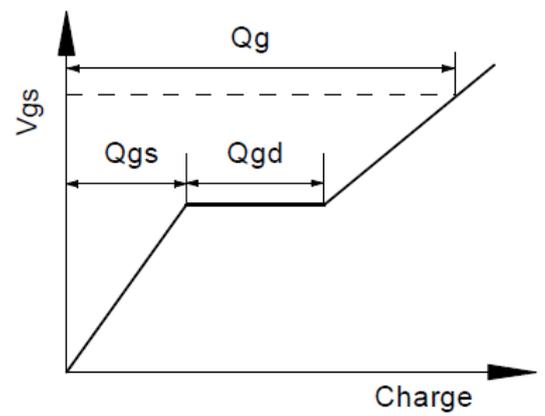


Fig.2-2 Gate charge waveform

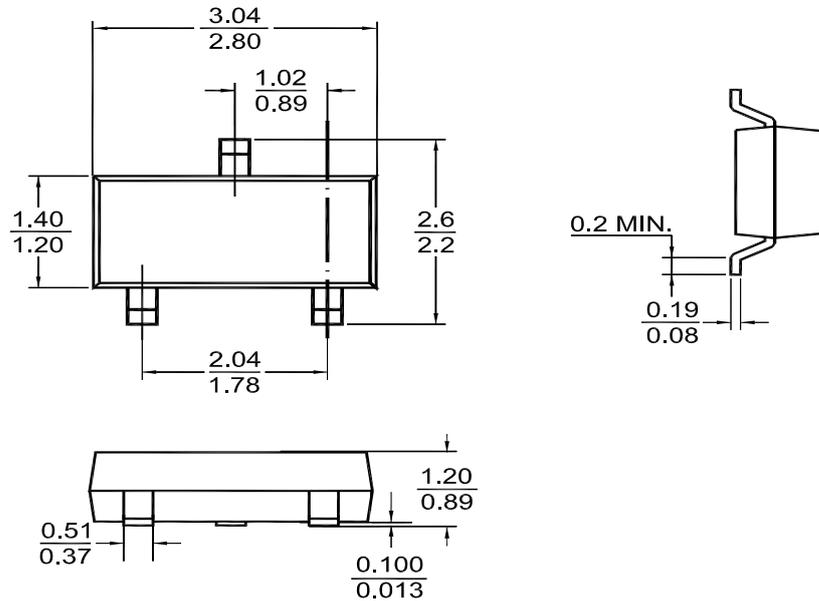


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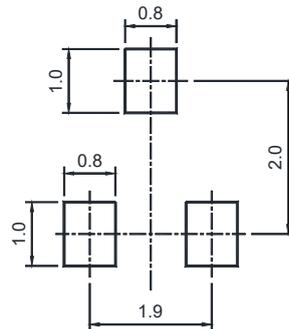
PACKAGE OUTLINE

Plastic surface mounted package (Dimensions in mm)

SOT-23



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-23	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

"VY" = Part No.
 "YM" = Date Code Marking
 "Y" = Year
 "M" = Month
 Font type: Arial

