XC6140 Series

ETR02050-002b

Voltage monitoring IC for rechargeable batteries with CV charging.
(Release Voltage 2.475V, Hysteresis width 0.275V~0.875V, Ultra low power Voltage Detector.)

■GENERAL DESCRIPTION

The XC6140 series are battery voltage monitoring ICs optimal to CV rechargeable batteries and electric double layer capacitors.

By setting release voltage to 2.475V and increasing the hysteresis width, it is possible to continue to output the release signal even in the voltage drop of the rechargeable batteries with high internal impedance due to inrush current.

When the battery voltage drops, it is possible to make the subsequent system stop and stand by on the rear stage until the charging is completed by setting the output signal at detection state.

In addition, hysteresis width is selectable in the range from 0.275V to 0.875V. So based on the internal impedance or over discharge voltage of a rechargeable battery, hysteresis width can be decided.

The SSOT-24 as well as ultra-small and low profile package USPQ-4B05 are available contributing to miniaturization of portable devices and high densely mounting applications.

Even when V_{IN} voltage is lower than the minimum operating voltage, malfunction of the system can be avoided by the undefined operation prevention function which minimizes the rise of output voltage.

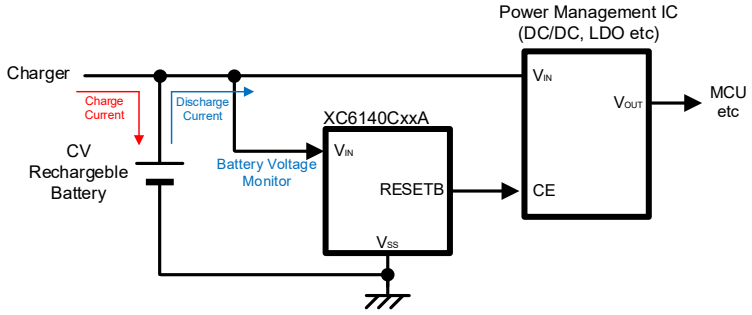
■APPLICATIONS

- Voltage monitoring for rechargeable batteries with CV charging.
- Voltage monitoring for electric double layer capacitors

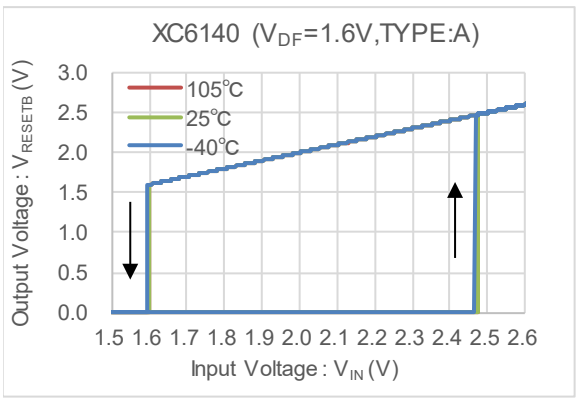
■ FEATURES

Operating Voltage Range	: 1.1V ~ 6.0V
Release Voltage	: 2.475V
Detect Voltage	: 1.6V ~ 2.2V (0.1V increments)
Release Voltage Accuracy	: ± 1.3% (Ta=25℃) ± 3.0% (Ta=-40℃~ 105℃)
Detection Voltage Accuracy	: ± 0.8% (Ta=25℃) : ± 2.5% (Ta=-40℃~ 105℃)
Temperature Characteristics	: ± 50ppm/℃ (TYP.)
Ultra-Low Power	: 104nA TYP.(@detect, V_{DF}=1.6V, V_{IN}=1.44V) 139nA TYP.(@release, V_{IN}=2.7V)
Output type	: CMOS Nch open drain
Output logic	: RESETB (Active Low) RESET (Active High)
Undefined operation Protection (CMOS Output only)	: Output pin Voltage 0.38V (MAX: Ta=-40℃~105℃) @Power supply Input pin Voltage＜ Operating voltage (MIN.)
Operating Ambient Temperature	: -40℃ ~ 105℃
Packages	: USPQ-4B05 (1.0 x 1.0 x 0.33mm) SSOT-24 (2.0 x 2.1 x 1.1mm)
Environment friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

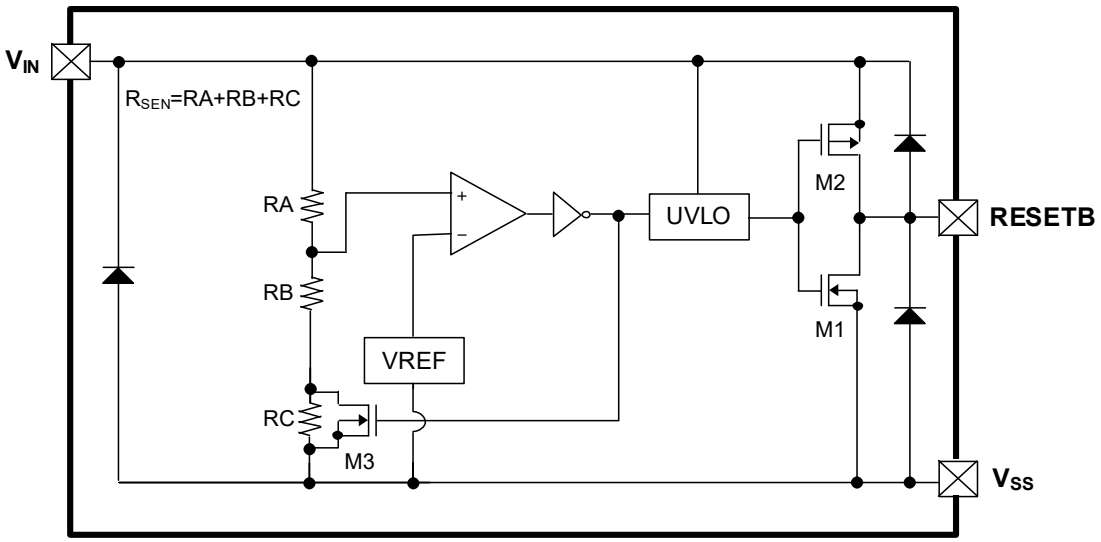


■TYPICAL PERFORMANCE CHARACTERISTICS



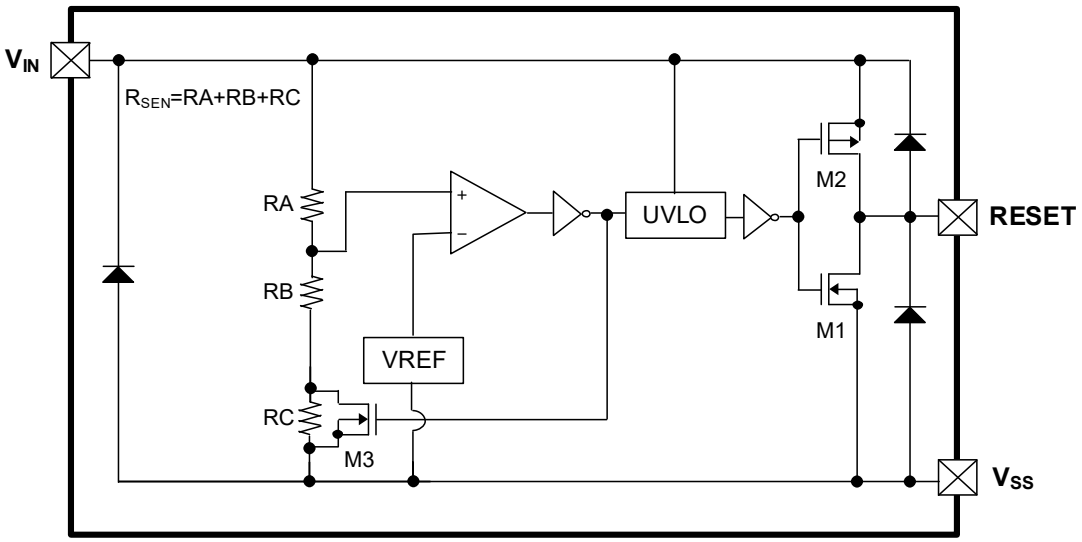
■BLOCK DIAGRAMS

(1) XC6140C Series A type (RESETB OUTPUT : CMOS output / Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

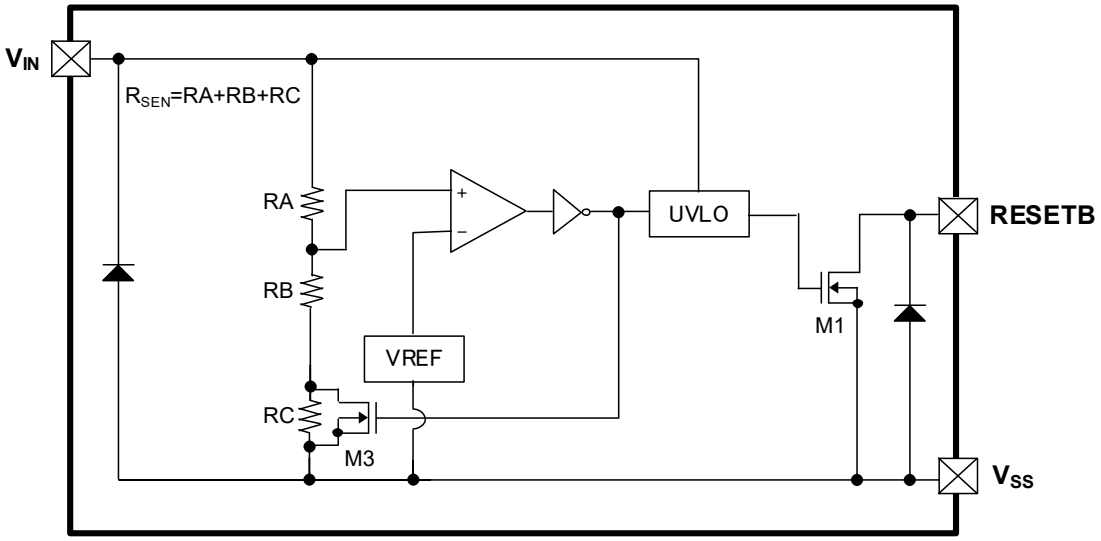
(2) XC6140C Series C type (RESET OUTPUT : CMOS output / Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

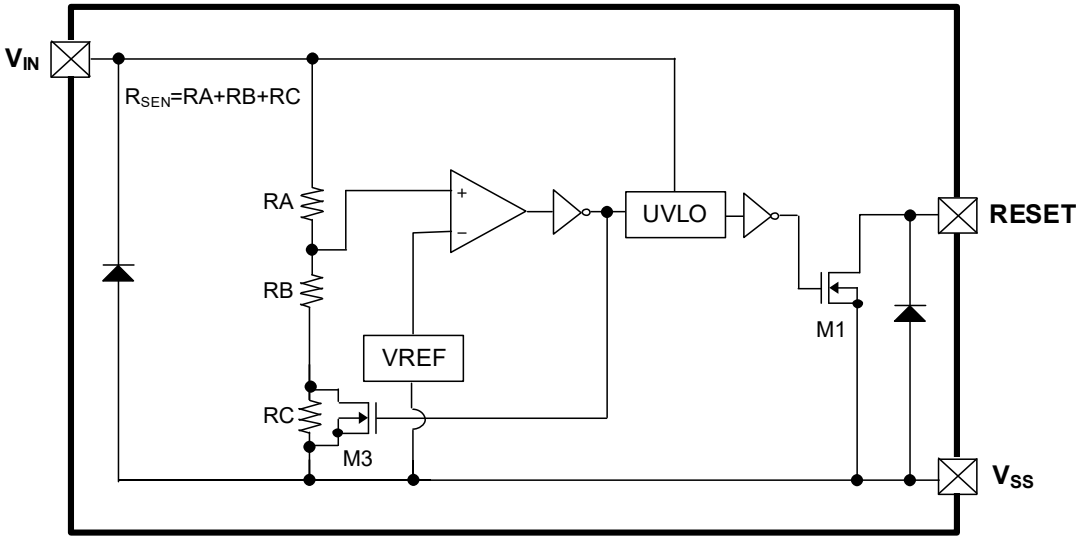
■BLOCK DIAGRAMS(Continued)

(3) XC6140N Series A type (RESETB OUTPUT : Nch open drain output / Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

(4) XC6140N Series C type (RESET OUTPUT : Nch open drain output / Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

■PRODUCT CLASSIFICATION

●Ordering Information

XC6140①②③④⑤⑥-⑦(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	Nch open drain output
②③	Detect Voltage	16 ~ 22	e.g. 1.6V → ②=1, ③=6 * 0.1V increments
④	Type	A	Refer to Selection Guide
		C	
⑤⑥-⑦(*1)	Packages (Order Unit)	9R-G	USPQ-4B05 (5,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)

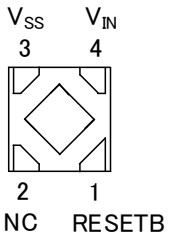
(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

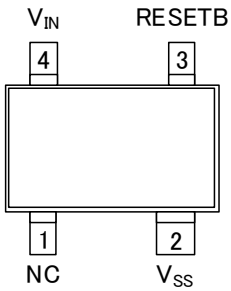
TYPE	RESET OUTPUT	OUTPUT PIN NAME	DESCRIPTION
A	Active Low	RESETB	Output Low level in detection state.
C	Active High	RESET	Output High level in detection state.

■ PIN CONFIGURATION

●Type : A

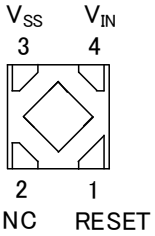


USPQ-4B05
(BOTTOM VIEW)

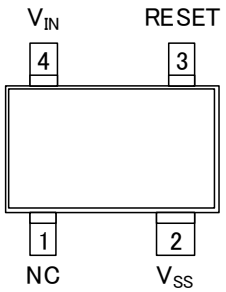


SSOT-24
(TOP VIEW)

●Type : C



USPQ-4B05
(BOTTOM VIEW)



SSOT-24
(TOP VIEW)

* The dissipation pad for the USPQ-4B05 package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to V_{SS} (No.3) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
USPQ-4B05	SSOT-24		
1	3	RESETB	Reset Output (Active Low)
		RESET	Reset Output (Active High)
2	1	NC	No Connection
3	2	V_{SS}	Ground
4	4	V_{IN}	Power Supply Input

■LOGIC CHART

TYPE	OUTPUT Configuration	Reset Output		
		Release State	Detection State /UVLO operating State	Undefined State ($V_{IN} \leqq V_{INL}$:0.4V)
A	Nch open drain	"H" (Vpull : High impedance)	"L" (GND : Low Impedance)	"H" (Vpull : High impedance)
	CMOS	"H" (V_{IN})	"L" (GND)	V_{UNO} (TYP. 0.1V)
C	Nch open drain	"L" (GND : Low Impedance)	"H" (Vpull : High impedance)	"H" (Vpull : High impedance)
	CMOS	"L" (GND)	"H" (V_{IN})	Undefined

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL		RATINGS	UNITS
Input Voltage		V_{IN}		-0.3 ~ 7.0	V
Output Voltage	XC6140C	V_{RESETB}	V_{RESET}	V_{SS} - 0.3 ~ V_{IN} + 0.3 or 7.0 (*1)	V
	XC6140N			V_{SS} - 0.3 ~ 7.0	V
Output Current	XC6140C	I_{RBOUT}	I_{ROUT}	±50	mA
	XC6140N			50	
Power Dissipation (Ta=25℃)	USPQ-4B05	Pd		550 (40mm x 40mm Standard board) (*2)	mW
	SSOT-24			680 (JESD51-7 board) (*2)	
Operating Ambient Temperature		Topr		-40 ~ 105	℃
Storage Temperature		Tstg		-55 ~ 125	℃

* All voltages are described based on the V_{SS}.
(*1) The maximum value should be either V_{IN}+0.3V or 7.0V in the lowest.
(*2) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦105℃(*4)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}		1.1		6.0	1.1		6.0	V	①
MIN Voltage Holding the Detection(*3) (CMOS output)	V_{INL}		-	-	0.4	-	-	0.4	V	
Detect Voltage	V_{DF}	$V_{DF(T)}$(*1)=1.6V~2.2V	$V_{DF(T)}$ ×0.992	$V_{DF(T)}$	$V_{DF(T)}$ ×1.008	$V_{DF(T)}$ ×0.975	$V_{DF(T)}$	$V_{DF(T)}$ ×1.025	V	
Release Voltage	V_{DR}		2.443	2.475	2.507	2.401	2.475	2.549	V	
Detect Voltage Temperature Characteristics	$\Delta V_{DF}/(\Delta Topr \cdot V_{DF})$		-	±50	-	-	±50	-	ppm/℃	
Supply Current1 (CMOS output, A Type)	I_{ss1}	$V_{IN} = V_{DF} \times 0.9$	-	E-3		-	E-4		nA	②
Supply Current1 (CMOS output, C Type)							E-5			
Supply Current1 (Nch open drain output , A/C Type)							E-6			
Supply Current2 (CMOS output, A Type)	I_{ss2}	V_{IN} = 2.7V	-	139	289	-	139	431		
Supply Current2 (CMOS output, C Type)							139	580		
Supply Current2 (Nch open drain output , A/C Type)							139	433		
Peak of Undefined Operation (CMOS output, A Type)	V_{UNO}	V_{IN} < 0.4V	-	0.1	0.38	-	0.1	0.38	V	③
UVLO Release Voltage	V_{UVLOR}	V_{IN} = 0V→1.1V	-	0.82	1.05(*2)	-	0.82	1.07	V	-
UVLO Detect Voltage	V_{UVLOD}	V_{IN} = 1.1V→0V	0.57(*2)	0.79	-	0.55	0.79	-		
UVLO Release Delay Time	t_{UVLOR}	V_{IN} = 0V→1.1V	-	157	290(*2)	-	157	425	μs	-

(*1) $V_{DF(T)}$: Nominal detect voltage
(*2) The MIN. and MAX. specifications related to UVLO are setting values.
(*3) V_{IN} value where RESETB < 0.05V or RESET > V_{IN} - 0.05V.
(*4) The ambient temperature range (-40℃≦Ta≦105℃) is a design value.

■ELECTRICAL CHARACTERISTICS(Continued)

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦105℃(*4)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Release Delay Time(*5)	t_{DR0}	$V_{IN}=V_{DF}\times0.9\rightarrow V_{DF}\times1.1$	-	44	200	-	44	224	μs	④
Detect Delay Time(*6)	t_{DF0}	$V_{IN}=V_{DF}\times1.1\rightarrow V_{DF}\times0.9$	-	40	170	-	40	184		
RESETB Output Current	I_{RBOUTN}	Nch. V_{RESETB}=0.3V							mA	⑤
		V_{IN}=1.1V	0.3	1.4	-	0.2	1.4	-		
		V_{IN}=2.0V ($V_{DF(T)}\geqq2.1V$)	4.1	6.2	-	3.1	6.2	-		
	I_{RBOUTP}	Pch. $V_{RESETB}=V_{IN}$-0.3V								
		V_{IN}=3.0V	-	-3.2	-1.4	-	-3.2	-1.3		
		V_{IN}=6.0V	-	-5.1	-2.9	-	-5.1	-2.6		
RESET Output Current	I_{ROUTN}	Nch. V_{RESET}=0.3V							mA	
		V_{IN}=2.0V ($V_{DF(T)}\leqq1.9V$)	4.1	6.2	-	3.1	6.2	-		
		V_{IN}=3.0V	8.1	10.8	-	4.3	10.8	-		
		V_{IN}=4.0V	11.2	14.3	-	6.2	14.3	-		
		V_{IN}=5.0V	13.7	17.1	-	7.3	17.1	-		
		V_{IN}=6.0V	15.7	19.3	-	8.1	19.3	-		
	I_{ROUTP}	Pch. $V_{RESET}=V_{IN}$-0.3V								
		V_{IN}=1.1V	-	-0.7	-0.2	-	-0.7	-0.15		
RESETB Output Leakage Current	I_{LEAKN}(*7)	V_{IN}=6.0V Nch. V_{RESETB}=6.0V	-	0.01	0.1	-	0.01	0.3	μA	
	I_{LEAKP}	V_{IN}=1.1V Pch. V_{RESETB}=0V	-	-0.01	-	-	-0.01	-		
RESET Output Leakage Current	I_{LEAKN}(*7)	V_{IN}=1.1V Nch. V_{RESET}=6.0V	-	0.01	0.1	-	0.01	0.3		
	I_{LEAKP}	V_{IN}=6.0V Pch. V_{RESET}=0V	-	-0.01	-	-	-0.01	-		

(*5) RESETB product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches $V_{IN}\times90\%$.
RESET product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches $V_{IN}\times10\%$
(*6) RESETB product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches $V_{IN}\times10\%$.
RESET product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches $V_{IN}\times90\%$.
(*7) Max. value is for XC6140N (Nch open drain).

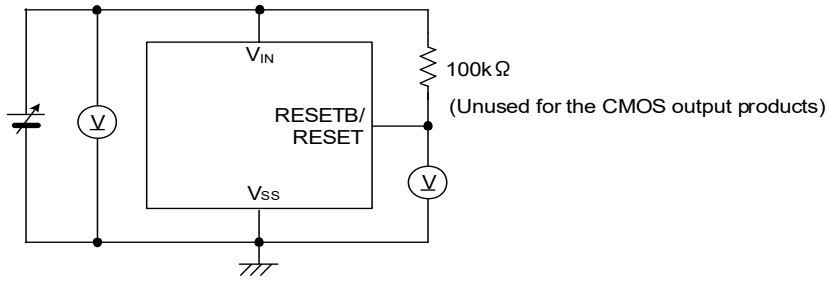
■ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

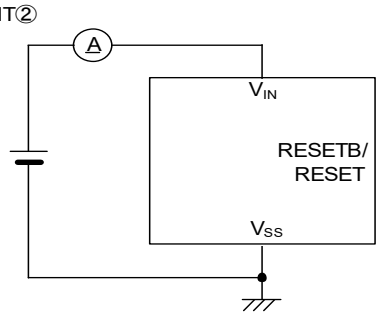
NOMINAL DETECT VOLTAGE(V)	E-3		E-4		E-5		E-6	
	Ta=25℃		-40℃≦Ta≦105℃					
	Supply Current1 (nA)							
$V_{DF(T)}$	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
1.6	104	235	104	457	104	351	104	364
1.7	108	240	108	464	108	357	108	371
1.8	111	245	111	471	111	363	111	377
1.9	114	251	114	478	114	370	114	384
2.0	117	256	117	484	117	376	117	390
2.1	121	262	121	491	121	383	121	397
2.2	124	267	124	498	124	389	124	403

■TEST CIRCUITS

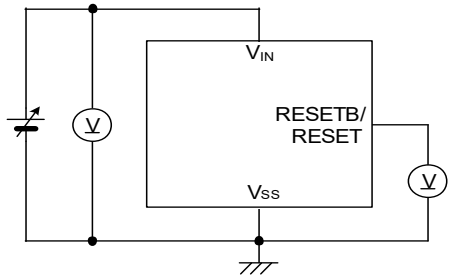
CIRCUIT①



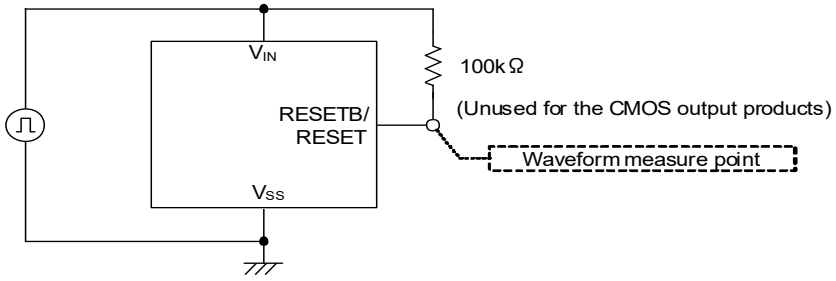
CIRCUIT②



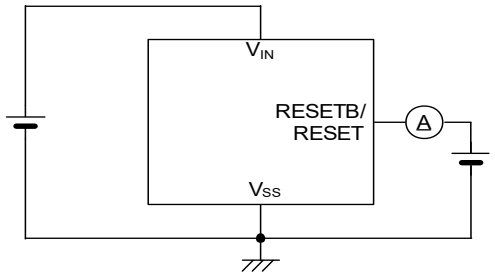
CIRCUIT③



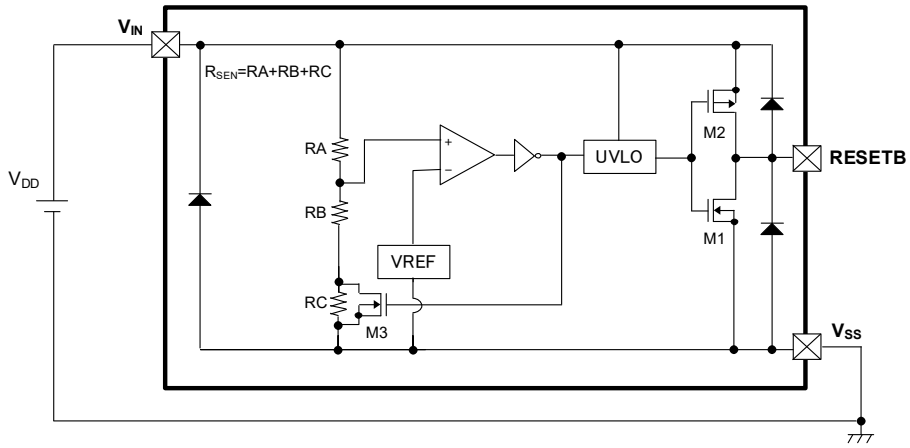
CIRCUIT④



CIRCUIT⑤



■OPERATIONAL DESCRIPTION (Active Low)



Typical block diagram (CMOS output/Active Low product)

The circuit operation in the above representative circuit example will be explained using the timing chart.

③ (③') Detection state

The RESETB pin will hold “L” until the V_{IN} pin voltage becomes equal to or greater than the release voltage (V_{DR}).

③→④ Transition from detection state to released state

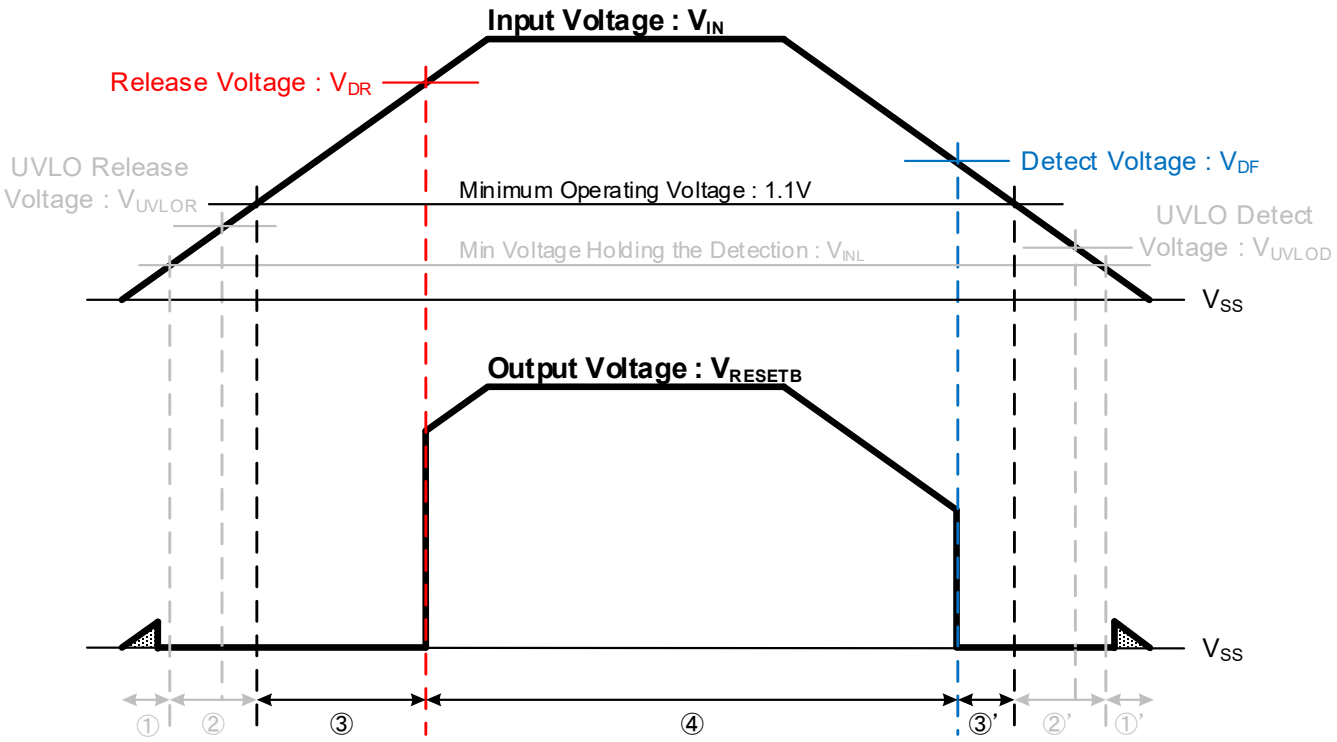
When the V_{IN} pin voltage reaches the release voltage (V_{DR}), the circuit will determine that the monitoring voltage has exceeded the release level. After the release delay time (t_{DR0}) has passed, it will turn M3 OFF and output “H” to the RESETB pin.

④ Released state

The RESETB pin will hold “H” until the V_{IN} pin voltage becomes equal to or less than the detection voltage (V_{DF}).

④→③' Transition from released state to detection state

When the V_{IN} pin voltage reaches the detection voltage (V_{DF}), the circuit will determine that the monitoring voltage has fallen below the detection level. After the detect delay time (t_{DF0}) has passed, it will turn M3 ON and output “L” to the RESETB pin.



■OPERATIONAL DESCRIPTION (Active Low)

●Operation below Minimum Operating Voltage

②(②') Detection holding state

If the V_{IN} pin voltage is equal to or greater than the minimum voltage holding the detection (V_{INL}), the operation of the UVLO function will cause the RESETB pin to maintain “L” (= detection state).

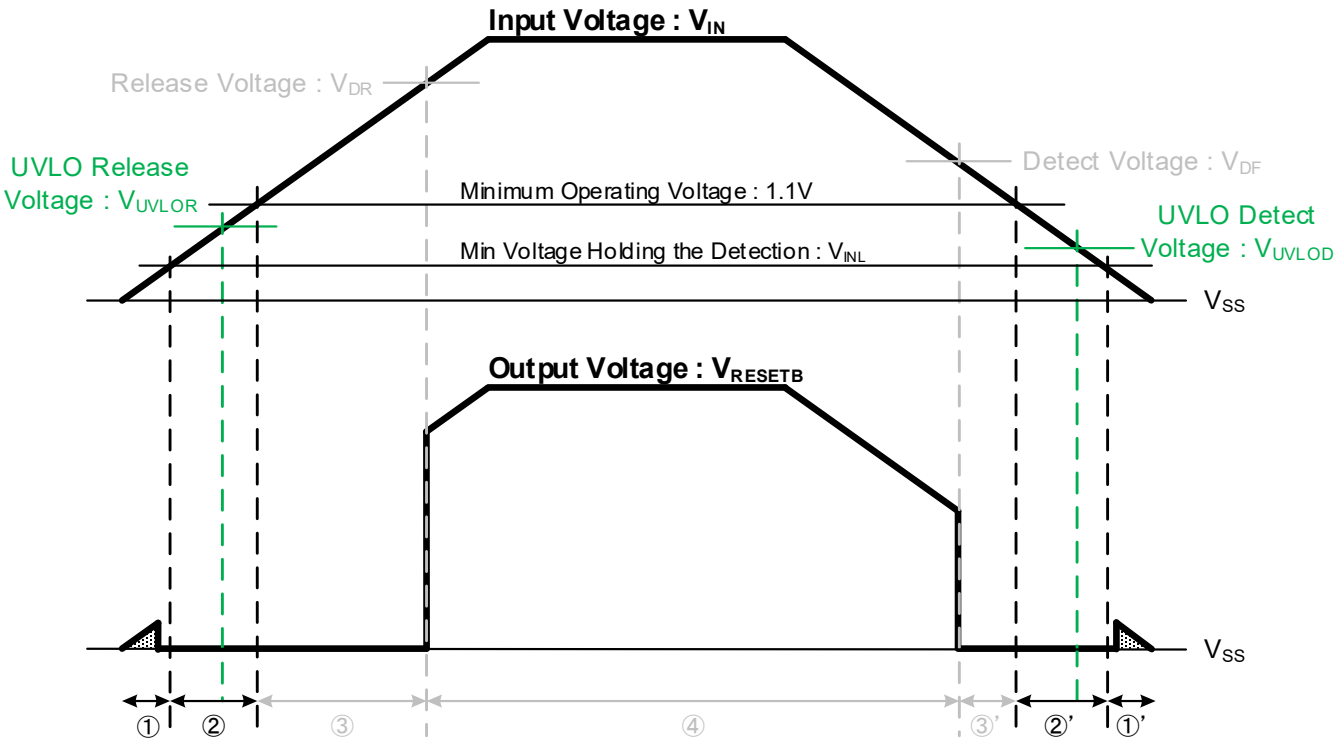
② Following the operation of the UVLO function, after the V_{IN} pin voltage reaches the UVLO release voltage (V_{UVLOR}), the UVLO function will be released once the UVLO release delay time (t_{UVLOR}) has passed.

②' If the V_{IN} pin voltage falls to the UVLO detect voltage (V_{UVLOD}), the UVLO function will operate and the RESETB pin will maintain “L”.

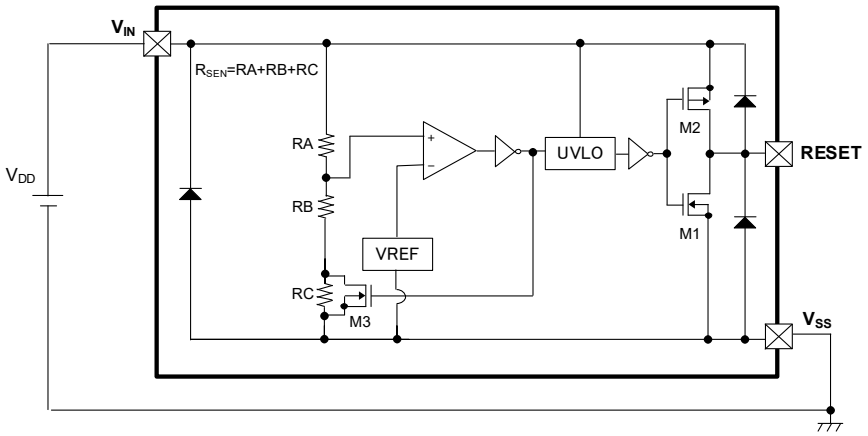
① (①') Undefined state

If the V_{IN} pin voltage is less than the minimum voltage holding the detection (V_{INL}), the UVLO function will not be able to operate properly, and the RESETB pin will be in an undefined state.

* The above operation description is for CMOS output products, but for Nch open drain products, the pull-up destination voltage will be output to the RESETB pin until FET M1 becomes ON state.



■OPERATIONAL DESCRIPTION (Active High)



Typical block diagram (CMOS output/Active High product)

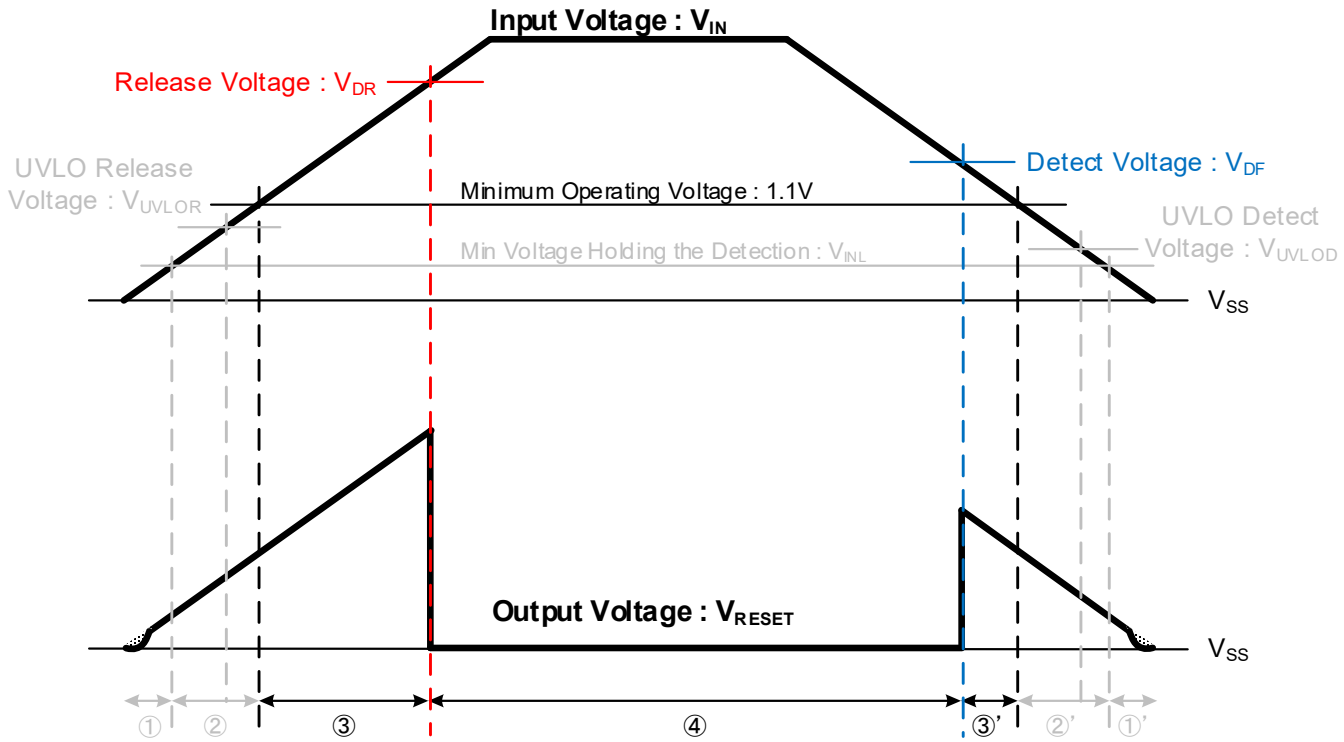
The circuit operation in the above representative circuit example will be explained using the timing chart.

③ (③') Detection state
The RESET pin will hold “H” until the V_{IN} pin voltage becomes equal to or greater than the release voltage (V_{DR}).

③→④ Transition from detection state to released state
When the V_{IN} pin voltage reaches the release voltage (V_{DR}), the circuit will determine that the monitoring voltage has exceeded the release level. After the release delay time (t_{DR0}) has passed, it will turn M3 OFF and output “L” to the RESET pin.

④ Released state
The RESET pin will hold “L” until the V_{IN} pin voltage becomes equal to or less than the detection voltage (V_{DF}).

④→③' Transition from released state to detection state
When the V_{IN} pin voltage reaches the detection voltage (V_{DF}), the circuit will determine that the monitoring voltage has fallen below the detection level. After the detect delay time (t_{DF0}) has passed, it will turn M3 ON and output “H” to the RESET pin.



■OPERATIONAL DESCRIPTION (Active High)

●Operation below Minimum Operating Voltage

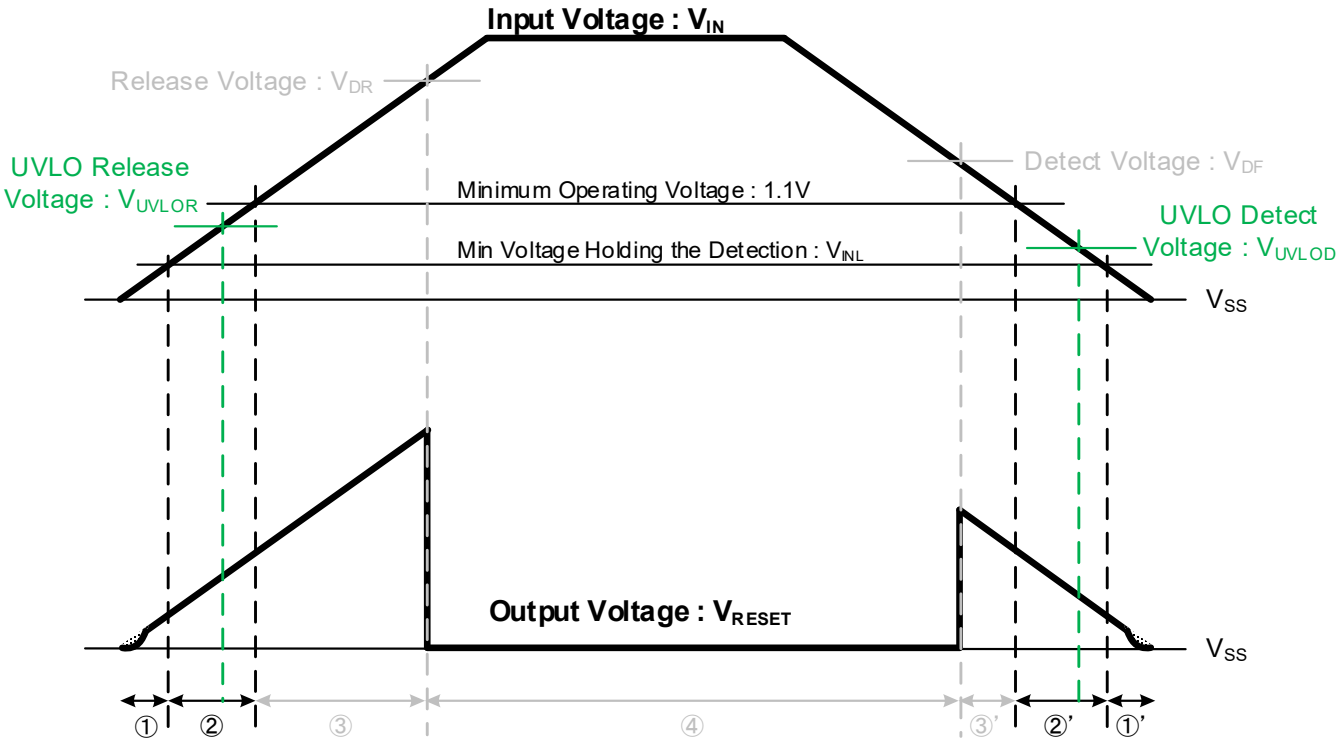
②(②') Detection holding state
If the V_{IN} pin voltage is equal to or greater than the minimum voltage holding the detection (V_{INL}), the operation of the UVLO function will cause the RESET pin to maintain “H” (= detection state).

② Following the operation of the UVLO function, after the V_{IN} pin voltage reaches the UVLO release voltage (V_{UVLOR}), the UVLO function will be released once the UVLO release delay time (t_{UVLOR}) has passed.

②' If the V_{IN} pin voltage falls to the UVLO detect voltage (V_{UVLOD}), the UVLO function will operate and the RESET pin will maintain “H”.

① (①') Undefined state
If the V_{IN} pin voltage is less than the minimum voltage holding the detection (V_{INL}), the UVLO function will not be able to operate properly, and the RESET pin will be in an undefined state.

* The above operation description is for CMOS output products, but for Nch open drain products, the pull-up destination voltage will be output to the RESET pin until FET M1 becomes ON state.



■OPERATIONAL DESCRIPTION

< Pull-up Resistance Selection Method >

When an Nch open drain output is used, the V_{RESETB} voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.

The selection method and calculation examples for the pull-up resistance with Active Low products are explained below.
To calculate the V_{RESET} voltage (Active High product), calculate by inverting the logic at detection and release.

【At detection : Lower Limit of pull-up resistance】

$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{ON})$
V_{pull} : Voltage after pull-up
R_{ON}(*1) : ON resistance of N-ch driver M1 (calculated from V_{RESETB}/I_{RBOUTN} based on electrical characteristics)

Example: When V_{IN}=2.0V(*2) ,
$R_{ON} = 0.3V / (4.1 \times 10^{-3} A) \fallingdotseq 73.2\Omega$ (MAX.)
If it is desired to make V_{RESETB} at detection 0.1V or less when V_{pull} is 3.0V,
$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{ON} = \{ (3V / 0.1V) - 1 \} \times 73.2\Omega \fallingdotseq 2.1k\Omega$

Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.1kΩ or higher.
(*1) Note that R_{ON} becomes larger as V_{IN} becomes smaller.
(*2) For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

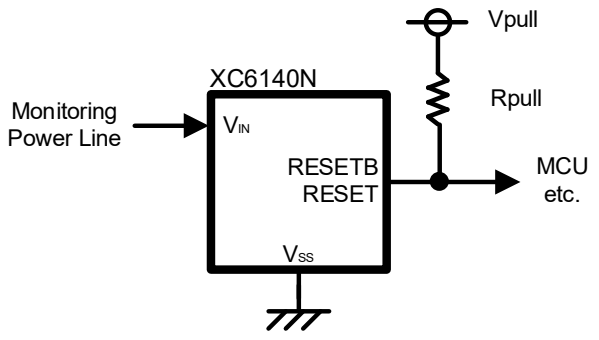
【At release : Upper limit of pull-up resistance】

$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{off})$
V_{pull} : Voltage after pull-up
R_{off} : Resistance when N-ch driver M1 is OFF (calculated from V_{RESETB}/I_{LEAKN} based on electrical characteristics)

Example: When V_{pull} is 6.0V,
$R_{off} = 6V / (0.1 \times 10^{-6} A) = 60M\Omega$ (MIN.).
If it is desired to make V_{RESETB} 5.99V or higher,
$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{off} = \{ (6V / 5.99V) - 1 \} \times 60 \times 10^{6}\Omega \fallingdotseq 100k\Omega$

Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100kΩ or less.

Also, use a value of 6.0V or less for the pull-up voltage.



Pull-up resistance (Nch Open Drain)

■NOTES ON USE

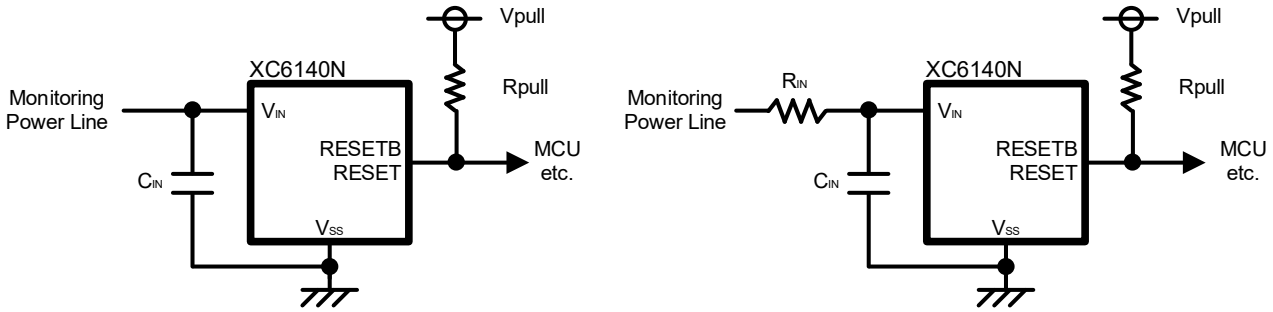
(1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

(2) Factors such as the V_{IN} pin voltage slope, surrounding components, or noise from external sources may cause the conditions indicated in (a) ~ (c) below to occur.
If these conditions occur, carry out measures such as inserting a capacitor between V_{IN} and V_{SS}, if necessary.
(Indicated in the following diagram.)

(a) If a resistance is inserted between the power supply and V_{IN} pin, the V_{IN} pin voltage may drop due to the flow-through current and resistance generated during detection and release.
In addition, with CMOS output products the drop in V_{IN} pin voltage may become larger due to the output current.
This temporary drop in V_{IN} pin voltage may cause oscillation of the output and malfunctions.

(b) If the V_{IN} pin voltage has a steep slope, it may cause the output voltage to float or other such unstable operation to occur.

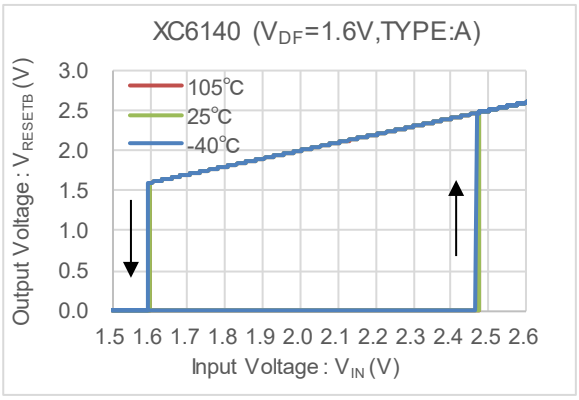
(c) Power supply noise from external sources may cause IC malfunctions.

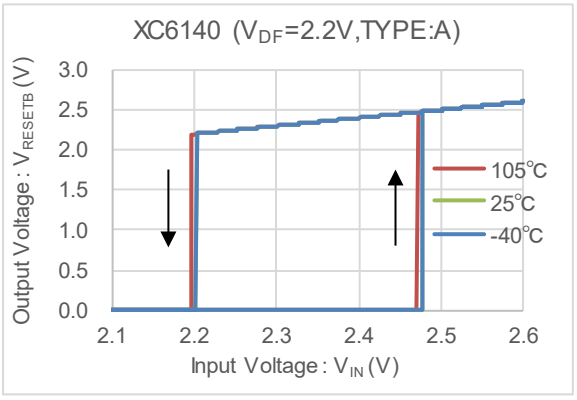


(3) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

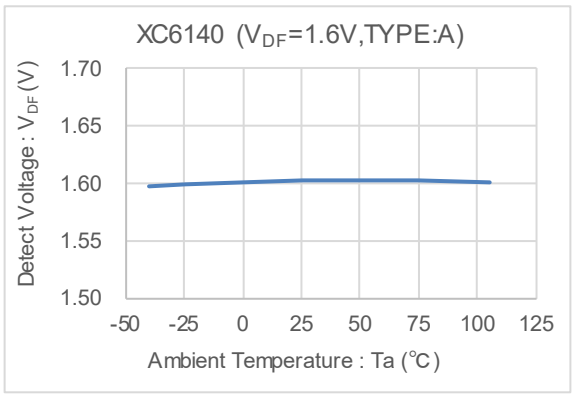
■TYPICAL PERFORMANCE CHARACTERISTICS

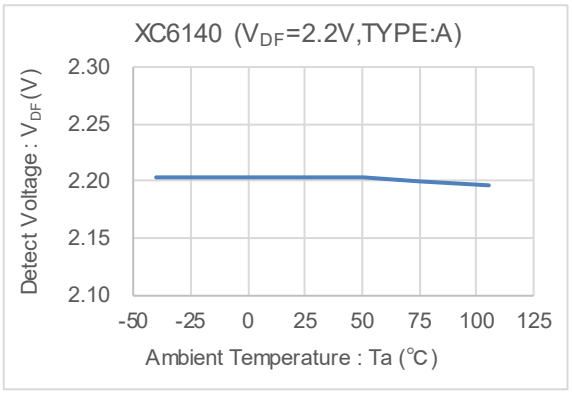
(1)Output Voltage vs. Input Voltage



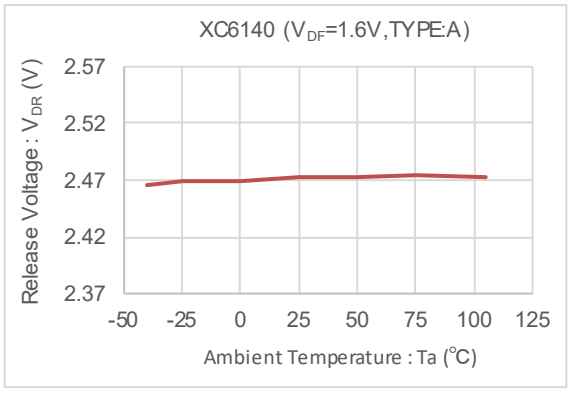


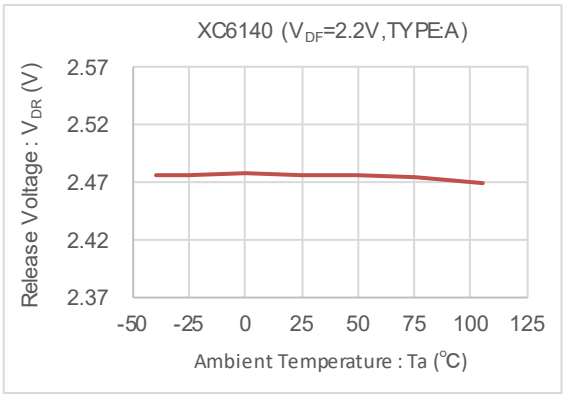
(2)Detect Voltage vs. Ambient Temperature



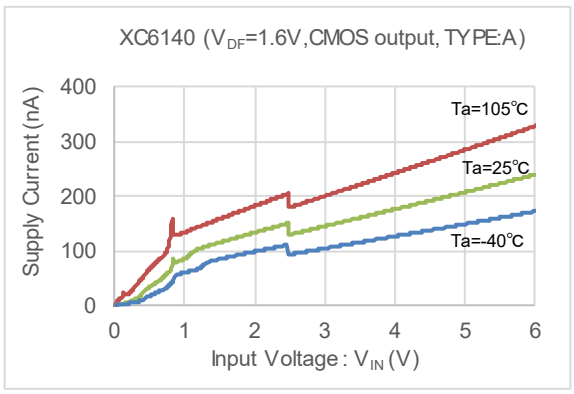


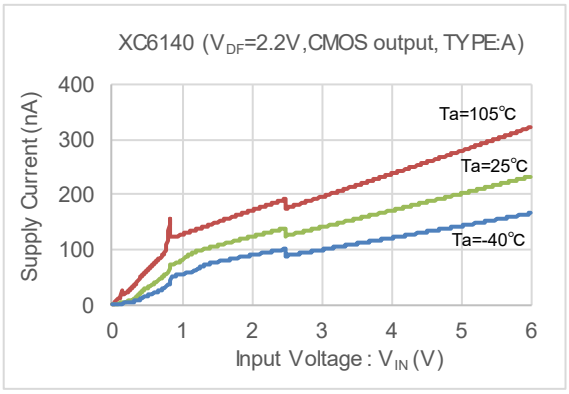
(3)Release Voltage vs. Ambient Temperature





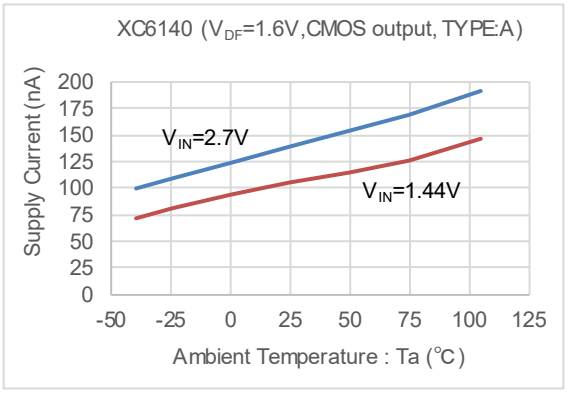
(4)Supply Current vs. Input Voltage

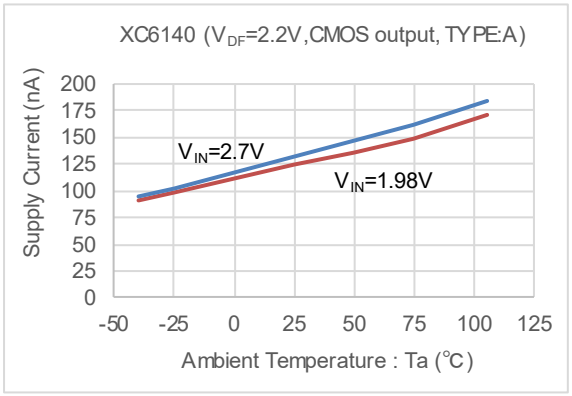




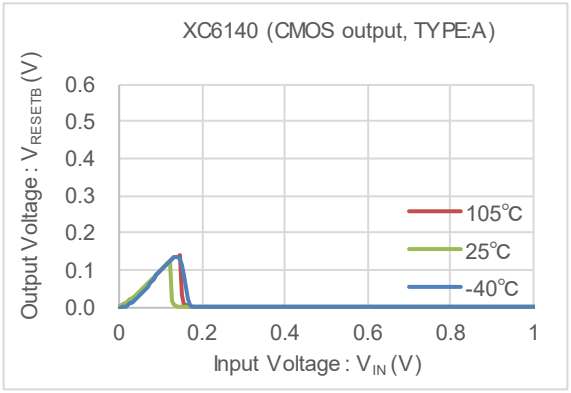
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

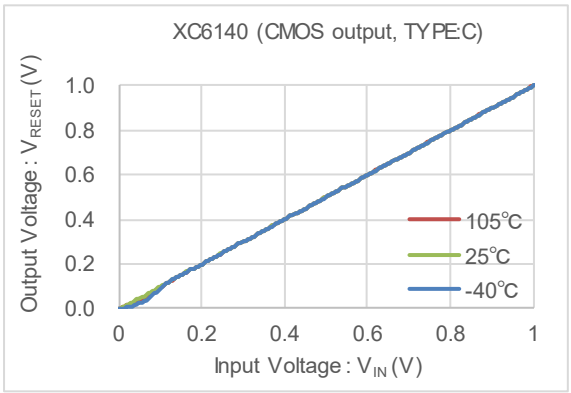
(5)Supply Current vs. Ambient Temperature



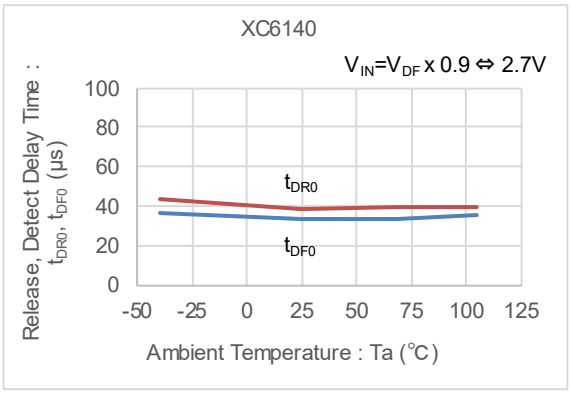


(6)Output Voltage vs. Input Voltage (V_{IN}<Operating Voltage)

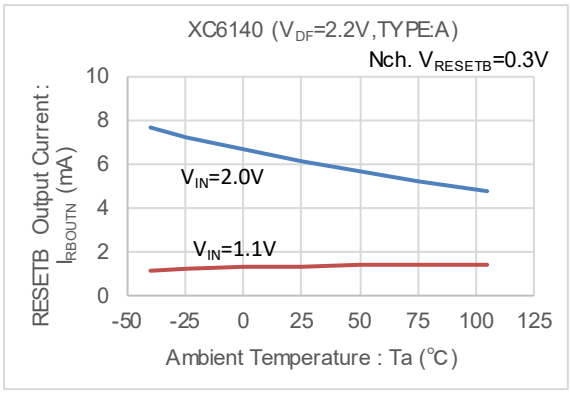


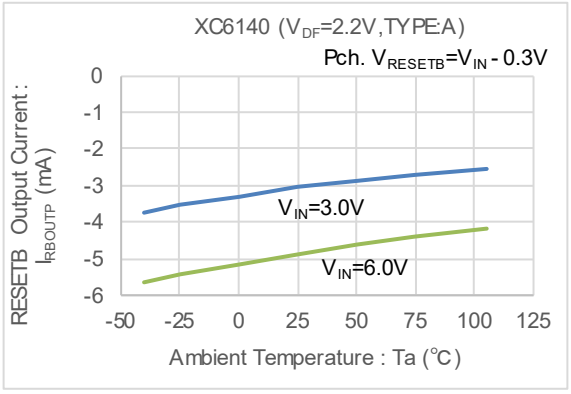


(7)Release, Detect Delay Time vs. Ambient Temperature

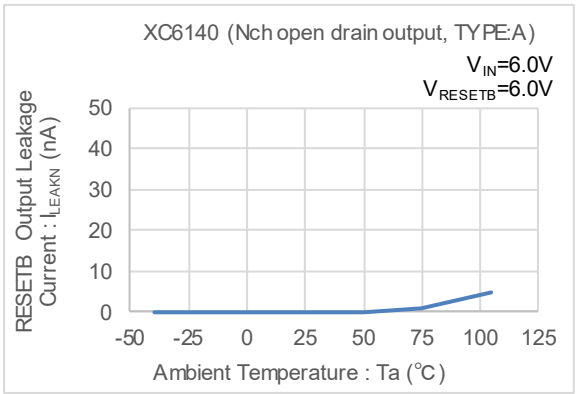


(8)RESETB Output Current vs. Ambient Temperature





(9)RESETB Output Leakage Current vs. Ambient Temperature



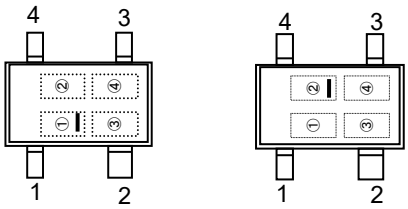
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

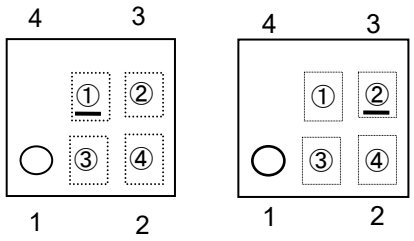
PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SSOT-24	SSOT-24 PKG	SSOT-24 Power Dissipation
USPQ-4B05	USPQ-4B05 PKG	USPQ-4B05 Power Dissipation

■MARKING RULE

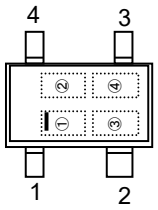
SSOT-24 (with underline mark)



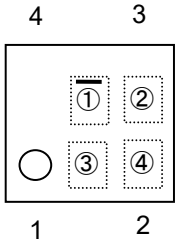
USPQ-4B05 (with underline mark)



SSOT-24 (with overline mark)



USPQ-4B05 (with overline mark)



① represents products series

MARK	Registration order	PRODUCT SERIES
X (with underline)	1	XC6140******-G
$\overline{1}$ (with overline)	2	
$\overline{3}$ (with overline)	3	
$\overline{5}$ (with overline)	4	
A (no line)	5	
B (no line)	6	
C (no line)	7	

*Mark ① is a common symbol and Mark ② is assigned a sequential number.

② represents internal sequential number

MARK ①	MARK ②
X (with under line)	No line
$\overline{\overline{1}}$ (with over line)	No line
$\overline{3}$ (with over line)	No line
$\overline{5}$ (with over line)	No line
A (no line)	Under line
B (no line)	Under line
C (no line)	Under line

0～9、A～Z repeated.
(G, I, J, O, Q, W excluded)

③,④ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～A9, AA～Z9 repeated.
(G, I, J, O, Q, W excluded)

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

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8. We assume no responsibility for damage or loss due to abnormal use.

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