USB Type-C Analog Audio and USB Switch

General Description

The RT8980H is a USB Type-C audio interface switch IC which supports analog audio headsets for mobile devices.

The RT8980H provides a general USB Type−C port to pass USB2.0 data signal (DP, DN), sideband use signal, analog audio R L signal, and analog microphone signal.

The RT8980H also supports high voltage protection for USB port and SBU port on USB Type−C receptacle side.

Ordering Information

RT8980H □

Package Type
WSC : WL-CSP-25B 2.21x2.25 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

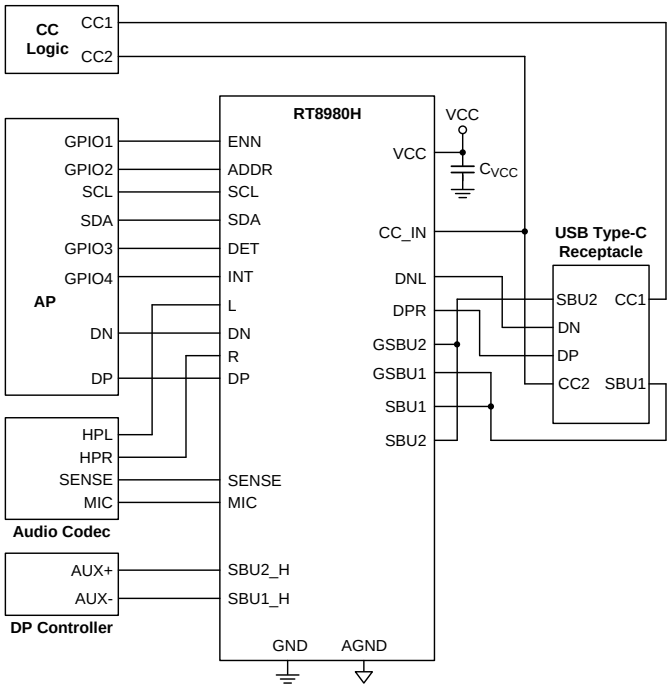
Features

- **Power Supply : V_{CC} = 2.7V to 5.5V**
- **High Absolute Maximum Ratings, 24V of SBU1/2 and GSBU1/2. 20V of DPR/DNL**
- **USB High Speed (480Mbps) Switch R_{ON} of 3Ω Typical**
- **Audio Switch R_{ON} of 1Ω Typical**
- **Negative Rail Capability : –3V to 3V**
- **THD + N = –110dB; $1V_{RMS}$, f = 20Hz to 20kHz, 32Ω Load**
- **OMTP and CTIA Pinout Support**
- **Support Audio Sense GND Path**

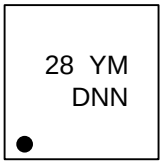
Applications

- Mobile Phones
- Tablets
- Notebooks/PCs
- USB-C Media Players

Simplified Application Circuit



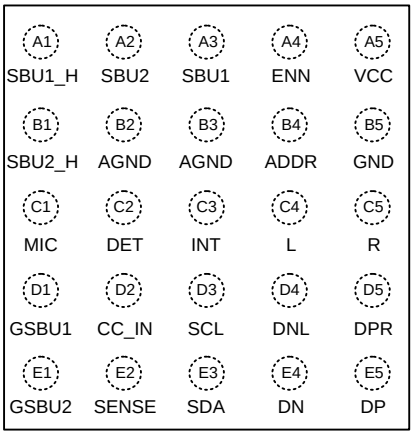
Marking Information



28 : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



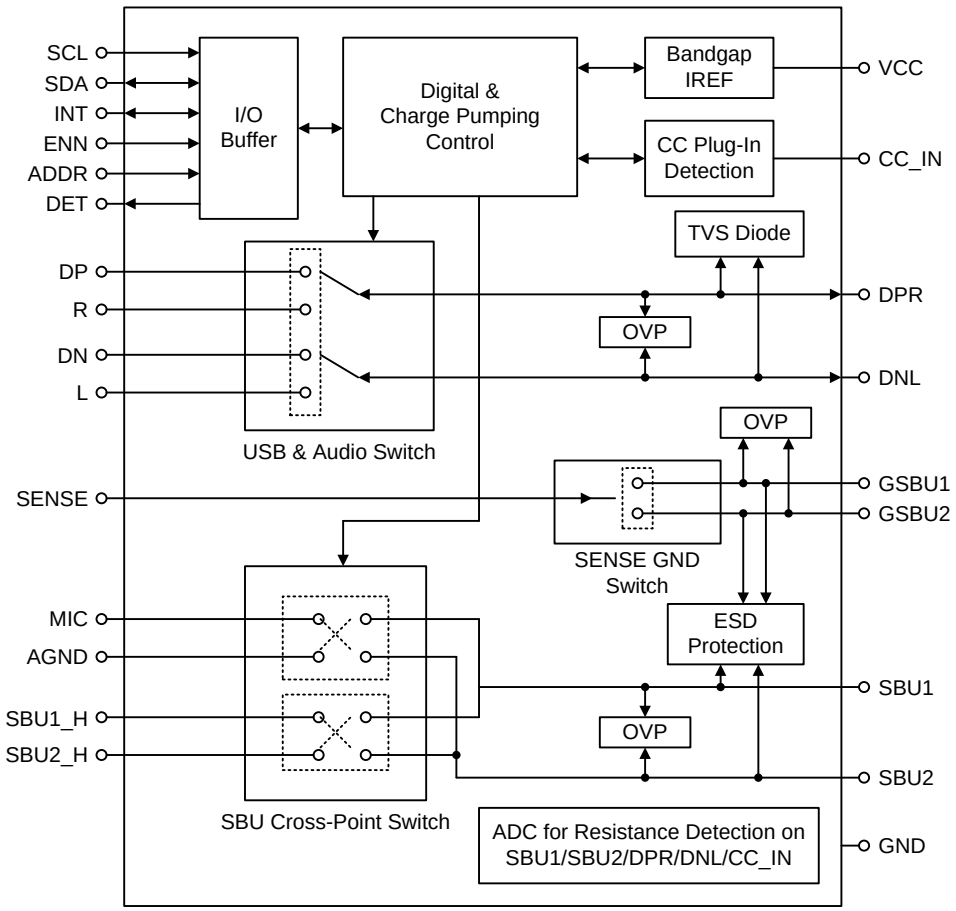
WL-CSP-25B 2.21x2.25 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	SBU1_H	Host side sideband uses wire 1.
A2	SBU2	Sideband use wire 2.
A3	SBU1	Sideband use wire 1.
A4	ENN	Chip enable. Active low, internal pull−down by 470kΩ.
A5	VCC	Power supply. (2.7 to 5.5V)
B1	SBU2_H	Host side sideband uses wire 2.
B2, B3	AGND	Audio signal ground.
B4	ADDR	I^2C slave address pin.
B5	GND	Chip ground.
C1	MIC	Microphone signal.
C2	DET	Push−pull output. When CC_IN > 1.5V, DET is low and CC_IN < 1.2V, DET is high.
C3	INT	I^2C Interrupt output, active low. (open drain) Manual mode input.
C4	L	Audio – left channel.
C5	R	Audio – right channel.
D1	GSBU1	Audio sense path 1 to headset jack GND.
D2	CC_IN	Audio accessory attachment detection input.
D3	SCL	I^2C interface serial clock input. An external pull-up resistor is required.
D4	DNL	USB/Audio common connector.
D5	DPR	USB/Audio common connector.
E1	GSBU2	Audio sense path 2 to headset jack GND.
E2	SENSE	Audio ground reference output.
E3	SDA	I^2C interface serial data input/output. Open-drain. An external pull-up resistor is required.
E4	DN	USB data. (Differential -)

Pin No.	Pin Name	Pin Function
E5	DP	USB data. (Differential +)

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- CC_IN/SBU1/SBU2/GSBU1/GSBU2 ---------- –0.5V to 24V
- DPR/DNL ---------- –3.6V to 20V
- R/L ---------- –3.6V to 6.5V
- VCC/DP/DN/MIC/SENSE/SBU1_H/SBU2_H/DET/INT ---------- –0.5V to 6.5V
- SCL/SDA/ENN/ADDR ---------- –0.5V to 6.5V
- Switch I/O Current, (Audio Path) ---------- –250mA to 250mA
- Switch I/O Current, (USB Path) ---------- 100mA
- Switch I/O Current, (MIC to SBUx/SBUx_H to SBUx) ---------- 50mA
- Switch I/O Current, (SENSE to GSBUx) ---------- 100mA
- Switch I/O Current, (AGND to SBUx) ---------- 500mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-25B 2.21x2.25 (BSC) ---------- 4.04W
- Package Thermal Resistance (Note 2)

  WL-CSP-25B 2.21x2.25 (BSC), θ_{JA} ---------- 30.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model)
  - Connector Side : SBU1, SBU2, DPR, DNL,

    GSBU1, GSBU2, CC_IN (Pin to GND) ---------- ±4kV
  - Power Pins : VCC (Pin to GND) ---------- ±2kV
  - Host Side Pins : The Rest Pins ---------- ±2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 2.7V to 5.5V
- USB Switch ---------- 0V to 3.6V
- AUDIO Switch ---------- –3.6V to 3.6V
- MIC Switch ---------- 0V to 3.6V
- SENSE Switch ---------- 0V to 3.6V
- SBU TO SBUx_H Switch ---------- 0V to 3.6V
- CC_IN Pin ---------- 0V to 5.5V
- Input Voltage High of Control Voltage (ENN/ADDR/SDA/SCL/INT) ---------- 1.3V to V_{CC}
- Input Voltage Low of Control Voltage (ENN/ADDR/SDA/SCL/INT) ---------- 0V to 0.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(V_{CC} = 2.7V to 5.5V, V_{CC} (Typ.) = 3.3V, T_A = –40°C to 85°C and T_A (Typ.) = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	USB switches on, SBUx to SBUx_H switches on V_{CC} : 2.7V to 5.5V	--	--	100	μA
		Audio switches on, MIC switch on and Audio GND switch on V_{CC} : 2.7V to 5.5V	--	--	120	μA
Quiescent Current	I_{CCZ}	ENN = L, 04H'b7 = 0 V_{CC} : 2.7V to 5.5V	--	--	7	μA
USB/AUDIO Common Pins : DPR, DNL						
Off Leakage Current of DPR and DNL	I_{OZ}	DNL, DPR = –3V to 3.6V V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Power−Off Leakage Current of DPR and DNL	I_{OFF}	DNL, DPR = 0V to 3.6V, Power off	–3	--	3	μA
Input OVP Lockout on DPR/DNL	V_{OV_TRIP}	Rising edge V_{CC} : 2.7V to 5.5V	4.5	5	5.3	V
Input OVP Hysteresis of DPR/DNL	V_{OV_HYS}	V_{CC} : 2.7V to 5.5V	--	0.3	0.55	V
AUDIO Switch						
On Leakage Current of Audio Switch	I_{ON}	DNL, DPR = −3V to 3V, DP, DN, R, L = Float V_{CC} : 2.7V to 5.5V	–2.5	--	2.5	μA
Power−Off Leakage Current of L and R	I_{OFF}	L, R = 0V to 3V; DPR, DNL = Float Power off	–1	--	1	μA
AUD Switch On-Resistance	R_{ON}	ISW = 100mA, VSW = −3V to 3V V_{CC} : 2.7V to 5.5V	--	1	2	Ω
Pull-Down Resistor on R/L Pin when Audio Switch is Off	R_{SHUNT}	L = R = 3V V_{CC} : 2.7V to 5.5V	6	10	14	kΩ
USB Switch						
On Leakage Current of USB Switch	I_{ON}	DNL, DPR = 0V to 3.6V; DP, DN, R, L = Float V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Off Leakage Current of DP and DN	I_{OZ}	DN, DP = 0V to 3.6V V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Power−Off Leakage Current of DP and DN	I_{OFF}	DP, DN = 0V to 3.6V; Power off	–3	--	3	μA
USB Switch On-Resistance	R_{ON}	ISW = 8mA, VSW = 0.4V V_{CC} : 2.7V to 5.5V	--	3	5	Ω
SENSE Switch						
On Leakage Current of SENSE Switch	I_{ON}	GSBUx = 0V to 1V, SENSE is floating V_{CC} : 2.7V to 5.5V	–2	--	2	μA
Off Leakage Current of SENSE	I_{OZ}	SENSE = 0 V to 1V V_{CC} : 2.7V to 5.5V	–2	--	2	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Leakage Current of GSBUx	I_{OZ}	GSBUx = 0 V to 1V V_{CC} : 2.7V to 5.5V	–2	--	2	μA
		GSBUx = 1 V to 3.6V V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Power−Off Leakage Current of SENSE	I_{OFF}	SENSE = 0V to 1V; Power off	–2	--	2	μA
Power−Off Leakage Current of GSBUx	I_{OFF}	GSBUx = 0V to 3.6V; Power off	–3	--	3	μA
SENSE Switch On Resistance	R_{ON}	ISW = 100mA, VSW = 1V V_{CC} : 2.7V to 5.5V	--	300	600	mΩ
Input OVP Lockout on GSBUx	V_{OV_TRIP}	Rising edge V_{CC} : 2.7V to 5.5V	4.5	5	5.3	V
Input OVP Hysteresis of GSBUx	V_{OV_HYS}	V_{CC} : 2.7V to 5.5V	--	0.3	0.55	V
SBUX Pins						
Off Leakage Current of SBUx	I_{OZ}	SBUx = 0V to 3.6V V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Power−Off Leakage Current of SBUx	I_{OFF}	SBUx = 0 V to 3.6 V, Power off	–3	--	3	μA
Input OVP Lockout on SBUx	V_{OV_TRIP}	Rising edge V_{CC} : 2.7V to 5.5V	4.5	5	5.3	V
Input OVP Hysteresis of SBUx	V_{OV_HYS}	V_{CC} : 2.7V to 5.5V	--	0.3	0.55	V
MIC Switch						
On Leakage Current of MIC Switch	I_{ON}	SBUx = 0V to 3.6V, MIC = Float V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Off Leakage Current of MIC	I_{OZ}	MIC = 0V to 3.6V V_{CC} : 2.7V to 5.5V	–1	--	1	μA
Power−Off Leakage Current of MIC	I_{OFF}	MIC = 0V to 3.6V; Power off	–1	--	1	μA
MIC Switch On-Resistance	R_{ON}	ISW = 30mA, VSW = 3.6V V_{CC} : 2.7V to 5.5V	--	3	5	Ω
SBUX_H Switch						
On Leakage Current of SBUx_H Switch	I_{ON}	SBUx = 0V to 3.6V, SBUx_H = Float V_{CC} : 2.7V to 5.5V	–3	--	3	μA
Off Leakage Current of SBUx_H	I_{OZ}	SBUx_H = 0V to 3.6V V_{CC} : 2.7V to 5.5V	–1	--	1	μA
Power−Off Leakage Current of SBUx_H	I_{OFF}	SBUx_H = 0V to 3.6V; Power off	–1	--	1	μA
SBUx_H Switch On-Resistance	R_{ON}	ISW = 30mA, VSW = 3.6V V_{CC} : 2.7V to 5.5V	--	3	5	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AUDIO GROUND Switch : Pin : AGND to SBUX						
AGND Switch On-Resistance	R_{ON}	I_{SOURCE} = 100mA on SBUx, V_{CC} : 2.7V to 5.5V	--	50	90	mΩ
CC_IN Pin						
Input Low Threshold	V_{TH_L}	V_{CC} : 2.7V to 5.5V	1.03	1.2	1.37	V
Input High Threshold	V_{TH_H}	V_{CC} : 2.7V to 5.5V	1.35	1.5	1.65	V
Input Leakage of CC_IN	V_{TH_H}	CC_IN = 0V to 5.5V V_{CC} : 2.7V to 5.5V	--	--	1	μA
INT DET Pins						
Output High for DET	V_{OH}	I_O = –2mA V_{CC} : 2.7V to 5.5V	1.5	1.8	2	V
Output Low for DET and INT	V_{OL}	I_O = 2mA V_{CC} : 2.7V to 5.5V	--	--	0.4	V
Input High for INT	V_{IH}	V_{CC} : 2.7V to 5.5V	1.5	--	--	V
Input Low for INT	V_{IL}	V_{CC} : 2.7V to 5.5V	--	--	0.45	V
ADDR Pin						
Input voltage High	V_{IH}	V_{CC} : 2.7V to 5.5V	1.3	--	--	V
Input voltage Low	V_{IL}	V_{CC} : 2.7V to 5.5V	--	--	0.45	V
Control Input Leakage	V_{TH_H}	ADDR = 0V to V_{CC} V_{CC} : 2.7V to 5.5V	–1	--	1	μA
ENN Pin						
Input voltage High	V_{IH}	V_{CC} : 2.7V to 5.5V	1.3	--	--	V
Input voltage Low	V_{IL}	V_{CC} : 2.7V to 5.5V	--	--	0.45	V
Internal Pull Down Resistor	R_{PD}	V_{CC} : 2.7V to 5.5V	300	470	630	kΩ
SDA, SCL Pins						
Low−Level Input Voltage	V_{ILI2C}	V_{CC} : 2.7V to 5.5V	--	--	0.4	V
High-Level Input Voltage	V_{IHI2C}	V_{CC} : 2.7V to 5.5V	1.2	--	--	V
Input Current of SDA and SCL Pins	I_{I2C}	SCL/SDA = 0 V to 3.6V V_{CC} : 2.7V to 5.5V	–2	--	2	μA
Low−Level Output Voltage	V_{OLSDA}	I_{OL} = 2mA	--	--	0.3	V
Low−Level Output Current	I_{OLSDA}	V_{OLSDA} = 0.2V	10	--	--	mA
I^2C Work Voltage	V_{I2C}		--	1.8	--	V
I^2C CLK Frequency	f_{SCL}		--	--	400	kHz
I^2C Data Hold Time	t_{DH_I2C}		--	--	900	ns
I^2C Data Set-Up Time	t_{DS_I2C}		100	--	--	ns

AC Electrical Characteristics

(V_{CC} = 2.7V to 5.5V, V_{CC} (Typ.) = 3.3V, T_A = −40°C to 85°C and T_A (Typ.) = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AUDIO Switch						
Audio Switch Turn On Delay Time	t_{DELAY_AUD}	DPR = DNL = 1V, R_L = 32Ω, V_{CC} = 3.3V	--	75	--	μs
		DPR = DNL = 1V, R_L = 32Ω, V_{CC} = 3.3V (Note 5)	--	60	--	
Audio Switch Turn On Rising Time	t_{RISE_AUD}	DPR = DNL = 1V, R_L = 32Ω, V_{CC} = 3.3V (Note 6)	--	200	--	μs
Audio Switch Turn Off Time	t_{OFF_AUD}	DPR = DNL = 1V, R_L = 32Ω, V_{CC} = 3.3V	--	2.5	5	μs
Cross Talk (Adjacent)	X_{TALK}	f = 1kHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$	--	−100	--	dB
−3dB Bandwidth	BW	R_L = 50Ω	--	600	--	MHz
Off Isolation	O_{IRR}	f = 1kHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$	--	−100	--	dB
Total Harmonic Distortion + Noise Performance with A−weighting Filter	THD+N	R_L = 600Ω, f = 20Hz to 20kHz, V_{SW} = $2V_{RMS}$	--	−110	--	dB
		R_L = 32Ω, f = 20Hz to 20kHz, V_{SW} = $1V_{RMS}$	--	−110	--	dB
		R_L = 16Ω, f = 20Hz to 20kHz, V_{SW} = $0.5V_{RMS}$	--	−110	--	dB
USB Switch						
USB Switch Turn−On Time	t_{ON_USB}	DPR = DNL = 1.5V, R_L = 50Ω, V_{CC} = 3.3V	--	45	--	μs
		DPR = DNL = 1.5V, R_L = 50Ω, V_{CC} = 3.3V (Note 5)	--	45	--	
USB Switch Turn−Off Time	t_{OFF_USB}	DPR = DNL = 1.5V, R_L = 50Ω, V_{CC} = 3.3V	--	3.7	7	μs
Single Ended −3dB Bandwidth	BW	R_L = 50Ω, V_{CC} = 3.3V	--	850	--	MHz
Differential −3dB Bandwidth			--	850	--	
Off Isolation	O_{IRR}	f = 1kHz, R_L = 50Ω, V_{SW} = 1 V_{RMS}, V_{CC} = 3.3V	--	−100	--	dB
DPR and DNL Pins OVP Response Time	t_{OVP}	V_{SW} = 3.5V to 5.5V, V_{CC} = 3.3V	--	0.5	1	μs
MIC/AUDIO Ground Switch						
MIC Switch Turn-On Delay Time	t_{DELAY_MIC}	SBUx= 1V, R_L = 50Ω, V_{CC} = 3.3V	--	70	--	μs
		SBUx= 1V, R_L = 50Ω, V_{CC} = 3.3V (Note 5)	--	65	--	
MIC Switch Turn-On Rising Time	t_{RISE_MIC}	SBUx= 1V, R_L = 50Ω, V_{CC} = 3.3V (Note 6)	--	250	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AGND Switch Turn-On Delay Time	t_{DELAY_AGND}	SBUx pulled up to 0.5V by 16Ω, AGND connect to GND V_{CC} = 3.3V	--	40	--	µs
		SBUx pulled up to 0.5V by 16Ω, AGND connect to GND V_{CC} = 3.3V (Note 5)	--	30	--	
AGND Switch Turn-On Rising Time	t_{RISE_AGND}	SBUx pulled up to 0.5 V by 16Ω, AGND connect to GND V_{CC} = 3.3V (Note 6)	--	700	--	µs
MIC Switch Turn-Off Time	t_{OFF_MIC}	SBUx = 2.5 V, R_L = 50Ω, V_{CC} = 3.3V	--	3	6	µs
AGND Switch Turn-Off Time	$t_{OFF\_AUDIO GND}$	SBUx : Isource = 10mA, clamp to 2.5V	--	3	6	µs
−3dB Bandwidth	BW	R_L = 50Ω, V_{CC} = 3.3V	--	50	--	MHz
SBUx_H Switch						
SBUx_H Switch Turn-On Time	$t_{ON\_SBUx\_H}$	SBUx = 2.5V, R_L = 50Ω, V_{CC} = 3.3V	--	95	--	µs
		SBUx = 2.5V, R_L = 50Ω, V_{CC} = 3.3V (Note 5)	--	3	--	
SBUx_H Switch Turn-Off Time	$t_{OFF\_SBUx\_H}$	SBUx = 2.5V, R_L = 50Ω, V_{CC} = 3.3V	--	3	6	µs
−3dB Bandwidth	BW	R_L = 50Ω, V_{CC} = 3.3V	--	50	--	MHz
SBUx Pins OVP Response Time	t_{OVP}	V_{SW} = 3.5V to 5.5V, V_{CC} = 3.3V	--	0.5	1	µs
SENSE Switch						
SENSE Switch Turn-On Delay Time	t_{ON_SENSE}	GSBUx = 1V, R_L = 50Ω, V_{CC} = 3.3V	--	110	--	µs
		GSBUx = 1V, R_L = 50Ω, V_{CC} = 3.3V (Note 5)	--	110	--	
SENSE Switch Turn-On Rising Time	t_{RISE_SENSE}	GSBUx = 1V, R_L = 50Ω, V_{CC} = 3.3V (Note 6)	--	160	--	µs
SENSE Switch Turn-Off Time	t_{OFF_SENSE}	GSBUx = 1 V, R_L = 50Ω, V_{CC} = 3.3V	--	4	8	µs
−3dB Bandwidth	BW	R_L = 50Ω, V_{CC} = 3.3V	--	150	--	MHz
GSBUx Pins OVP Response Time	t_{OVP}	V_{SW} = 3.5V to 5.5V, V_{CC} = 3.3V	--	0.75	1.5	µs
DET Delay						
DET Response Delay	t_{DELAY_DET}	Transition from 0V to 1.8V, V_{CC} = 3.3V	--	6	7	µs
		Transition from 1.8V to 0V, V_{CC} = 3.3V	--	6	7	µs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. If any switch enable, turn on and turn on delay time will enable faster.

Note 6. Turn-on rising timing can be controlled by I^2C register.

Typical Application Circuit

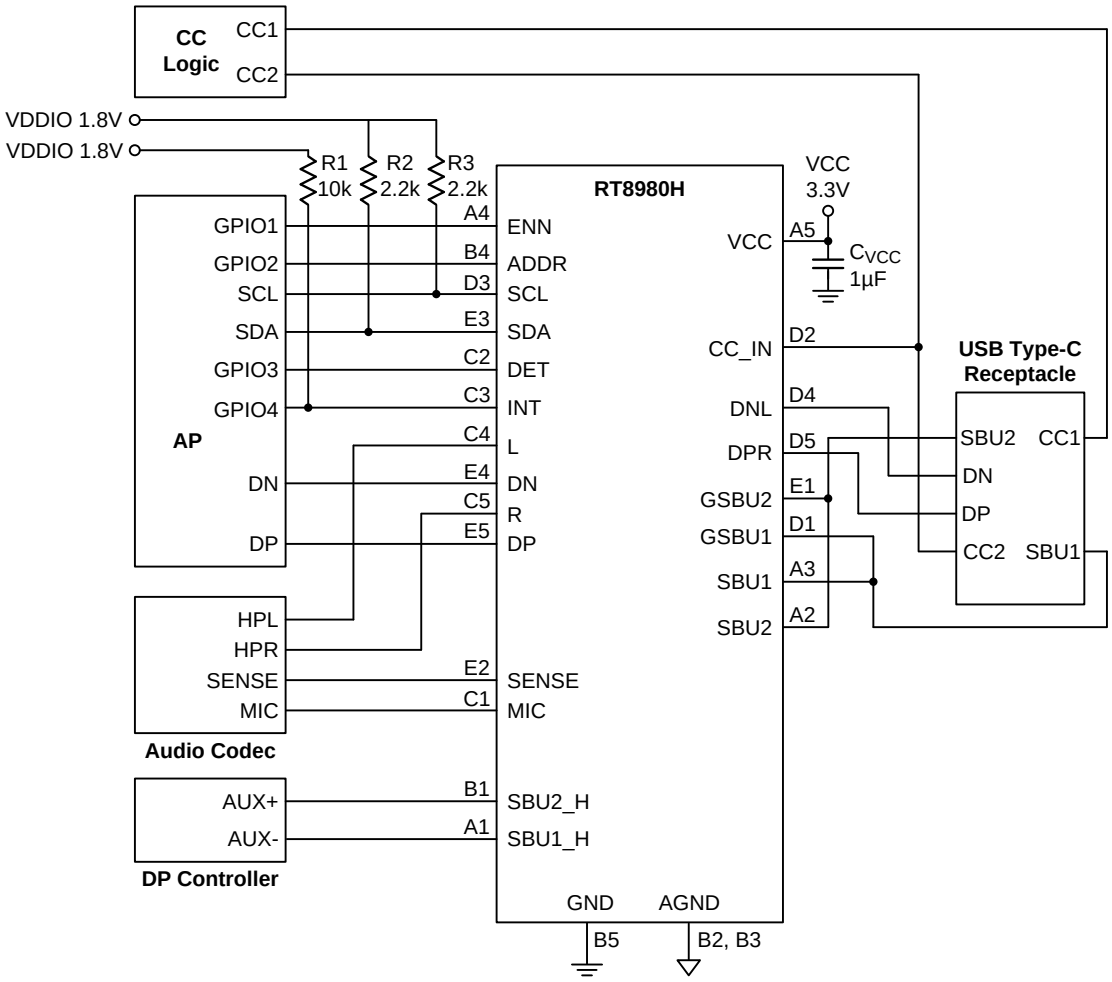
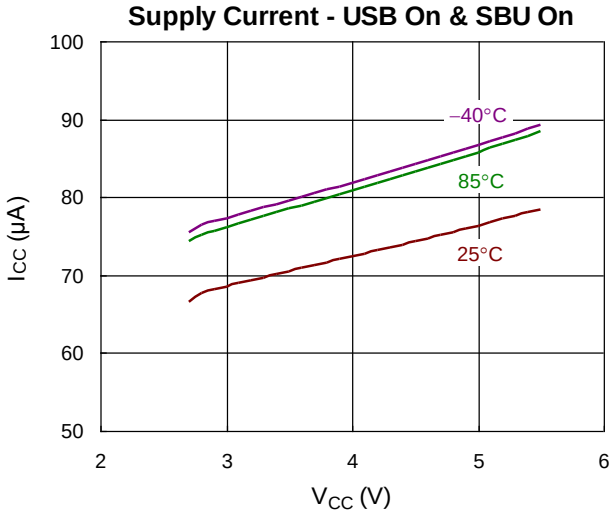
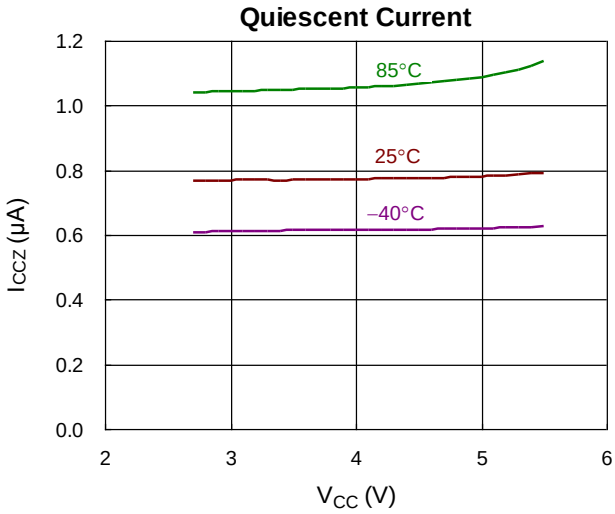


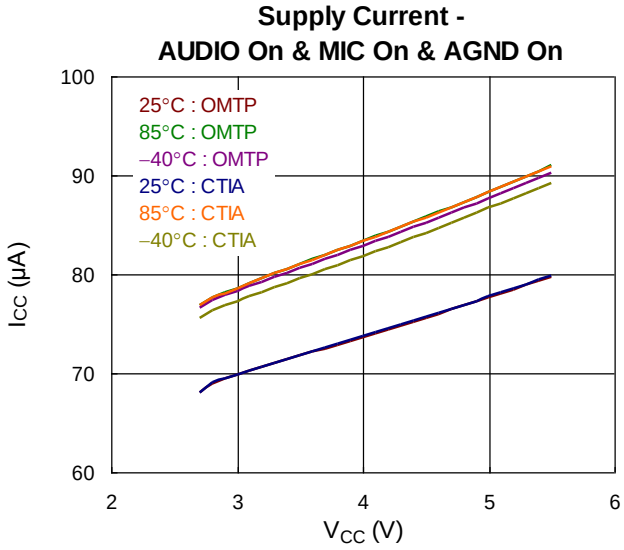
Table 1. Recommended Components Information

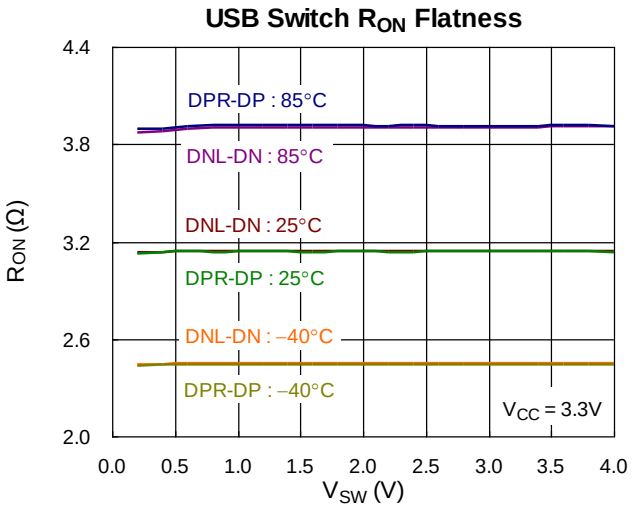
Reference	Q'ty	Part Number	Description	Package	Manufacturer
C_{VCC}	1	TMK107BJ105KA-T	1µF/X5R/25V	0603	TAIYO YUDEN
R1	1	WR06X1002FTL	10k	0603	WALSIN
R2, R3	2	WR06X2201FTL	2.2k	0603	WALSIN

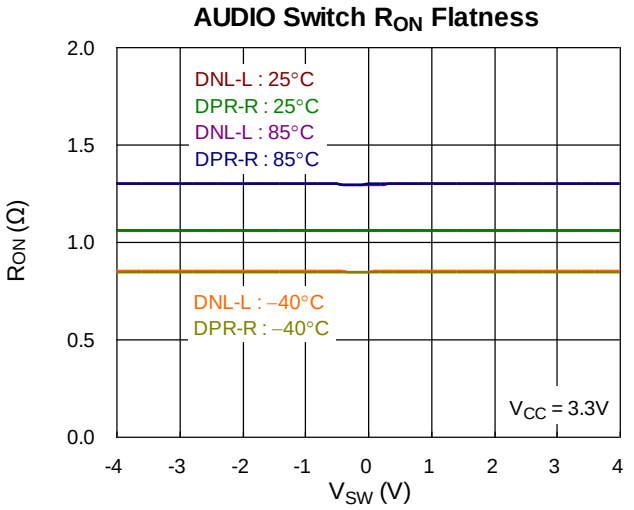
Typical Operating Characteristics

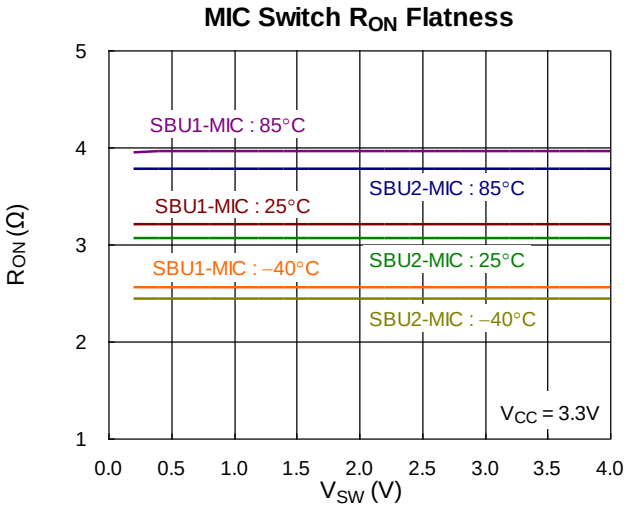


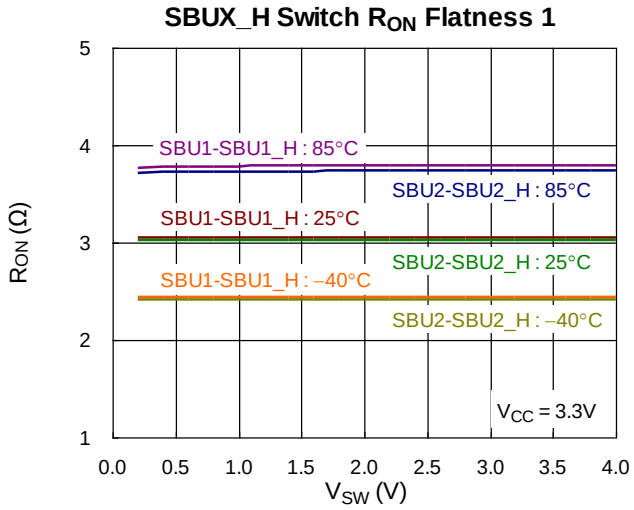


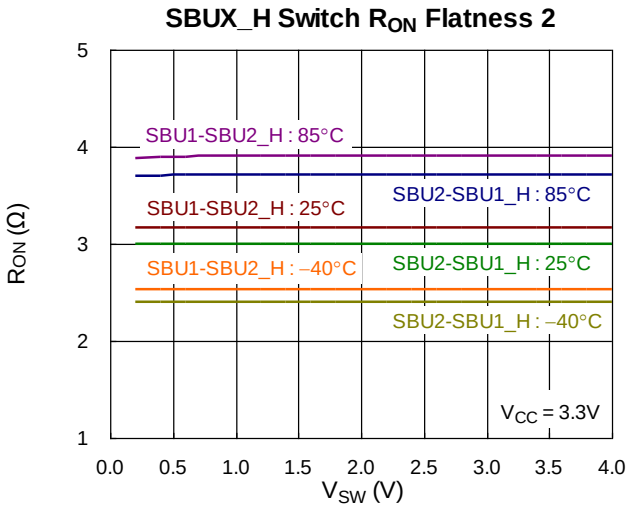


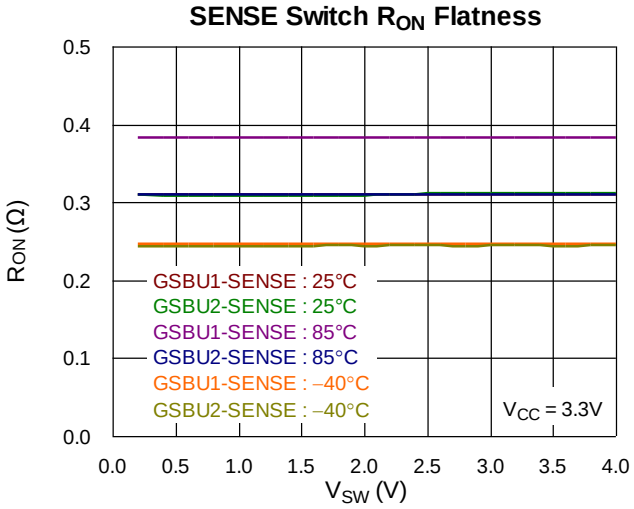












Application Information

Over−Voltage Protection

The RT8980H provides over-voltage protection (OVP) on Type-C receptacle side pins (DPR, DNL, SBU1, SBU2, GSBU1 and GSBU2). When the input voltage exceeds the OVP threshold, switch will be turned off until OVP event release. If OVP event occurs, the device will send interrupt by INT signal and OVP-status will provide information about which pin has OVP event.

Headset Detection

The RT8980H detects the CC_IN voltage, and monitors headset jack to see if the Type-C plug is inserted. The headset detection function is always active when the RT8980H is enabled. The DET will be low when CC_IN > 1.5V. When CC_IN < 1.2V, the DET will be rise to high.

	Device Disable	Device Enable
CC_IN < VTH_L = 1.2V	DET = 0	DET = 1
CC_IN > VTH_H = 1.5V	DET = 0	DET = 0

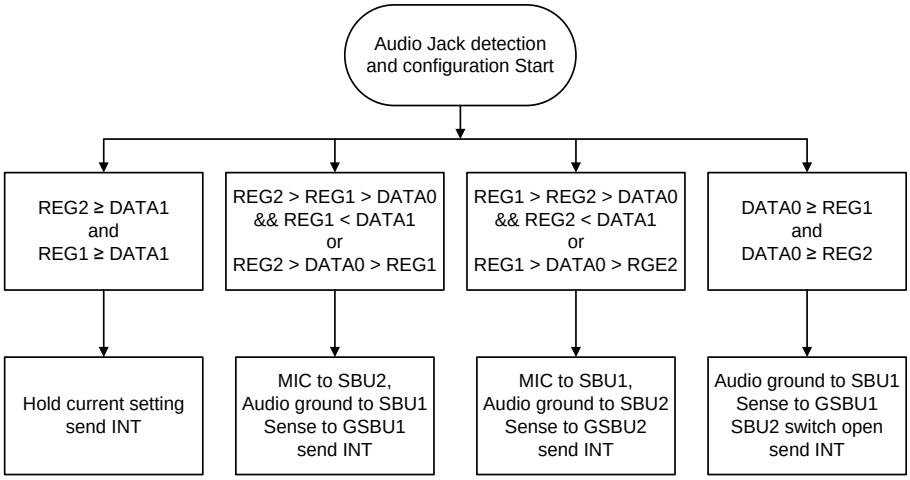
MIC Switch Auto−Off Function

The MIC auto-off function is active when R, L, Audio ground switches are under on status, CC_IN > 1.5V and control enable bit 0x12[2] = 1. The MIC switch will be turned off and receptacle side pin (SBU1/2) will be shorted to ground for 50μs first. Then it shows high−Z status when MIC switch is set to on status.

Audio Ground Detection and Configuration

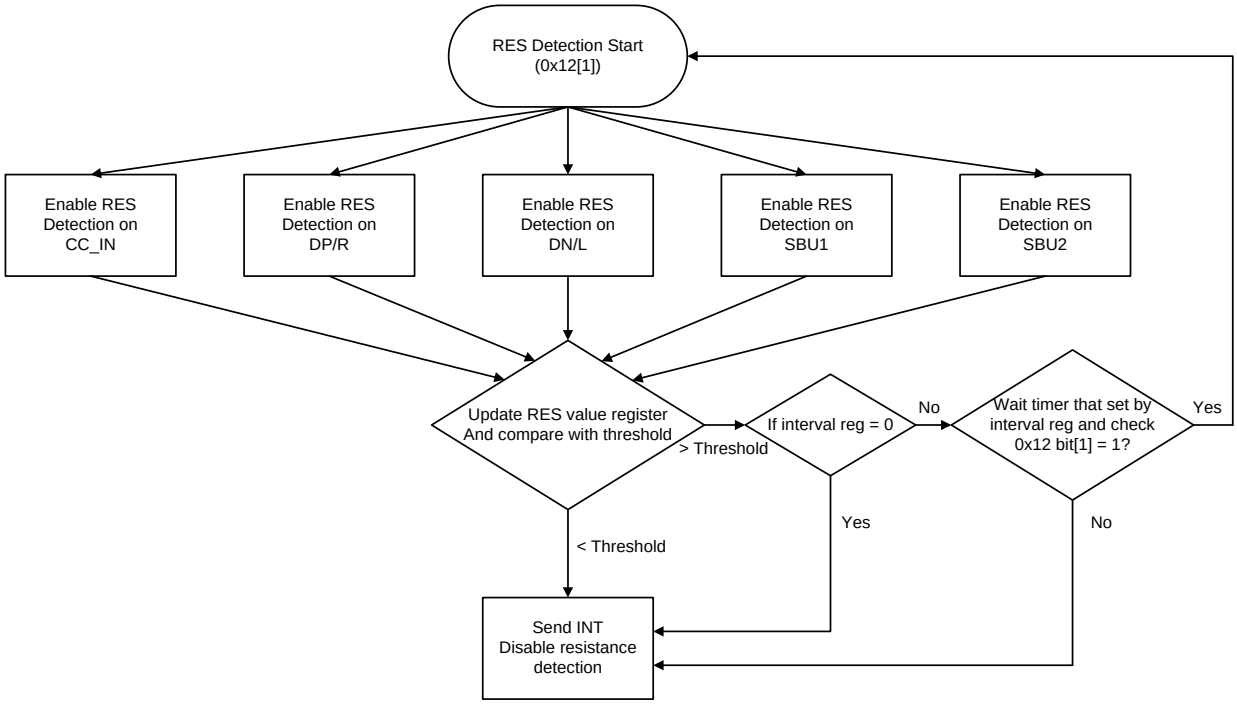
This function is active when control enable bit 0x12[0] = 1 and R, L, AGND switches are turned on. For Type−C interface analog headset, the audio ground can be the SBU1 pin or the SBU2 pin. This function automatically detects two different configurations for headsets with microphones. Users can adjust current source setting by 0x1F to optimize configuration.

During detection and configuration, the R, L, MIC, Sense and Audio ground switches will be turned off. When device detection and configuration is done, R, L, MIC, Sense and Audio ground switch will turn on according to detection results and timing control setting.



Resistance Detection

Resistance Detection function is active when control enable bit 0x12[1] = 1. It will detect foreign object between receptacle side pins and ground. During RES detection, the switch which is monitored will be turned off. It will detect for 1.2ms and the ADC sample time is 0.7ms. The total RES detection timing is 1.9ms. The detection result will be saved in the 0x14h resistance flag register. The CC_IN, SBU1 and SBU2 measurement can be from 1kΩ to 2.32MΩ, and the DPR and DNL measurement can be from 1kΩ to 1.7MΩ which is controlled by internal register. The cycling detection (100ms, 1s or 10s) can be set by register 0x16h.



Manual Switch Control

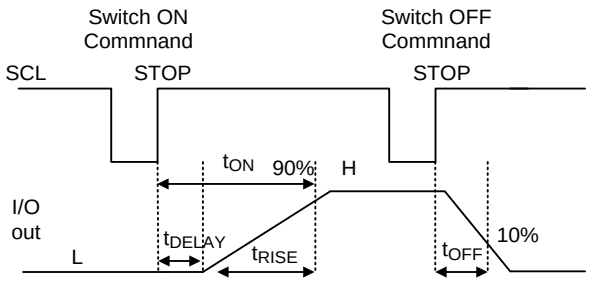
Manual Switch function is active when control enable bit 0x12[4] = 1 and switch setting enable bit 0x04h = FF. During this setup, the ADDR and INT pins will be set as logic control input. It will provide manual mode control for device.

Table 2. Manual Mode Table

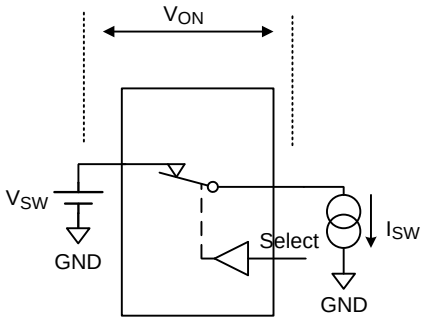
Power	ENN	ADDR	INT	USB Switch	SBU bypass Switch	Audio Switch	MIC Switch	Audio Ground Switch	Sense Switch	Headset Detection
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	ON DPR to DP DNL to DN	ON : SBU1 to SBU1_H SBU2 to SBU2_H	OFF	OFF	OFF	OFF	OFF
ON	L	0	1	ON DPR to DP DNL to DN	ON : SBU1 to SBU2_H SBU2 to SBU1_H	OFF	OFF	OFF	OFF	OFF
ON	L	1	0	OFF	OFF	ON : DPR to R DNL to L	ON : SBU1 to MIC	ON : SBU2 to Audio GND	ON : GSBU2 to SESNE	ON
ON	L	1	1	OFF	OFF	ON : DPR to R DNL to L	ON : SBU2 to MIC	ON : SBU1 to Audio GND	ON : GSBU1 to SESNE	ON

Test Diagrams

1. Turn On/Off Waveforms

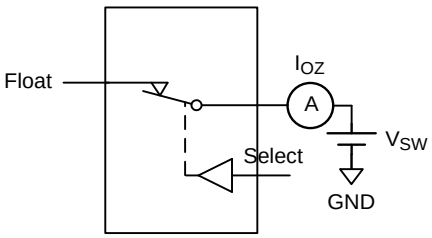


2. Switch On-Resistance



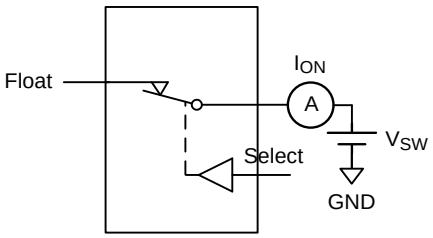
$R_{ON} = V_{ON} / I_{SW}$

3. Switch-Off Leakage (I_{OZ}) (Each switch is tested separately)



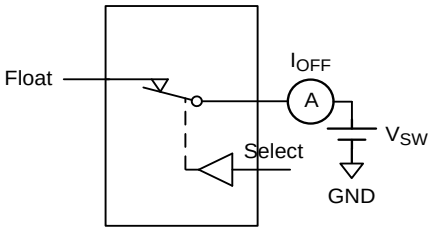
V_{SEL} = 0 or V_{CC}

4. Switch-On Leakage (I_{ON}) (Each switch is tested separately)



V_{SEL} = 0 or V_{CC}

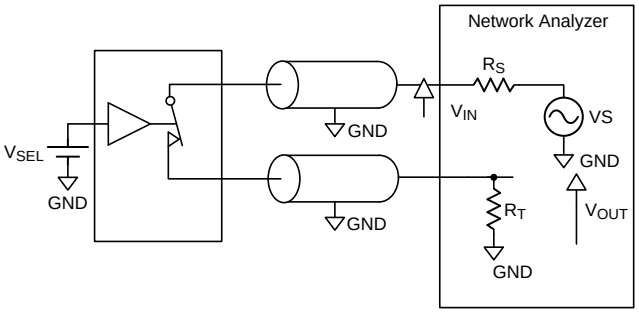
5. Power-Off Leakage (I_{OFF}) (Each switch is tested separately)



V_{CC} = 0V

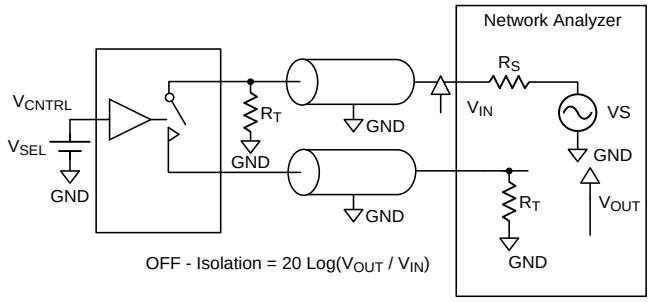
6. Bandwidth

R_S and R_T are function of application environment (see AC/DC Tables).



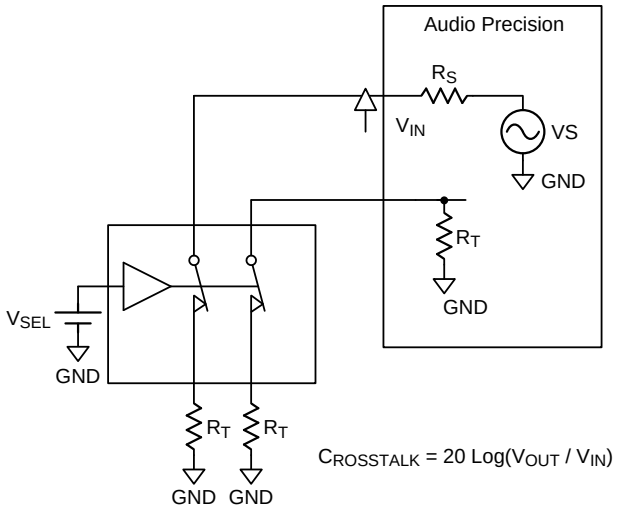
7. Channel Off Isolation

   R_S and R_T are function of application environment (see AC/DC Tables).



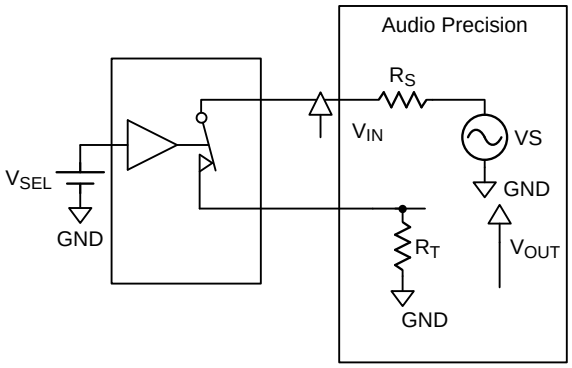
8. Adjacent Channel $C_{ROSSTALK}$

   RS and RT are function of application environment (see AC/DC Tables).



9. Total Harmonic Distortion (THD + N)

   R_S and R_T are function of application environment (see AC/DC Tables).



I²C Interface

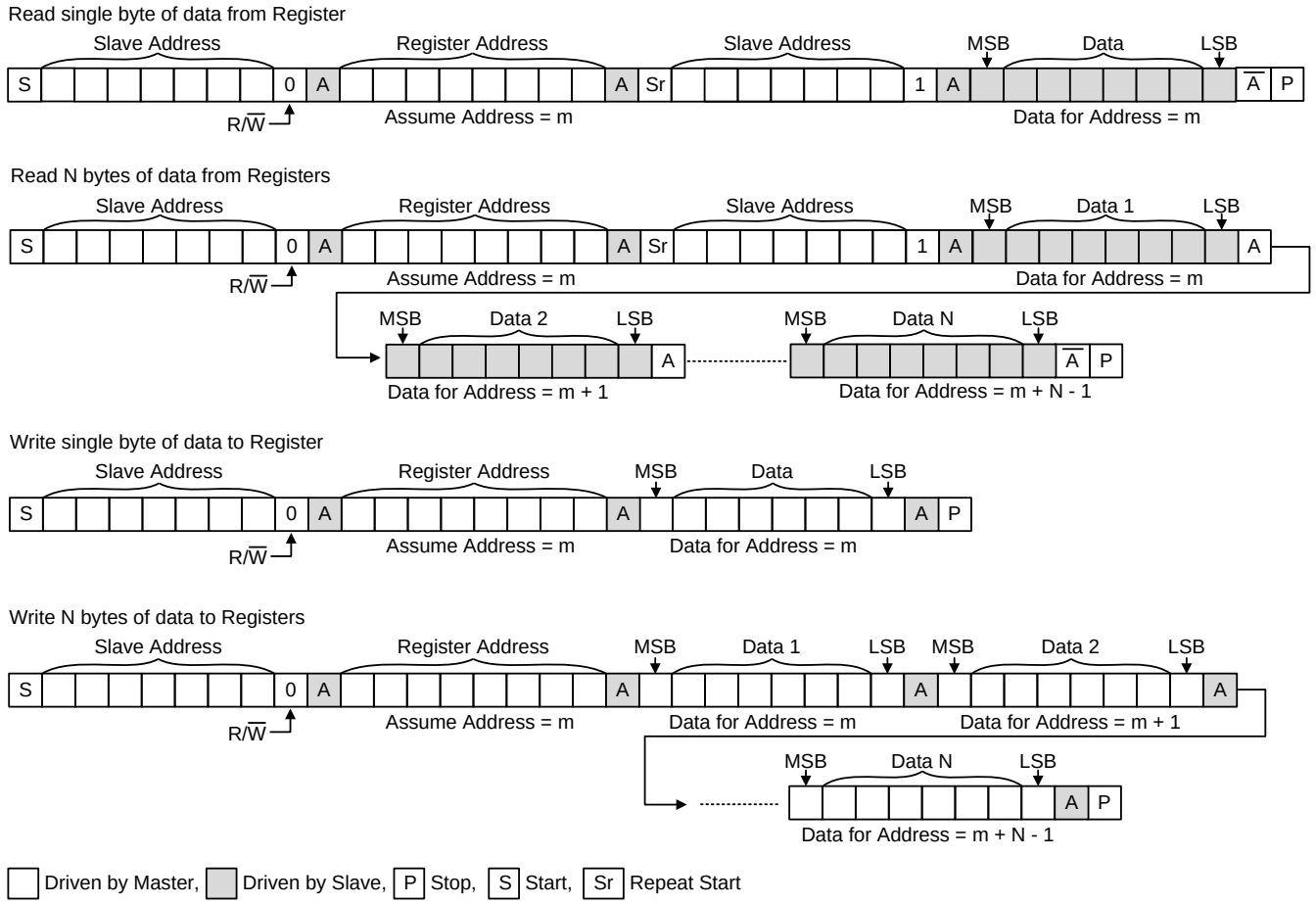
The following table shows the RT8980H unique address as below.

Table 3. The RT8980H Unique AddressRT8980H I²C Slave Address

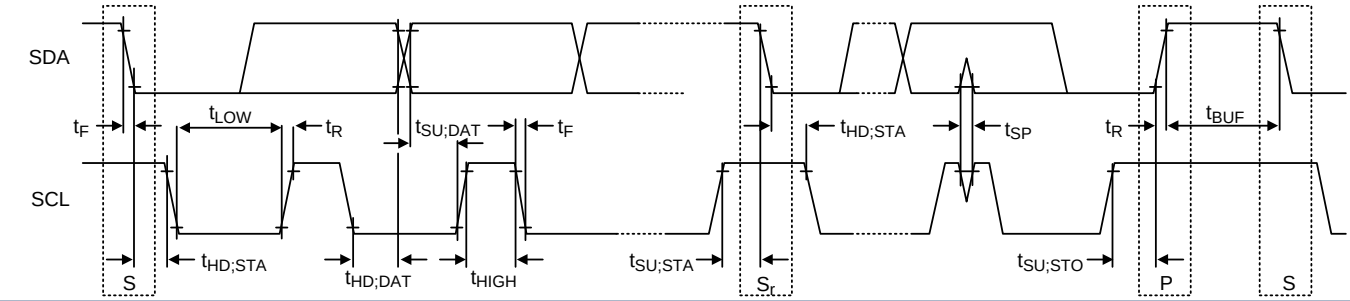
ADDR	MSB	LSB	R/W bit	R/W
ADDR = L	100001	0	1/0	85/84
ADDR = H	100001	1	1/0	87/86

The I²C interface bus must be connected to a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.

- **Read and Write Function**



- **I²C Waveform Information**



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-23B 2.21x2.25 (BSC) package, the thermal resistance, θ_{JA}, is 30.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (150°C - 25°C) / (30.9°C/W) = 4.04W for a WL-CSP-23B 2.21x2.25 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

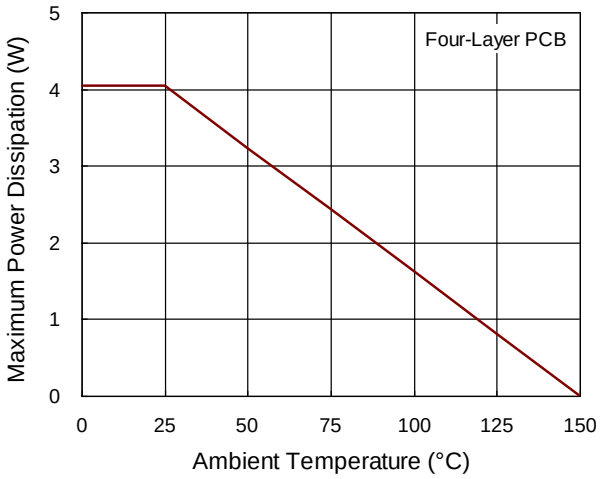


Figure 1. Derating Curve of Maximum Power Dissipation

I²C Register Table

R : Read only.

RC : Read then Clear.

RW : Read and Wirte.

WC : Write “1” then clear to “0” after this procedure finish.

Register Maps

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x00	1	DEVICE ID	7:6	Vendor ID	11	R	Vendor ID
			5:3	Version ID	010	R	Device version ID
			2:0	Revision ID	110	R	Revision history ID
0x01	1	OVP INTERRUPT MASK	7	Reserved	0	R	Do not use
			6	OVP Interrupt mask control	0	R/W	OVP interrupt function enable/disable 0 : Controlled by [5:0] bit (default) 1 : Mask all connector side pins OVP interrupt
			5	DPR OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt
			4	DNL OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt
			3	SBU1 OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt
			2	SBU2 OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt
			1	GSBU1 OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt
			0	GSBU2 OVP Interrupt mask control	0	R/W	0 : Do not mask OVP interrupt (default) 1 : Mask OVP interrupt

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x02	1	OVP INTERRUPT FLAG	7:6	Reserved	00	R	Do not use
			5	DPR OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			4	DNL OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			3	SBU1 OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			2	SBU2 OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			1	GSBU1 OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			0	GSBU2 OVP	0	RC	0 : OVP event has not occurred (default) 1 : OVP event has occurred
0x03	1	OVP STATUS	7:6	Reserved	00	R	Do not use
			5	ST_OVP_DPR	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			4	ST_OVP_DNL	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			3	ST_OVP_SBU1	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			2	ST_OVP_SBU2	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			1	ST_OVP_GSBU1	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred
			0	ST_OVP_GSBU2	0	R	0 : OVP event has not occurred (default) 1 : OVP event has occurred

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x04	1	SWITCHING SETTING ENABLE	7	DEVICE_ENABLE	1	RW	0 : Device disable; L, R pull down by 10k and other switch nodes will be high−Z for positive input. 1 : Device enable. (default) ----------Device enable = 1 Device enable = 0 ENN = 1 Device disable Device Disable ENN = 0 Device enable Device disable
			6	SW_SBU1_H_SBUX	0	RW	0 : Switch disable; SBU1_H will be high−Z for positive input (default) 1 : Switch enable
			5	SW_SBU2_H_SBUX	0	RW	0 : Switch disable; SBU2_H will be high−Z for positive input (default) 1 : Switch enable
			4	SW_DNL	1	RW	0 : Switch disable; DNL,DN will be high−Z for positive input. L pull down by 10kΩ 1 : Switch enable (default)
			3	SW_DPR	1	RW	0 : Switch disable; DPR, DP will be high−Z for positive input. R pull down by 10kΩ 1 : Switch enable (default)
			2	SW_SENSE_GSBUX	0	RW	0 : Switch disable; Sense,GSBU1 and GSBU2 will be high−Z for positive input (default) 1 : Switch enable
			1	SW_MIC_SBUX	0	RW	0 : Switch disable : MIC will be high−Z for positive input. (default) 1 : Switch enable
			0	SW_AGND_SBUX	0	RW	0 : Switch disable : AGND will be high−Z for positive input. (default) 1 : Switch enable

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x05	1	SWITCH SELECT	7	Reserved	0	R	Do not use
			6	SEL_SBU1_H_SBUX	0	RW	0 : SBU1_H to SBU1 switch on (default) 1 : SBU1_H to SBU2 switch on
			5	SEL_SBU2_H_SBUX	0	RW	0 : SBU2_H to SBU2 switch on (default) 1 : SBU2_H to SBU1 switch on
			4	SEL_DNL	1	RW	0 : DNL to L switch on 1 : DNL to DN switch on (default)
			3	SEL_DPR	1	RW	0 : DPR to R switch on 1 : DPR to DP switch on (default)
			2	SEL_SENSE_GSBUX	0	RW	0 : Sense to GSBU1 switch on (default) 1 : Sense to GSBU2 switch on
			1	SEL_MIC_SBUX	0	RW	0 : MIC to SBU2 switch on (default) 1 : MIC to SBU1 switch on
			0	SEL_AGND_SBUX	0	RW	0 : AGND to SBU1 switch on (default) 1 : AGND to SBU2 switch on
0x06	1	SWITCH STATUS0	7:6	Reserved	00	R	Do not use
			5:4	ST_SENSE_SWITCH	00	R	00 : Sense switch is open/not connected (default) 01 : Sense connected to GSBU1 10 : Sense connected to GSBU2 11 : Not valid
			3:2	ST_DPR_SWITCH	00	R	00 : DPR switch open/not connected (default) 01 : DPR connected to DP 10 : DPR connected to R 11 : Not valid
			1:0	ST_DNL_SWITCH	00	R	00 : DNL switch open/not connected (default) 01 : DNL connected to DN 10 : DNL connected to L 11 : Not valid

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x07	1	SWITCH STATUS1	7:6	Reserved	00	R	Do not use
			5:3	ST_SBU2_SWITCH	000	R	000 : SBU2 switch is open/not connected (default) 001 : SBU2 connected to MIC 010 : SBU2 connected to AGND 011 : SBU2 connected to SBU1_H 100 : SBU2 connected to SBU2_H 101 : SBU2 connected both SBU1_H and SBU2_H 110…111 : Do not use
			2:0	ST_SBU1_SWITCH	000	R	000 : SBU1 switch is open/not connected (default) 001 : SBU1 connected to MIC 010 : SBU1 connected to AGND 011 : SBU1 connected to SBU1_H 100 : SBU1 connected to SBU2_H 101 : SBU1 connected both SBU1_H and SBU2_H 110…111 : Do not use
0x08	1	LEFT SLOW TURN−ON	7:0	L_SLOW_ON_TIME	00000001	RW	00000000 : 100μs 00000001 : 200μs (default) ... 11111111 : 25600μs
0x09	1	RIGHT SLOW TURN-ON	7:0	R_SLOW_ON_TIME	00000001	RW	00000000 : 100μs 00000001 : 200μs (default) ... 11111111 : 25600μs
0x0A	1	MIC SLOW TURN-ON	7:0	MIC_SLOW_ON_ TIME	00000001	RW	00000000 : 150μs 00000001 : 250μs (default) 00000010 : 350μs ... 11111111 : 25650μs

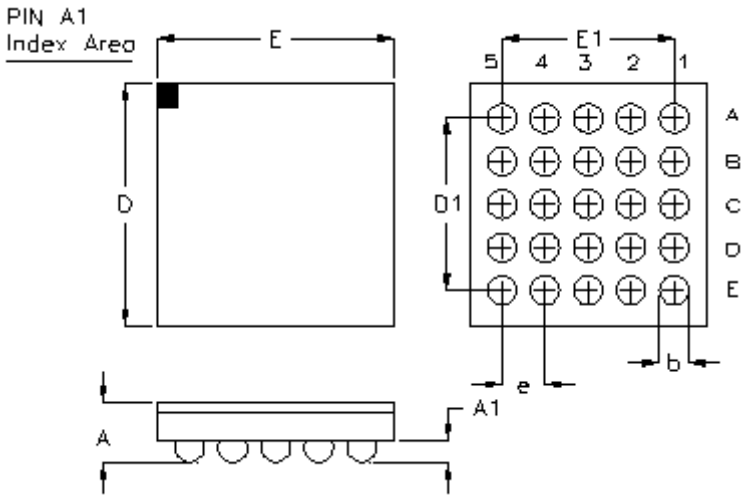
Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x0B	1	SENSE SLOW TURN-ON	7:0	SENSE_SLOW_ON_TIME	00000001	RW	00000000 : 100μs 00000001 : 200μs (default) ... 11111111 : 25600μs
0x0C	1	AGND SLOW TURN-ON	7:0	AGND_SLOW_ON_TIME	00000001	RW	00000000 : 700μs 00000001 : 1400μs (default) ... 11111111 : 179200μs
0x0D	1	TIMING DELAY BETWEEN R SWITCH ENABLE AND L SWITCH ENABLE	7:6	R_L_DELAY_TIME	00000000	RW	00000000 : 0μs (default) 00000001 : 100μs ... 11111110 : 25400μs 11111111 : 25500μs
0x0E	1	TIMING DELAY BETWEEN MIC SWITCH ENABLE AND L SWITCH ENABLE	7:0	MIC_L_DELAY_TIME	00000000	RW	00000000 : 0μs (default) 00000001 : 100μs ... 11111110 : 25400μs 11111111 : 25500μs
0x0F	1	TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE	7:0	SENSE_L_DELAY_TIME	00000000	RW	00000000 : 0μs (default) 00000001 : 100μs ... 11111110 : 25400μs 11111111 : 25500μs
0x10	1	TIMING DELAY BETWEEN AUDIO GROUND SWITCH ENABLE AND L SWITCH ENABLE	7:0	AGND_L_DELAY_TIME	00000000	RW	00000000 : 0μs (default) 00000001 : 100μs ... 11111110 : 25400μs 11111111 : 25500μs
0x11	1	AUDIO ACCESSORY STATUS	7:2	Reserved	000000	R	Do not use
			1	ST_CC_IN	1	R	0 : CC_IN < 1.2V 1 : CC_IN > 1.5V (default)
			0	ST_DET	0	R	0 : DET output is low .(default) 1 : DET is output is high.

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x12	1	FUNCTION ENABLE	7	Reserved	0	R	Do not use
			6	DET_IO_EN	0	RW	0 : DET pin is in Push/Pull Configuration (default) 1 : DET pin is in Open/Drain Configuration
			5	RES_DET_SET	0	RW	0 : 1k to 256k (default) 1: 6.5k / 9k to 1.7M / 2.3M
			4	GPIO_CTRL_EN	0	RW	0 : Disable (default) 1 : Enable
			3	SLOW_ON_CTRL_EN	1	RW	0 : Disable 1 : Enable (default)
			2	MIC_AUTO_OFF_EN	0	RW	0 : Disable (default) 1 : Enable
			1	RES_DET_EN	0	RW	0 : Disable (default) 1 : Enable; will be changed to ‘0’ after low resistance detection.
			0	AUD_JACK_DET_EN	0	RW	0 : Disable (default) 1 : Enable; will be changed to ‘0’ after audio jack detection and configuration.
0x13	1	RES DETECTION PIN SETTING	7:3	Reserved	00000	R	Do not use
			2:0	PIN_SEL	000	RW	000 : CC_IN (default) 001 : DPR 010 : DNL 011 : SBU1 100 : SBU2 101 : Reserved 110 : Reserved 111 : Reserved
0x14	1	RES VALUE	7:0	RES_DET_VALUE	11111111	R	00000000 : R < 1k / 6.5k / 9k … 11111111 : R > 256k / 1.7M / 2.32M (default)
0x15	1	RES DETECTION THRESHOLD	7:0	RES_DET_THD	00010110	RW	Selection by 1k per step if Reg 12h [5] = 0 Selection by 6.5k / 9k per step if Reg 12h [5] = 1 Default Value = 22k (default) 00000000 : 1k / 6.5k / 9k … 11111111 : 256k / 1.7M / 2.32M

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x16	1	RES DETECTION INTERVAL	7:2	Reserved	000000	R	Do not use
			1:0	RES_DET_INTERVAL	00	RW	RES detection interval 00 : Single (default) 01 : 100ms 10 : 1s 11 : 10s
0x17	1	AUDIO JACK STATUS	7:4	Reserved	0000	R	Do not use
			3	POLE4_SBU1_AGND	0	R	0 : Others (default) 1 : 4 pole SBU2 to MIC, SBU1 to audio ground
			2	POLE4_SBU2_AGND	0	R	0 : Others (default) 1 : 4 pole SBU1 to MIC, SBU2 to audio ground
			1	POLE3	0	R	0 : Others (default) 1 : 3 pole
			0	NO_AUDIO_ACC	1	R	0 : Audio accessory attached 1 : No audio accessory (default)
0x18	1	RES DETECTION / AUDIO JACK DETECTION INTERRUPT FLAG	7:3	Reserved	00000	R	Do not use
			2	INT_AUTO_JACK_DET	0	RC	0 : Audio jack detection and configuration has not occurred. (default) 1 : Audio jack detection and configuration has occurred.
			1	INT_RES_DET_LOW	0	RC	0 : Low resistance has not occurred. (default) 1 : Low resistance has occurred.
			0	INT_RES_DET_DONE	0	RC	0 : Low resistance has not occurred. (default) 1 : Low resistance has occurred.

Address	Length	RegName	Bit	Bit Name	Default	Type	Description
0x19	1	RES DETECTION / AUDIO JACK DETECTION INTERRUPT MASK	7:3	Reserved	00000	R	Do not use
			2	M_AUTO_JACK_DET	0	RW	0 : Do not mask Audio jack detection and configuration has occurred (default) 1: Mask Audio jack detection and configuration has occurred.
			1	M_RES_DET_LOW	0	RW	0 : Do not mask Low resistance has occurred. (default) 1 : Mask Low resistance has occurred.
			0	M_RES_DET_DONE	0	RW	0 : Do not mask Low resistance detection has occurred. (default) 1 : Mask Low resistance detection has occurred.
0x1A	1	AUDIO JACK DETECTION REG1 VALUE	7:0	AUTO_JACK_DET_REG1	11111111	R	Resistance between SBU1 to SBU2 10mV per step
0x1B	1	AUDIO JACK DETECTION REG2 VALUE	7:0	AUTO_JACK_DET_REG2	11111111	R	Resistance between SBU2 to SBU1 10mV per step
0x1C	1	MIC DETECTION THRESHOLD DATA0	7:0	AUTO_JACK_DET_DATA0	00100000	RW	MIC detection threshold DATA0 Selection by 10mV per step 00100000 : 320mV (default)
0x1D	1	MIC DETECTION THRESHOLD DATA1	7:0	AUTO_JACK_DET_DATA1	11111111	RW	MIC detection threshold DATA1 Selection by 10mV per step 11111111 : 2.5V (default)
0x1E	1	I2C RESET	7:1	Reserved	0000000	R	Do not use
			0	I2C_RESET	0	W	0 : Default (default) 1 : I^2C reset
0x1F	1	CURRENT SOURCE SETTING	7:4	Reserved	0000	R	Do not use
			3:0	AUTO_JACK_DET_SET	0111	RW	0000 : Invalid 0001 : 100μA ... 0111 : 700μA (default) ... 1111 : 1500μA

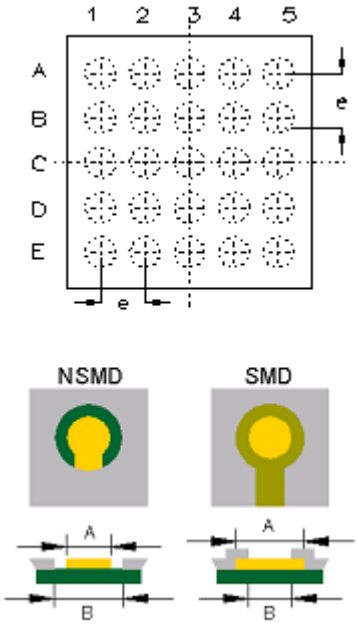
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.210	2.290	0.087	0.090
D1	1.600		0.063	
E	2.170	2.250	0.085	0.089
E1	1.600		0.063	
e	0.400		0.016	

25B WL-CSP 2.21x2.25 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.21x2.25-25(BSC)	25	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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