MAAP-010168

10 W Power Amplifier
0.5 - 3 GHz

Rev. V4

Features

- Saturated Output Power: 41 dBm
- Linear Gain: 24 dB
- Power Added Efficiency: 30% at P_{SAT}
- 50 Ω Input / Output Match
- Ceramic Flange Mount Package
- RoHS* Compliant and 260°C Re-flow Compatible

Description

The MAAP-010168 is a two stage MMIC power amplifier designed for broadband high power applications. It can be used as either a driver or an output stage amplifier. This device is fully matched input and output to 50 Ω which eliminates any sensitive external RF tuning components.

The device is packaged in a lead free 10-lead flanged hermetic package for high volume manufacturing.

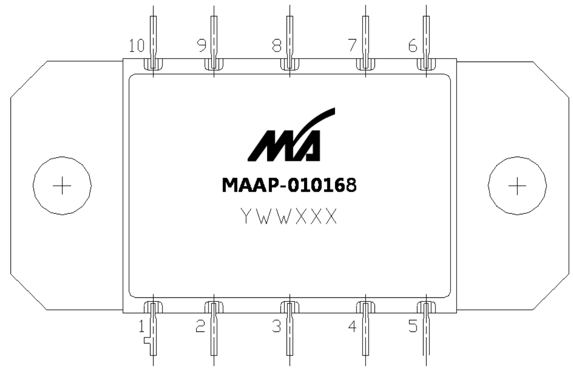
The MAAP-010168 is fabricated using a fully passivated high reliability pHEMT process. The device provides excellent power added efficiency and gain.

Ordering Information[1]

Part Number	Package
MAAP-010168-000000	Bulk
MAAP-010168-001SMB	Sample Board

1. Reference Application Note M567 for package handling and mounting procedure.

Functional Schematic



Pin Configuration[2]

Pin #	Function
1	V_{GG}2
2	V_{GG}1
3	RF Input[3]
4	V_{GG}1
5	V_{GG}2
6	V_{DD}1
7	V_{DD}2
8	RF Output[3]
9	V_{DD}2
10	V_{DD}1

2. Flange is DC and RF ground.
3. RF Input & RF Output ports have shunt DC paths to ground. No External DC voltage should be applied to the RF ports.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 0.5 - 3.0 GHz, V_{DD} = 10 V, I_{DQ} = 3.5 A, T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Small signal	dB	19	24	—
Input Return Loss	—	dB	—	10	—
Output Return Loss	—	dB	—	10	—
P1dB	—	dBm	—	39	—
P_{SAT}	—	dBm	38	41	—
Current	I_{DQ} P_{SAT}	A	—	3.5 5.5	—
PAE	P_{SAT}	%	—	30	—
Gate Bias	—	V	—	-0.7	—
Duty Cycle	—	%	—	—	100

Absolute Maximum Ratings[4,5]

Parameter	Absolute Maximum
Input Power	24 dBm
Operating Supply Voltage	+11 V
Operating Gate Voltage	-2 V
Operating Temperature	-40°C to +85°C
Channel Temperature[6,7]	+150°C
Storage Temperature	-65°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θ_{JC}) = 2.0°C/W
   a) For T_C = 25°C @ 1.5 GHz
   T_J = +80°C @ +10 V, 4 A, P_{OUT} = 41 dBm, P_{IN} = 21 dBm
   b) For T_C = 85°C @ 1.5 GHz
   T_J = +138°C @ +10 V, 3.9 A, P_{OUT} = 41 dBm, P_{IN} = 21 dBm

Operating the MAAP-010168

The MAAP-010168 is static sensitive. Please handle with care. To operate the device, follow these steps. Ramp down or shutdown in reverse order (gate bias on first and off last). All V_{GG} pins should have the same voltage applied at all times.

1. Apply V_{GG} (-1.5 V).
2. Apply V_{DD} (10.0 V Typical).
3. Set I_{DQ} by adjusting V_{GG}.
4. Apply RF_{IN}.

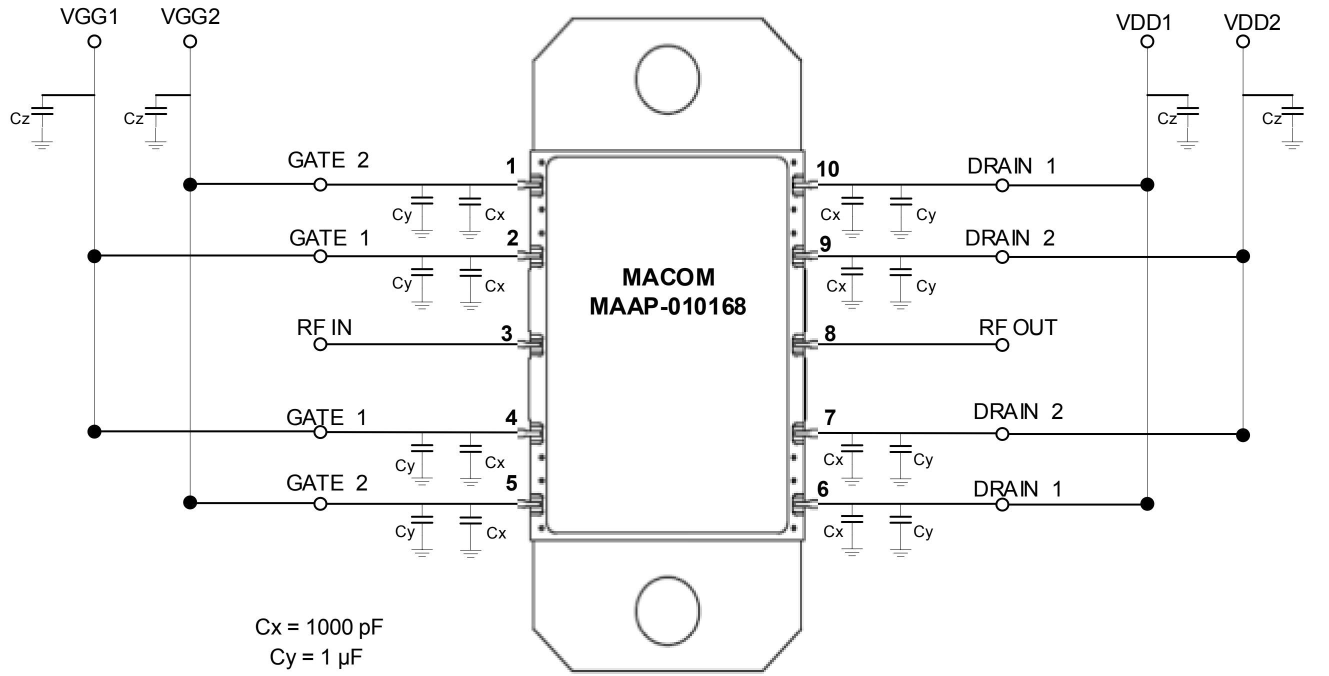
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

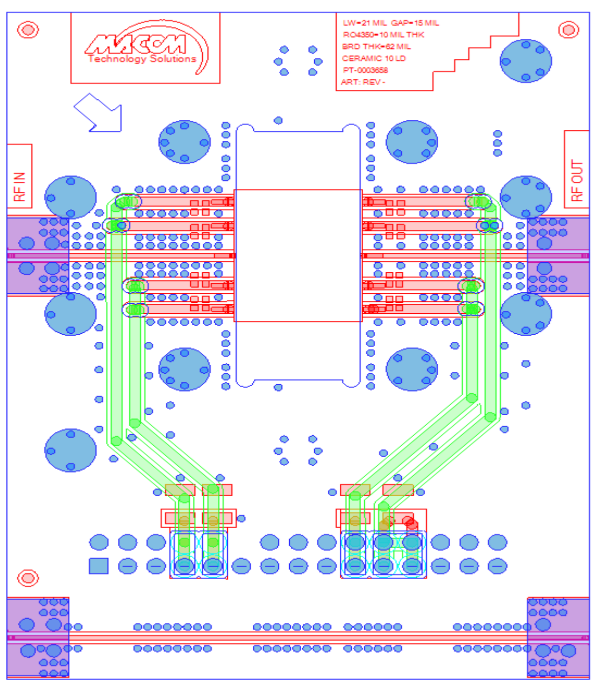
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Recommended Bias Configuration



Cx = 1000 pF
Cy = 1 µF
Cz = 10 µF

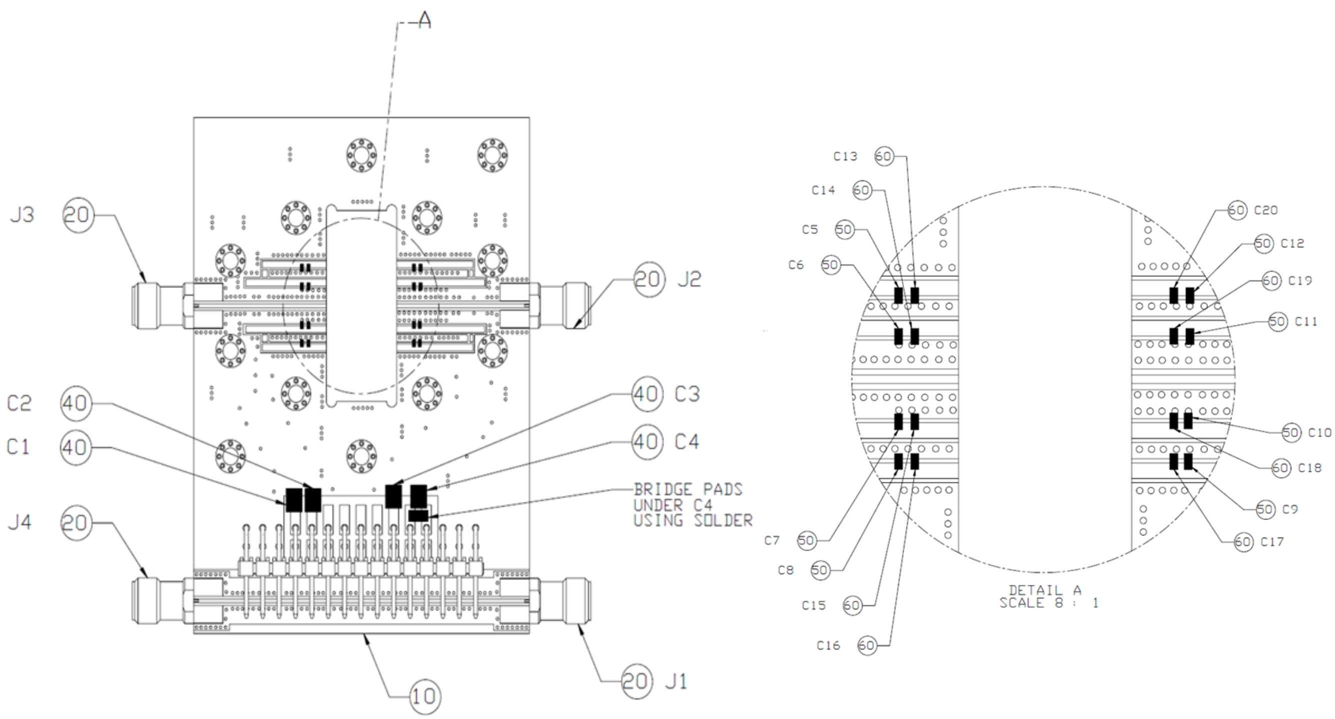
Sample Board Layout



MAAP-010168 Recommended Layout

Below is the recommended layout for the MAAP-010168. For optimal stability MACOM recommends adding bias decoupling capacitors of 10 µF at the entry point of V_G and V_{DD} (At the DC connections Header PIN). It is also recommended to add shunt decoupling capacitors of 1 µF & 1000 pF at the gate and drain pins of MAAP-010168 as shown in the details A below.
MACOM can provide gerber files of the sample board layout upon request.

MAAP-010168 Sample Board Layout

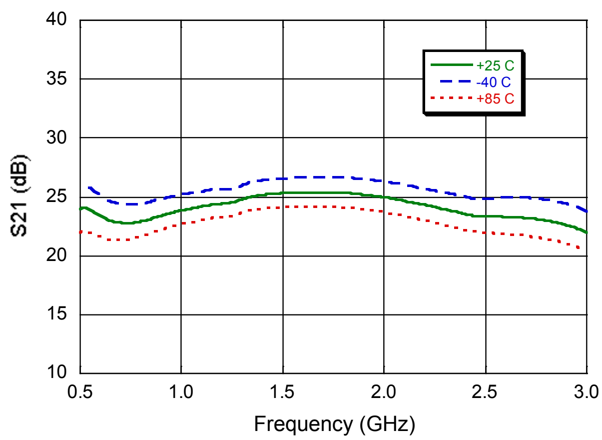


Parts List

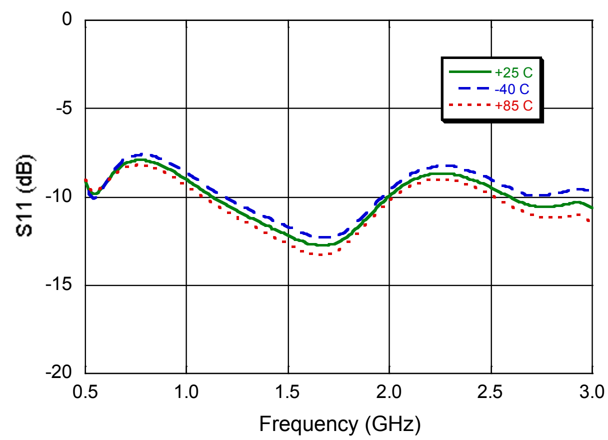
Item #	Component / Description
10	Test Board, RO4350 , ½ Oz copper , 10 mil thick
20	SMA Edge Mount Connectors
30	2x15 Right Angle Connector, 0.1 Grid
40	Capacitor, 10 µF, 10%, 16 V, 1210, X5R
50	Capacitor, 1 µF, 10%, 16 V, 0402, X5R
60	Capacitor, 1000 pF, 10 %, 25 V, 0402, X5R

Typical Performance Curves

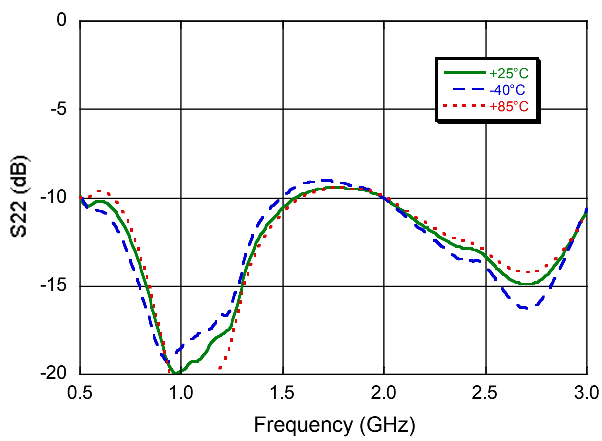
Gain



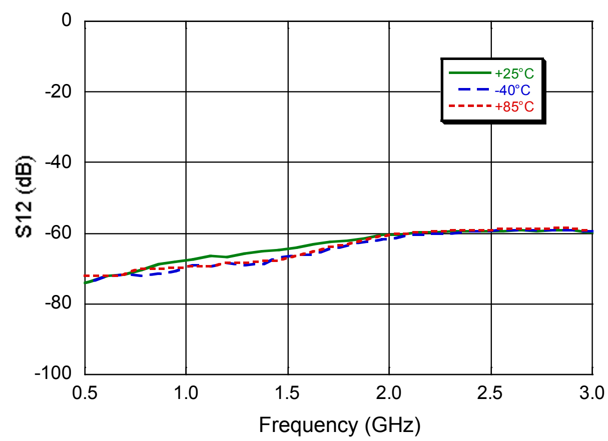
Input Return Loss



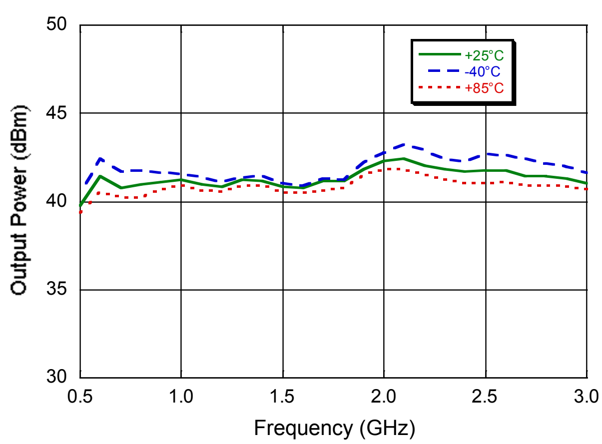
Output Return Loss



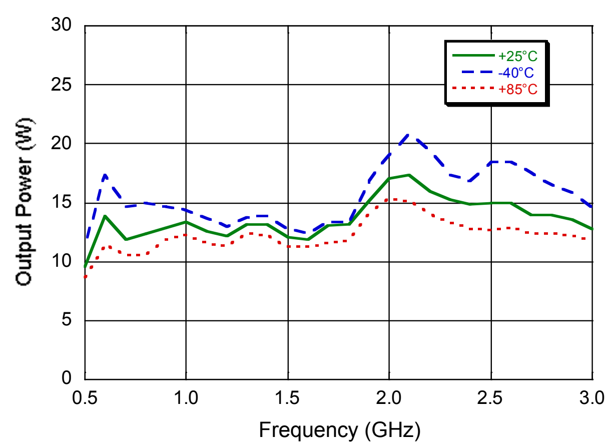
Reverse Isolation



Output Power (dBm)

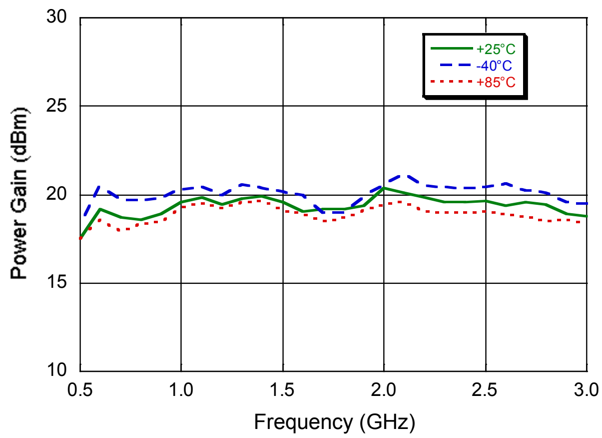


Output Power (W)

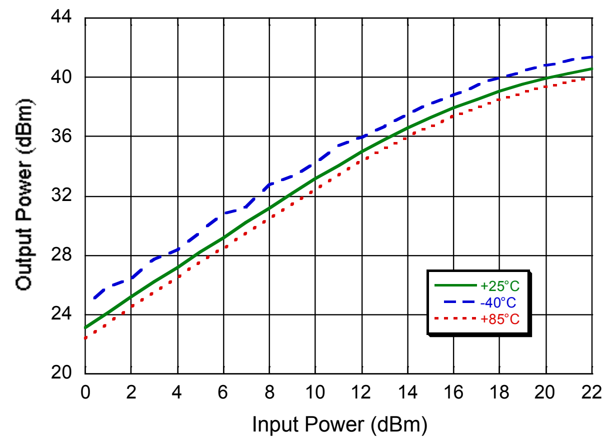


Typical Performance Curves

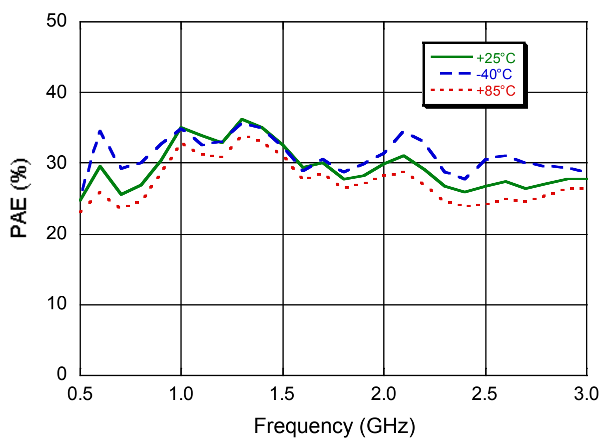
Power Gain



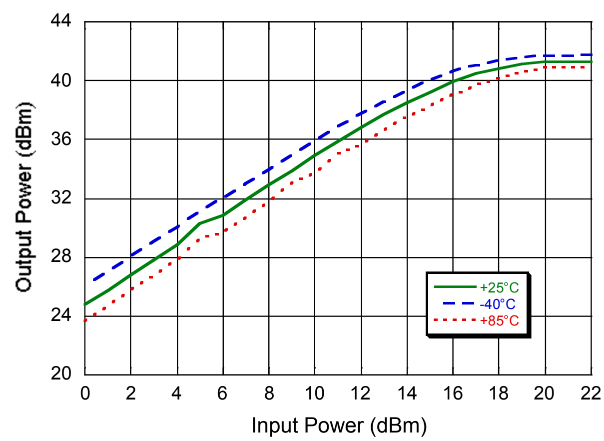
Output Power Sweep @ 0.7 GHz



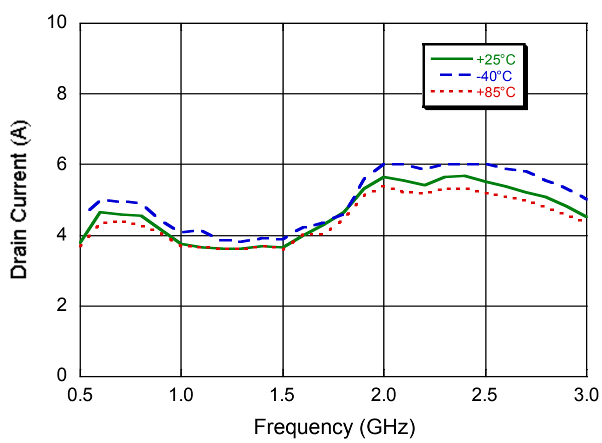
Power Added Efficiency



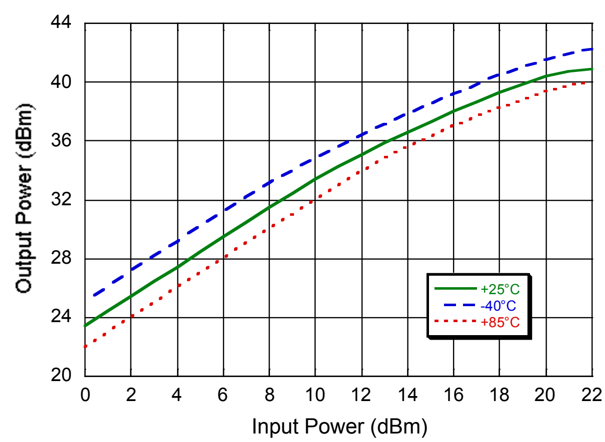
Output Power Sweep @ 1.5 GHz



Drain Current

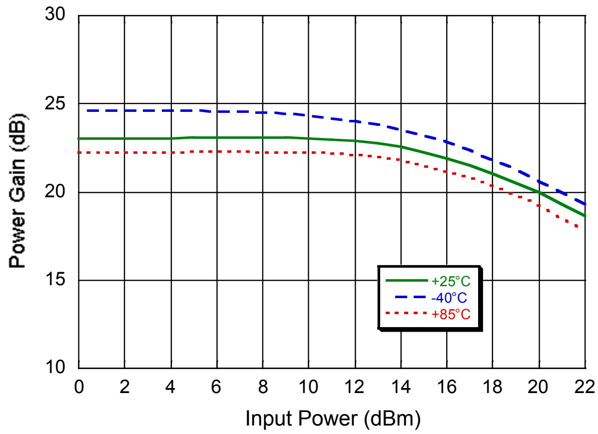


Output Power Sweep @ 2.5 GHz

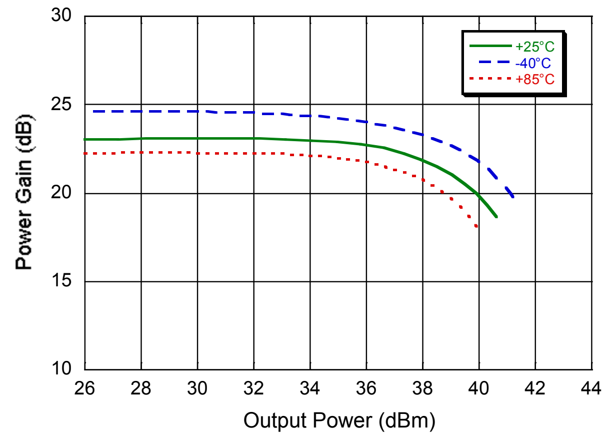


Typical Performance Curves

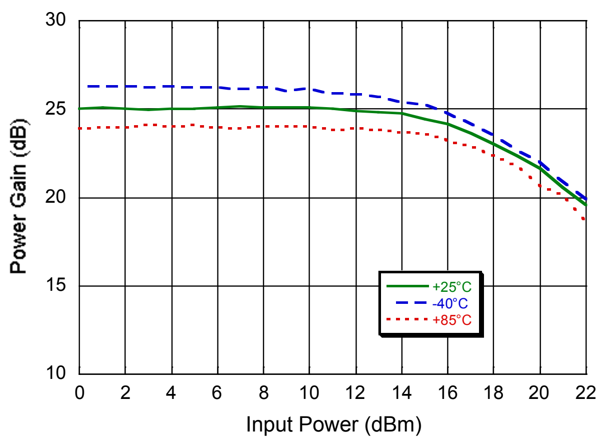
Power Gain vs. Input Power @ 0.7 GHz



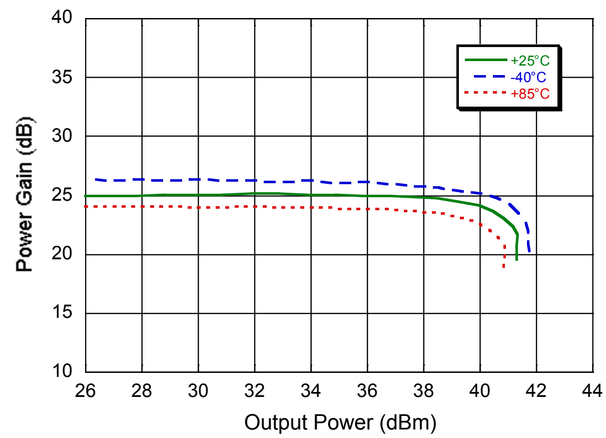
Power Gain vs. Output Power @ 0.7 GHz



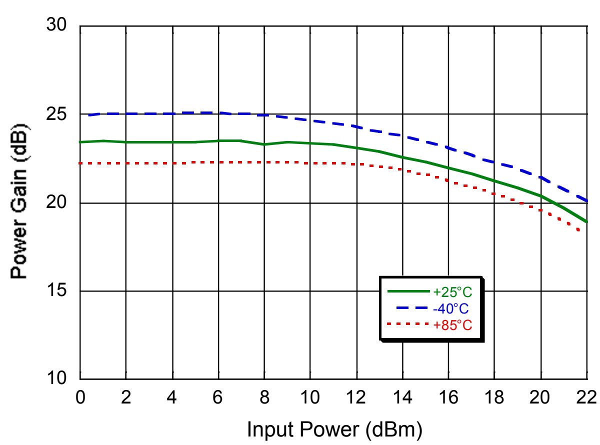
Power Gain vs. Input Power @ 1.5 GHz



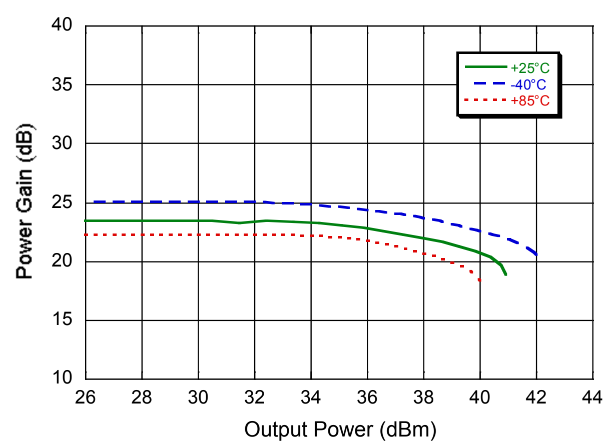
Power Gain vs. Output Power @ 1.5 GHz



Power Gain vs. Input Power @ 2.5 GHz

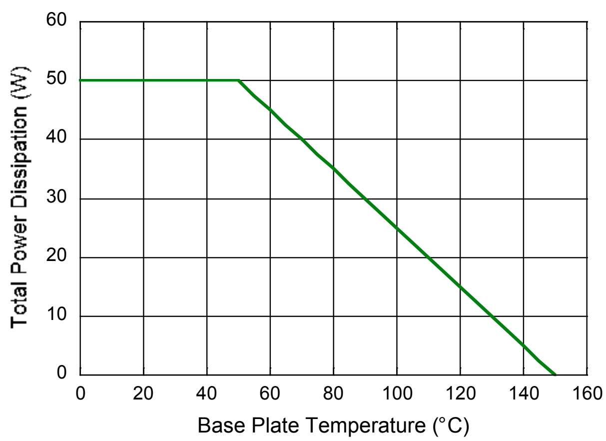


Power Gain vs. Output Power @ 2.5 GHz



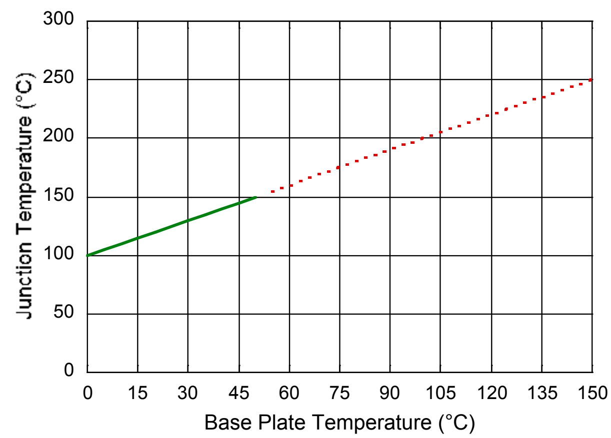
Typical Performance Curves

Max. Power Dissipation vs. Base Plate Temperature[7]

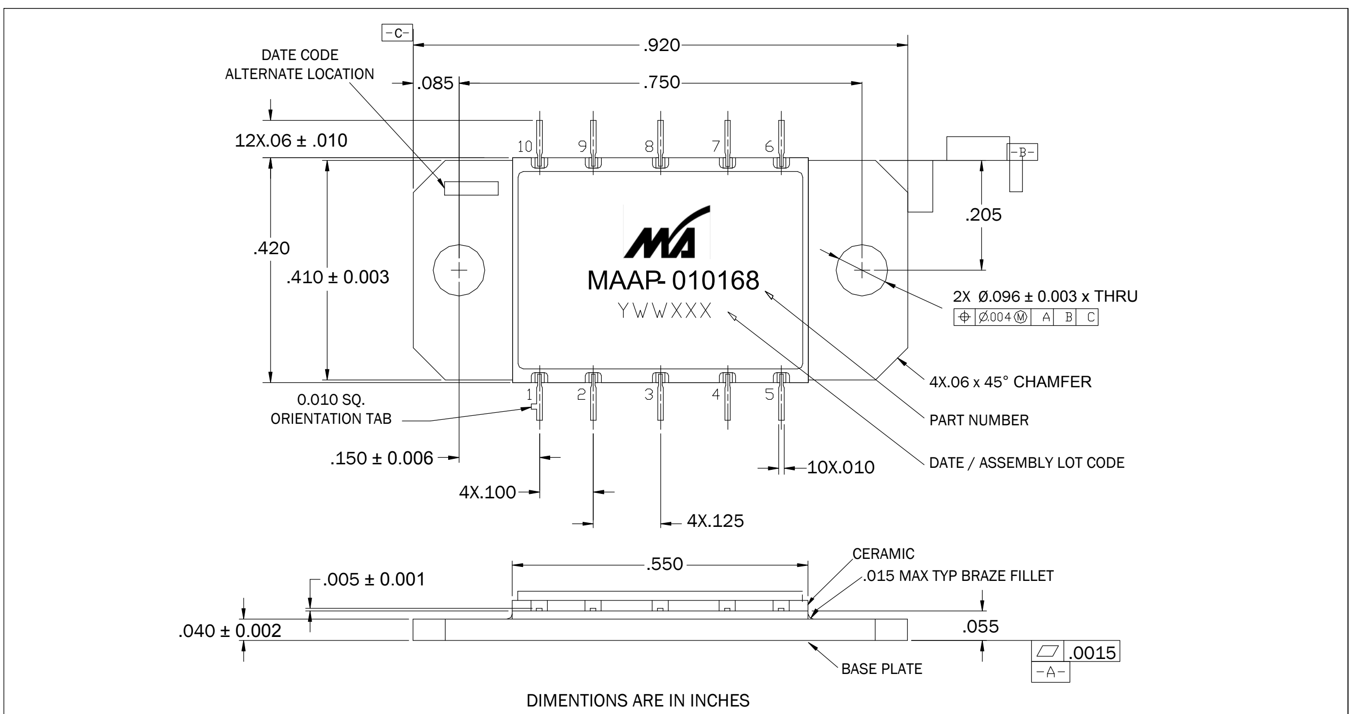


8. Power dissipation should not exceed the maximum plot shown above to maintain T_J <150°C. It is recommended to monitor power dissipation and decrease power dissipation in the device as required.

Junction Temperature vs. Base Plate Temperature with 50 W Power Dissipation



Ceramic Flange Mount Package†



† Reference Application Note M538 for lead-free solder reflow recommendations.
This is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.