



Isolated Fixed Ratio DC-DC Converter

Features & Benefits

- 48V_{DC} – 8V_{DC} 240W Bus Converter
- High efficiency (>95%) reduces system power consumption
- High power density (>817W/in³) reduces power system footprint by >40%
- Contains built-in protection features:
 - Undervoltage
 - Overvoltage Lockout
 - Overcurrent Protection
 - Short circuit Protection
 - Overtemperature Protection
- Provides enable/disable control, internal temperature monitoring
- Can be paralleled to create multi-kW arrays

Typical Applications

- High-End Computing Systems
- Automated Test Equipment
- High-Density Power Supplies
- Communications Systems

Product Ratings	
$V_{IN} = 48V (38 - 55V)$	$P_{OUT} = \text{up to } 240W$
$V_{OUT} = 8V (6.3 - 9.2V)$ (NO LOAD)	$K = 1/6$

Product Description

The VI Chip[®] bus converter is a high efficiency (>95%) Sine Amplitude Converter™ (SACT™) operating from a 38 to 55V_{DC} primary bus to deliver an isolated, ratiometric output voltage from 6.3 to 9.2V_{DC}. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the transformation ratio of the BCM48Bx080y240A00 is 1/6, the capacitance value can be reduced by a factor of 36x, resulting in savings of board area, materials and total system cost.

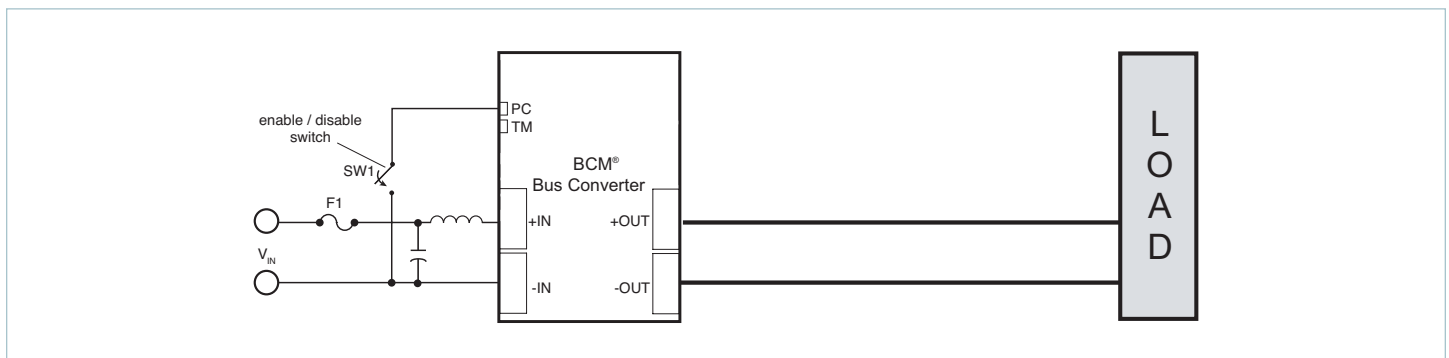
The BCM48BF080y240A00 is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded VI Chip package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the BCM48Bx080y240A00 increases overall system efficiency and lowers operating costs compared to conventional approaches.

Part Numbering

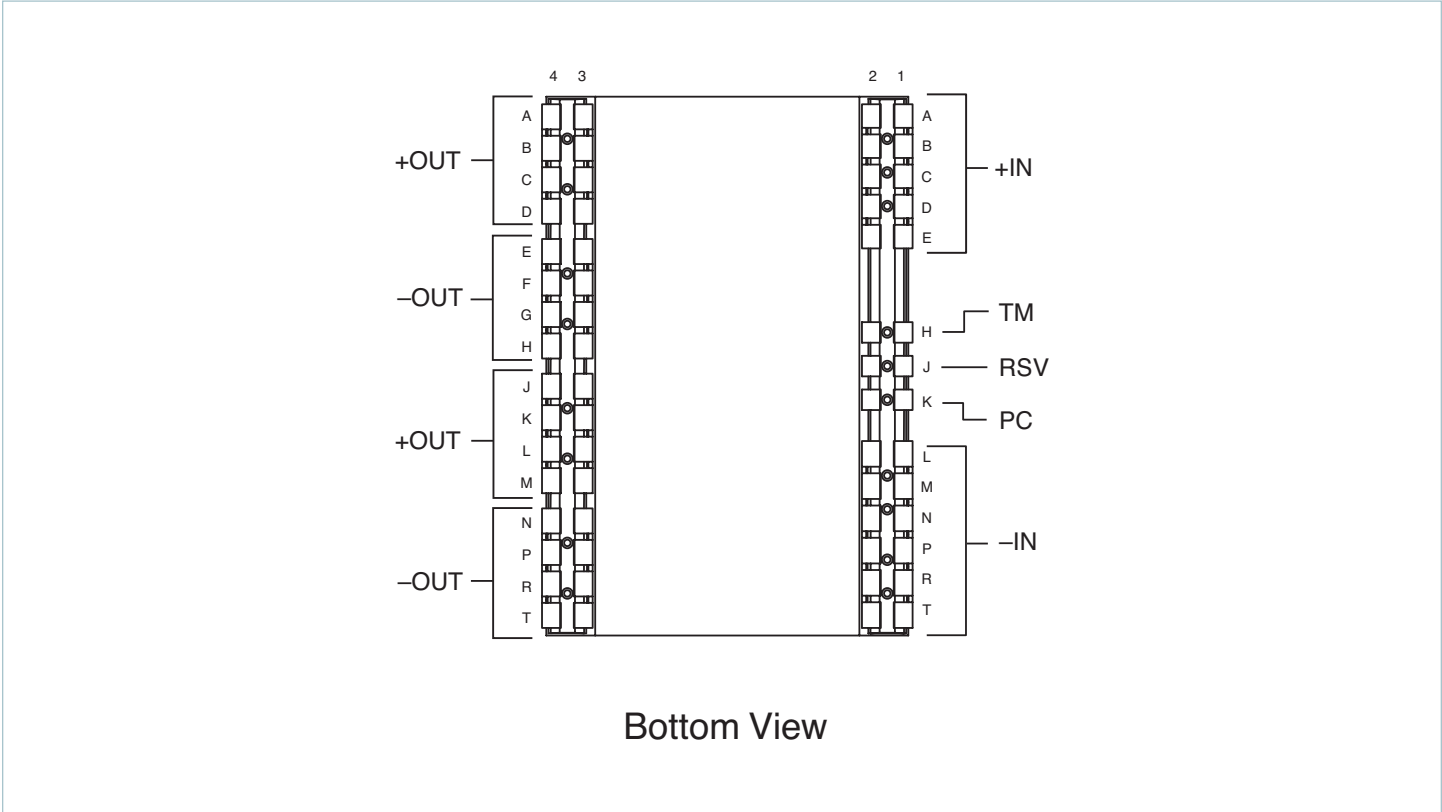
Product Number	Package Style (x)	Product Grade (y)
BCM48Bx080y240A00	F = J-Lead	T = -40 to 125°C
	T = Through hole	M = -55 to 125°C

For Storage and Operating Temperatures see General Characteristics

Typical Application



Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
A1-E1, A2-E2	+IN	INPUT POWER	Positive input power terminal
L1-T1, L2-T2	-IN	INPUT POWER RETURN	Negative input power terminal
H1, H2	TM	OUTPUT	Temperature monitor, input side referenced signal
J1, J2	RSV	NC	No connect
K1, K2	PC	OUTPUT/INPUT	Enable and disable control, input side referenced signal
A3-D3, A4-D4, J3-M3, J4-M4	+OUT	OUTPUT POWER	Positive output power terminal
E3-H3, E4-H4, N3-T3, N4-T4	-OUT	OUTPUT POWER RETURN	Negative output power terminal

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to -IN		-1	60	V
V _{IN} Slew Rate	Operational	-1	1	V/μs
Isolation Voltage, Input to Output			2250	V
+OUT to -OUT		-1	16	V
Output Current Transient	≤ 10ms, ≤ 10% DC	-3	45	A
Output Current Average		-2	36	A
PC to -IN		-0.3	20	V
TM to -IN		-0.3	7	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Input Voltage Range, Continuous	$V_{\text{IN_DC}}$		38		55	V
Input Voltage Range, Transient	$V_{\text{IN_TRANS}}$	Full current or power supported, 50ms max, 10% duty cycle max	38		55	V
Quiescent Current	I_{Q}	Disabled, PC Low		1.9	2.8	mA
V_{IN} to V_{OUT} Time	t_{ON1}	$V_{\text{IN}} = 48\text{V}$, PC floating	550	700	850	ms
No-Load Power Dissipation	P_{NL}	$V_{\text{IN}} = 48\text{V}$, $T_{\text{CASE}} = 25^{\circ}\text{C}$		4.0	5.5	W
		$V_{\text{IN}} = 48\text{V}$	3.0		10.0	
		$V_{\text{IN}} = 38 - 55\text{V}$, $T_{\text{CASE}} = 25^{\circ}\text{C}$			7.0	
		$V_{\text{IN}} = 38 - 55\text{V}$			11.0	
Inrush Current Peak	$I_{\text{INR_P}}$	Worse case of: $V_{\text{IN}} = 55\text{V}$, $C_{\text{OUT}} = 2300\mu\text{F}$, $R_{\text{LOAD}} = 350\text{m}\Omega$		7.5	12	A
DC Input Current	$I_{\text{IN_DC}}$	At $P_{\text{OUT}} = 240\text{W}$			0	A
Transformation Ratio	K	$K = V_{\text{OUT}} / V_{\text{IN}}$, at no load		1/6		V/V
Output Power (Average)	$P_{\text{OUT_AVG}}$				240	W
Output Power (Peak)	$P_{\text{OUT_PK}}$	10ms max, $P_{\text{OUT_AVG}} \leq 240\text{W}$			360	W
Output Current (Average)	$I_{\text{OUT_AVG}}$				36	A
Output Current (Peak)	$I_{\text{OUT_PK}}$	10ms max, $I_{\text{OUT_AVG}} \leq 36\text{A}$			45	A
Efficiency (Ambient)	η_{AMB}	$V_{\text{IN}} = 48\text{V}$, $I_{\text{OUT}} = 30\text{A}$; $T_{\text{CASE}} = 25^{\circ}\text{C}$	94.2	95.4		%
		$V_{\text{IN}} = 38 - 55\text{V}$, $I_{\text{OUT}} = 30\text{A}$; $T_{\text{CASE}} = 25^{\circ}\text{C}$	92.0			
		$V_{\text{IN}} = 48\text{V}$, $I_{\text{OUT}} = 15\text{A}$; $T_{\text{CASE}} = 25^{\circ}\text{C}$	94.0	95.6		
Efficiency (Hot)	η_{HOT}	$V_{\text{IN}} = 48\text{V}$, $I_{\text{OUT}} = 30\text{A}$; $T_{\text{CASE}} = 100^{\circ}\text{C}$	92.8	95.2		%
Efficiency (Over Load Range)	$\eta_{20\%}$	$6\text{A} < I_{\text{OUT}} < 30\text{A}$	91.0			%
Output Resistance	$R_{\text{OUT_COLD}}$	$I_{\text{OUT}} = 30\text{A}$, $T_{\text{CASE}} = -40^{\circ}\text{C}$	3.0	5.6	8.0	m Ω
	$R_{\text{OUT_AMB}}$	$I_{\text{OUT}} = 30\text{A}$, $T_{\text{CASE}} = 25^{\circ}\text{C}$	5.0	7.4	10.0	
	$R_{\text{OUT_HOT}}$	$I_{\text{OUT}} = 30\text{A}$, $T_{\text{CASE}} = 100^{\circ}\text{C}$	5.0	8.2	12.0	
Switching Frequency	F_{SW}		1.49	1.52	1.57	MHz
Output Voltage Ripple	$V_{\text{OUT_PP}}$	$C_{\text{OUT}} = 0\text{F}$, $I_{\text{OUT}} = 30\text{A}$, $V_{\text{IN}} = 48\text{V}$, 20MHz BW		160	230	mV
Output Inductance (Parasitic)	$L_{\text{OUT_PAR}}$	Frequency up to 30MHz, Simulated J-lead model		600		pH
Output Capacitance (Internal)	$C_{\text{OUT_INT}}$	Effective value at $8V_{\text{OUT}}$		45		μF
Output Capacitance (External)	$C_{\text{OUT_EXT}}$		0		2300	μF

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Protection						
Input Overvoltage Lockout Threshold	$V_{\text{IN_OVLO+}}$		55.1	58.5	60	V
Input Overvoltage Recovery Threshold	$V_{\text{IN_OVLO-}}$		55.1	57.2	58	V
Input Overvoltage Lockout Hysteresis	$V_{\text{IN_OVLO_HYST}}$			1.2		V
Overvoltage Lockout Response Time	t_{OVLO}			8		μs
Fault Recovery Time	$t_{\text{AUTO_RESTART}}$		610	670	730	ms
Input Undervoltage Lockout Threshold	$V_{\text{IN_UVLO-}}$		28.5	31.1	37.4	V
Input Undervoltage Recovery Threshold	$V_{\text{IN_UVLO+}}$		28.5	33.7	37.4	V
Input Undervoltage Lockout Hysteresis	$V_{\text{IN_UVLO_HYST}}$			1.6		V
Undervoltage Lockout Response Time	t_{UVLO}			8		μs
Output Overcurrent Trip Threshold	I_{OCP}		42	50	64	A
Output Overcurrent Response Time Constant	t_{OCP}	Effective internal RC filter		3.8		ms
Short Circuit Protection Trip Threshold	I_{SCP}		70			A
Short Circuit Protection Response Time	t_{SCP}			1		μs
Thermal Shut-Down Threshold	$T_{\text{J_OTP}}$		125			$^{\circ}\text{C}$

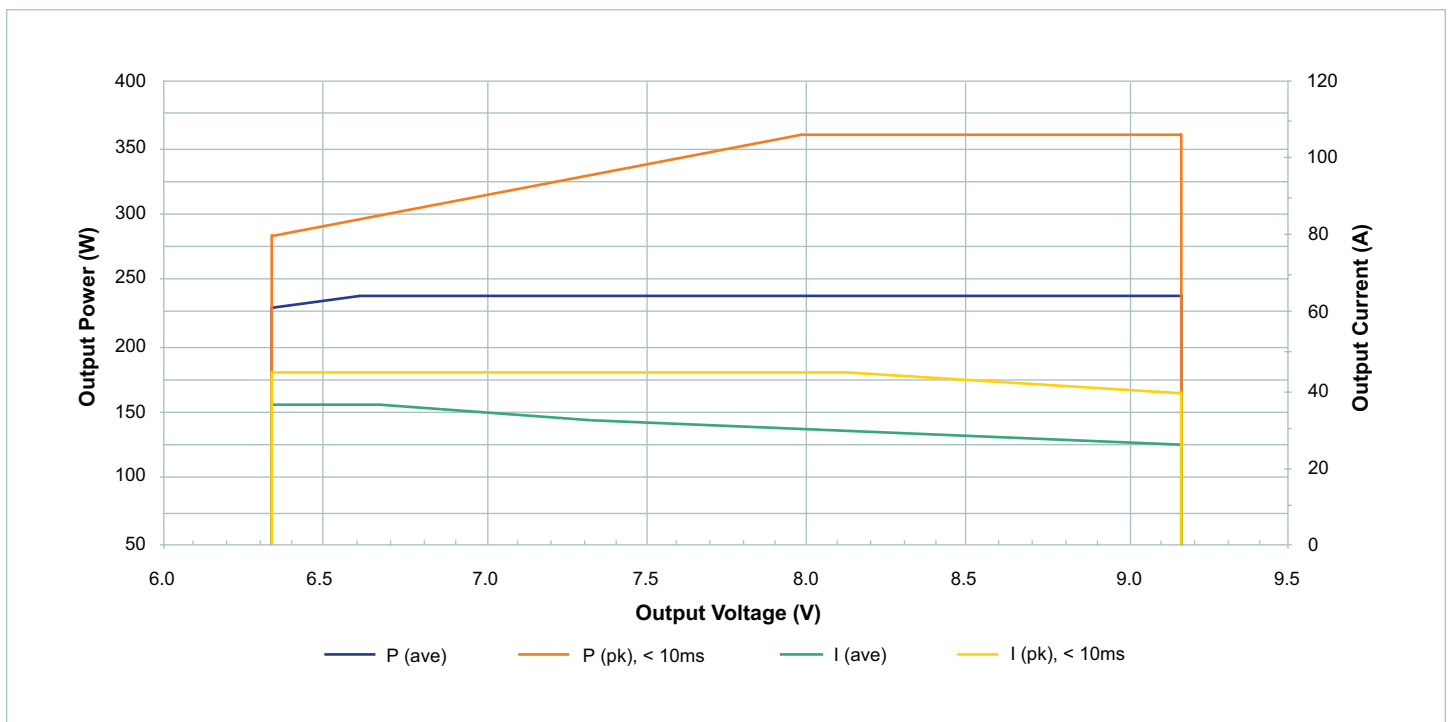


Figure 1 — Safe operating area

Signal Characteristics

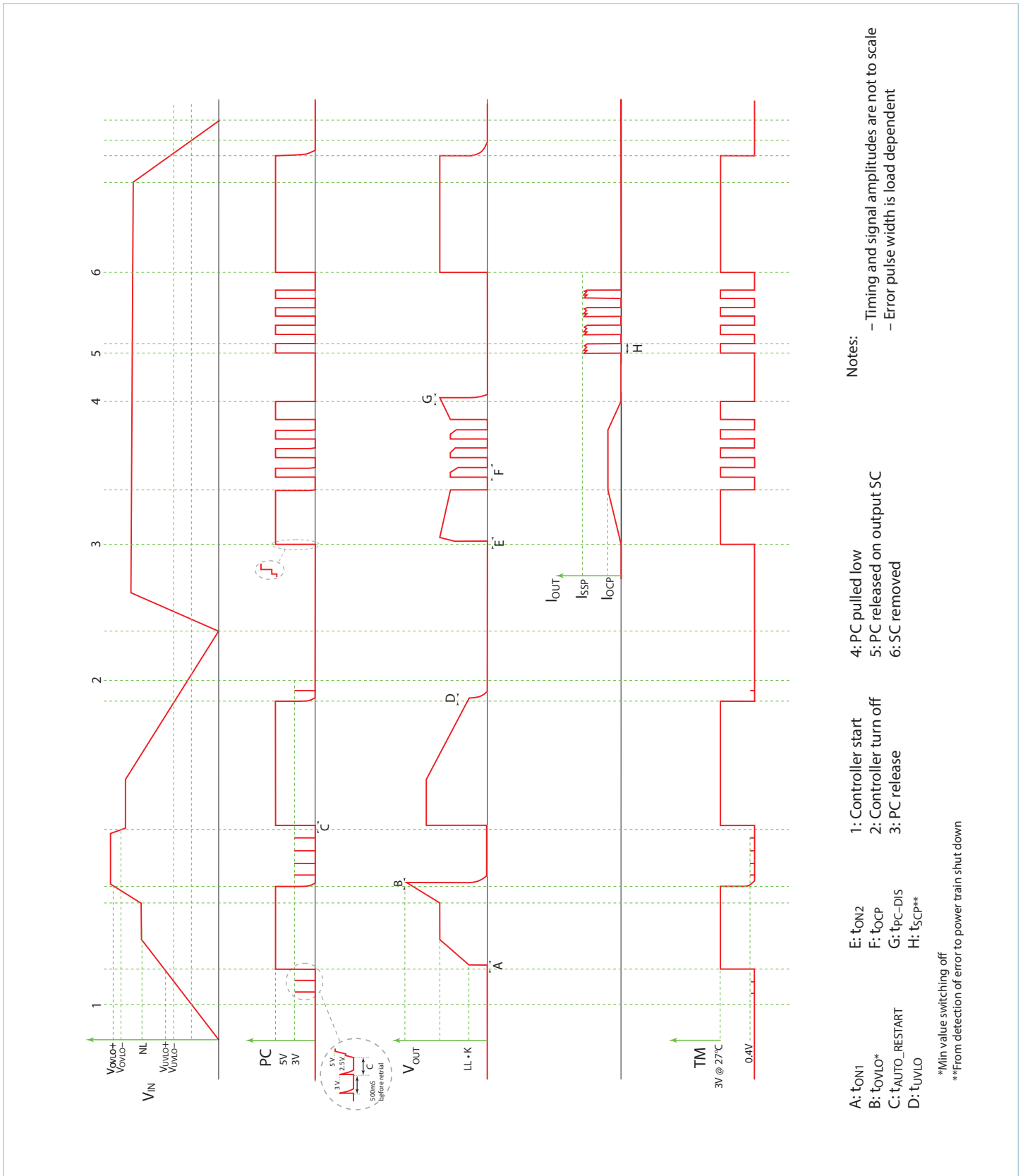
Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

Primary Control: PC									
<ul style="list-style-type: none"> The PC pin enables and disables the BCM. When held low, the BCM is disabled. In an array of BCM modules, PC pins should be interconnected to synchronize start up and permit start up into full load conditions. PC pin outputs 5V during normal operation. PC pin internal bias level drops to 2.5V during fault mode, provided V_{IN} remains in the valid range. 									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Output	Regular Operation	PC Voltage	V_{PC}		4.7	5.0	5.3	V	
		PC Available Current	$I_{\text{PC_OP}}$		2.0	3.5	5.0	mA	
	Standby	PC Source (Current)	$I_{\text{PC_EN}}$		50	100		μA	
		PC Resistance (Internal)	$R_{\text{PC_INT}}$	Internal pull down resistor	50	150	400	k Ω	
	Transition	PC Capacitance (Internal)	$C_{\text{PC_INT}}$				1000	pF	
	Start Up	PC Load Resistance	$R_{\text{PC_S}}$	To permit regular operation	60			k Ω	
Digital Input / Output	Regular Operation	PC Enable Threshold	$V_{\text{PC_EN}}$		2.0	2.5	3.0	V	
		PC Disable Threshold	$V_{\text{PC_DIS}}$				1.95	V	
	Standby	PC Disable Duration	$t_{\text{PC_DIS_T}}$	Minimum time before attempting re-enable	1			s	
	Transition	PC Threshold Hysteresis	$V_{\text{PC_HYSTER}}$				50	mV	
		PC Enable to V_{OUT} Time	t_{ON2}	$V_{\text{IN}} = 48\text{V}$ for at least t_{ON1} ms		50	100	150	μs
		PC Disable to Standby Time	$t_{\text{PC_DIS}}$				4	10	μs
		PC Fault Response Time	$t_{\text{FR_PC}}$	From fault to PC = 2V			100		μs

Temperature Monitor: TM									
<ul style="list-style-type: none"> The TM pin monitors the internal temperature of the controller IC within an accuracy of $\pm 5^{\circ}\text{C}$. Can be used as a "Power Good" flag to verify that the BCM module is operating. Is used to drive the internal comparator for Overtemperature Shut Down. 									
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit	
Analog Output	Regular Operation	TM Voltage Range	V_{TM}		2.12		4.04	V	
		TM Voltage Reference	$V_{\text{TM_AMB}}$	T_{J} controller = 27°C	2.95	3.00	3.05	V	
		TM Available Current	I_{TM}					100	μA
		TM Gain	A_{TM}				10		mV/ $^{\circ}\text{C}$
		TM Voltage Ripple	$V_{\text{TM_PP}}$	$C_{\text{TM}} = 0\text{pF}$, $V_{\text{IN}} = 48\text{V}$, $I_{\text{OUT}} = 30\text{A}$			120	200	mV
Digital Input / Output	Transition	TM Capacitance (External)	$C_{\text{TM_EXT}}$				50	pF	
		TM Fault Response Time	$t_{\text{FR_TM}}$	From fault to TM = 1.5V		10		μs	
	Standby	TM Voltage	$V_{\text{TM_DIS}}$				0	V	
		TM Pull Down (Internal)	$R_{\text{TM_INT}}$	Internal pull-down resistor		25	40	50	k Ω

Reserved: RSV								
Reserved for factory use. No connection should be made to this pin.								

Timing Diagram



Application Characteristics

The following values, typical of an application environment, are collected at $T_{CASE} = 25^{\circ}C$ unless otherwise noted. See associated figures for general trend data.

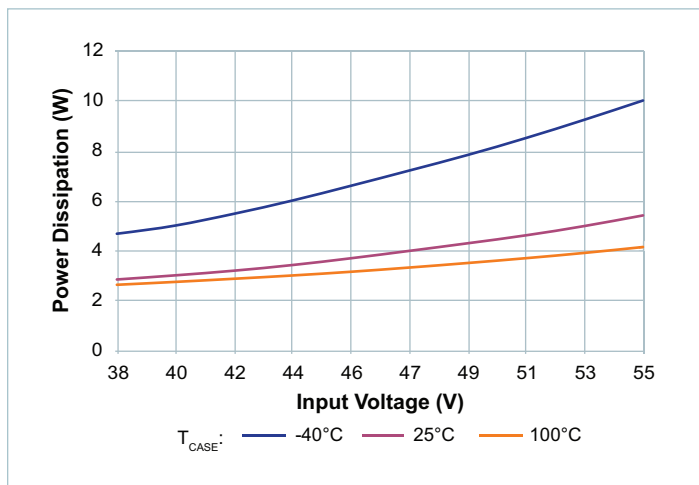


Figure 2 — No-load power dissipation vs. V_{IN}

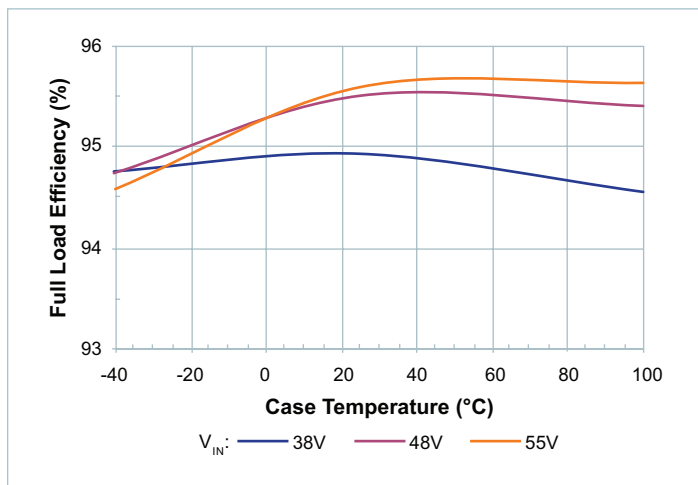


Figure 3 — Full-load efficiency vs. temperature; V_{IN}

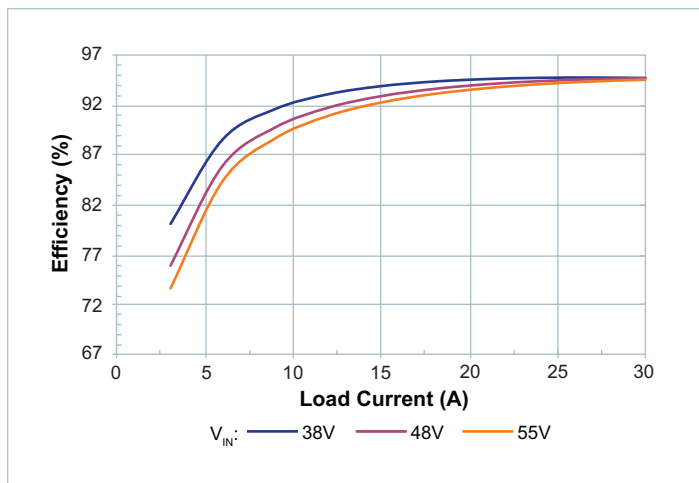


Figure 4 — Efficiency at $T_{CASE} = -40^{\circ}C$

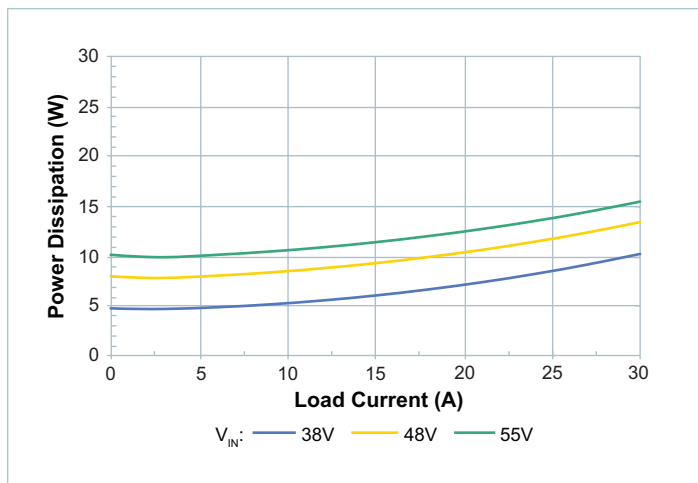


Figure 5 — Power dissipation at $T_{CASE} = -40^{\circ}C$

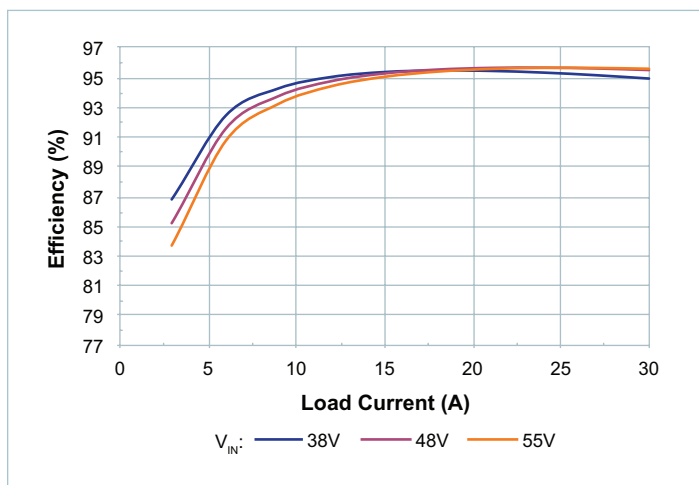


Figure 6 — Efficiency at $T_{CASE} = 25^{\circ}C$

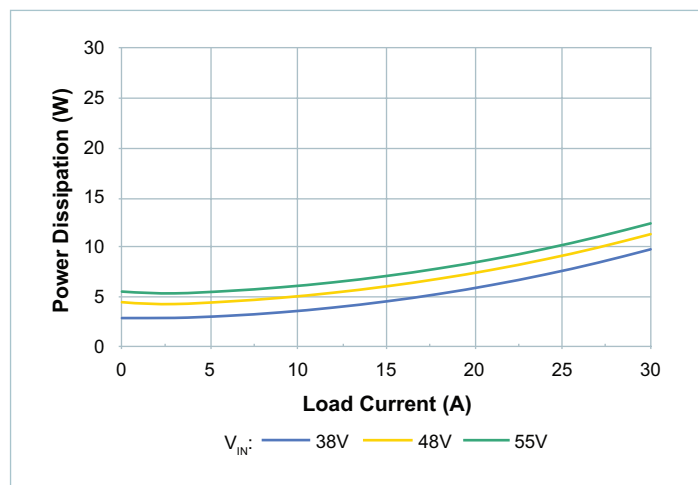


Figure 7 — Power dissipation at $T_{CASE} = 25^{\circ}C$

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at $T_{CASE} = 25^{\circ}C$ unless otherwise noted. See associated figures for general trend data.

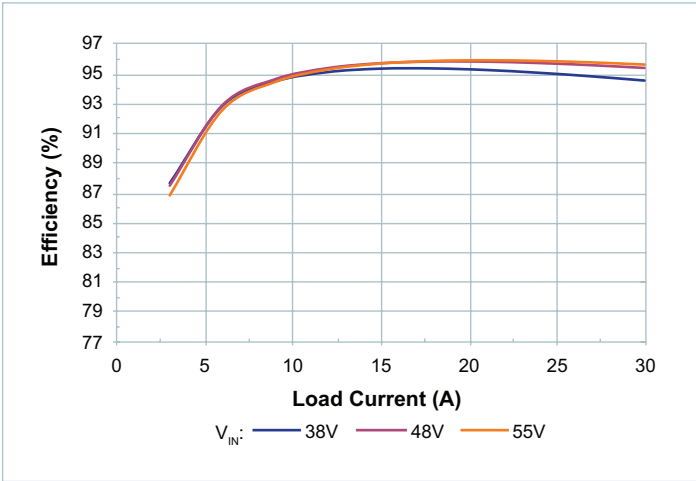


Figure 8 — Efficiency at $T_{CASE} = 100^{\circ}C$

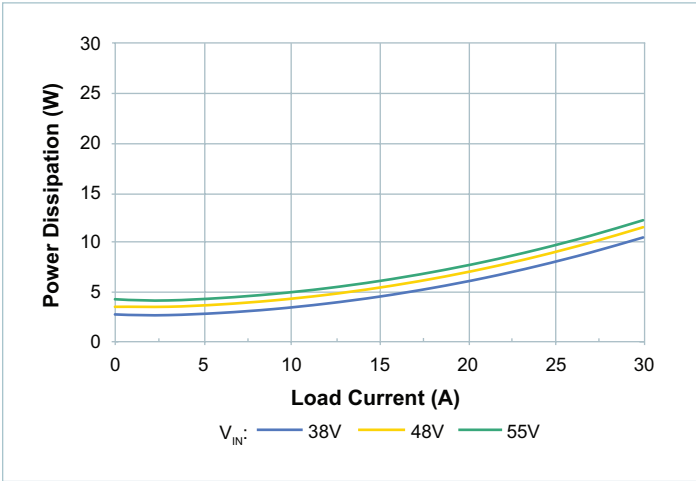


Figure 9 — Power dissipation at $T_{CASE} = 100^{\circ}C$

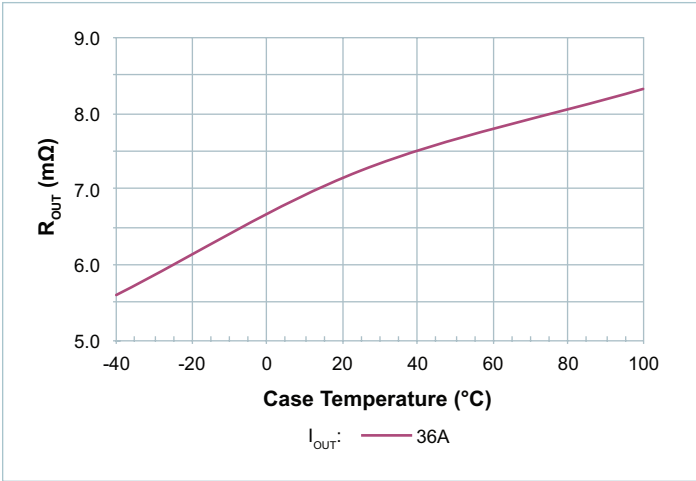


Figure 10 — R_{OUT} vs. temperature; nominal input

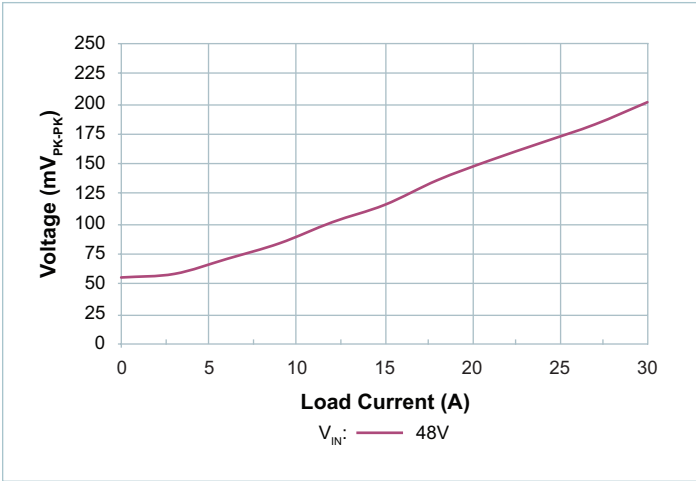


Figure 11 — V_{RIPPLE} vs. I_{OUT} ; no external C_{OUT} , board-mounted module, scope setting: 20MHz analog BW

Application Characteristics (Cont.)

The following values, typical of an application environment, are collected at $T_{CASE} = 25^{\circ}C$ unless otherwise noted. See associated figures for general trend data.

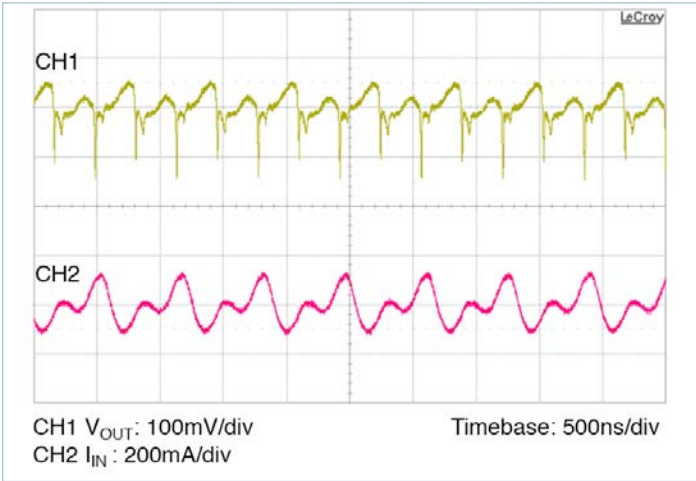


Figure 12 — Full-load ripple, $330\mu F C_{IN}$; no external C_{OUT} , board mounted module, scope setting: 20MHz analog BW

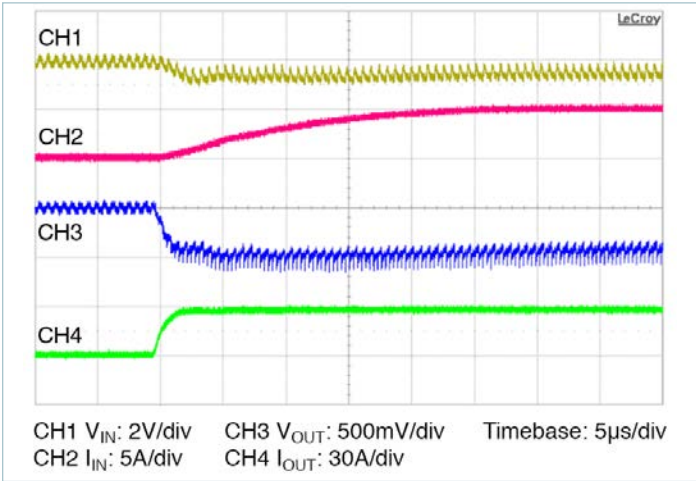


Figure 13 — 0 – 30A transient response: $C_{IN} = 330\mu F$, I_{IN} measured prior to C_{IN} , no external C_{OUT}

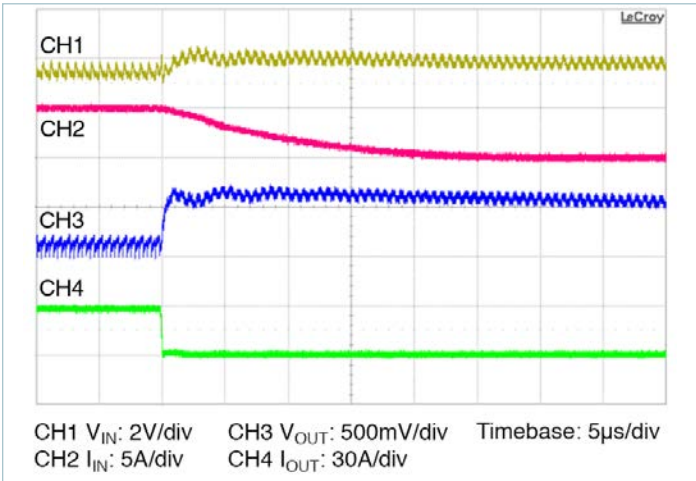


Figure 14 — 30 – 0A transient response: $C_{IN} = 330\mu F$, I_{IN} measured prior to C_{IN} , no external C_{OUT}

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		32.25 [1.270]	32.50 [1.280]	32.75 [1.289]	mm [in]
Width	W		21.75 [0.856]	22.00 [0.866]	22.25 [0.876]	mm [in]
Height	H		6.48 [0.255]	6.73 [0.265]	6.98 [0.275]	mm [in]
Volume	Vol	No heat sink		4.81 [0.294]		cm ³ [in ³]
Weight	W			14.5 [0.512]		g [oz]
Lead Finish		Nickel	0.51		2.03	μm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	T _J	BCM48Bx080T240A00 (T-Grade)	-40		125	°C
		BCM48Bx080M240A00 (M-Grade)	-55		125	
Thermal Resistance	θ _{JC}	Isothermal heatsink and isothermal internal PCB		1		°C/W
Thermal Capacity				5		Ws/°C
Assembly						
Peak Compressive Force Applied to Case (Z-Axis)		Supported by J-lead only			6	lbs
					5.41	lbs/ in ²
Storage Temperature	T _{ST}	BCM48Bx080T240A00 (T-Grade)	-40		125	°C
		BCM48Bx080M240A00 (M-Grade)	-65		125	°C
ESD Withstand	ESD _{HBM}	Human Body Model, JEDEC JESD 22-A114D.01 Class 1D	1000			V
	ESD _{CDM}	Charge Device Model, JEDEC JESD 22-C101-D	400			
Soldering						
Peak Temperature During Reflow		RoHS			245	°C
		Non-RoHS			225	
Peak Time Above Liquidus		Requires AN:009 compliance	60		90	s
Peak Heating Rate During Reflow		Requires AN:009 compliance	1	1.5	3	°C/s
Peak Cooling Rate Post Reflow		Requires AN:009 compliance	1	1.5	6	°C/s
Safety						
Working voltage (IN – OUT)	V _{IN_OUT}				60	V _{DC}
Isolation Voltage (Hipot)	V _{HIPOUT}		2,250			V _{DC}
Isolation Capacitance	C _{IN_OUT}	Unpowered unit	2500	3200	3800	pF
Isolation Resistance	R _{IN_OUT}	At 500V _{DC}	10			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer Profile		4.3		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		9.5		MHrs
Agency approvals / standards		cTÜVus				
		cURus				
		CE Marked for Low Voltage Directive and ROHS recast directive, as applicable.				

Using The Control Signals PC, TM

Primary Control (PC) pin can be used to accomplish the following functions:

- **Logic enable and disable for module:** Once t_{ON1} time has been satisfied, a PC voltage greater than V_{PC_EN} will cause the module to start. Bringing PC lower than V_{PC_DIS} will cause the module to enter standby.
- **Auxiliary voltage source:** Once enabled in regular operational conditions (no fault), each BCM module PC provides a regulated 5V, 3.5mA voltage source.
- **Synchronized start up:** In an array of parallel modules, PC pins should be connected to synchronize start up across units. This permits the maximum load and capacitance to scale by the number of paralleled modules.
- **Output disable:** PC pin can be actively pulled down in order to disable the module. Pull-down impedance shall be lower than 60Ω .
- **Fault-detection flag:** The PC 5V voltage source is internally turned off as soon as a fault is detected.

Note that PC can not sink significant current during a fault condition. The PC pin of a faulted module will not cause interconnected PC pins of other modules to be disabled.

Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- **Monitor the control IC temperature:** The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e., $3.0V = 300K = 27^{\circ}C$). If a heat sink is applied, TM can be used to protect the system thermally.
- **Fault-detection flag:** The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes microcontroller interface faults are detected on falling edges of TM signal.

Sine Amplitude Converter™ Point-of-Load Conversion

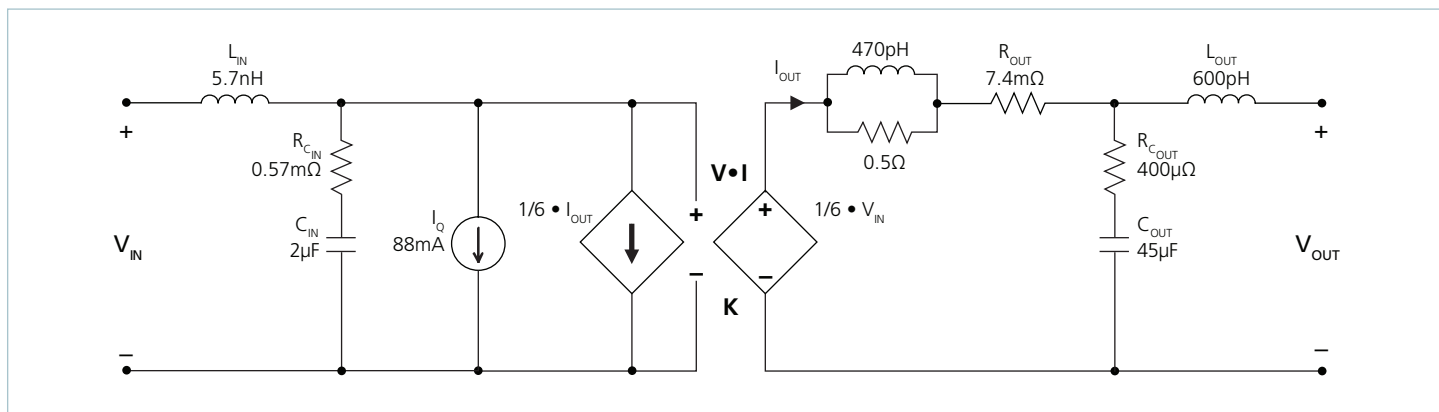


Figure 15 — VI Chip® module AC model

The Sine Amplitude Converter (SAC™) uses a high-frequency resonant tank to move energy from input to output. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The BCM48Bx080y240A00 SAC can be simplified into the preceding model.

At no load:

$$V_{OUT} = V_{IN} \cdot K \tag{1}$$

K represents the “turns ratio” of the SAC.

Rearranging Equation 1:

$$K = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

In the presence of a load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT} \tag{3}$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \tag{4}$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DS_ON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control, gate drive circuitry and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that R_{OUT} = 0Ω and I_Q = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{IN}.

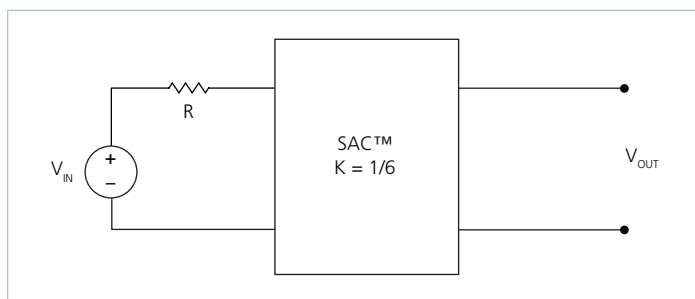


Figure 16 — K = 1/6 Sine Amplitude Converter with series input resistor

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \cdot R) \cdot K \tag{5}$$

Substituting the simplified version of Equation 4 (I_Q is assumed = 0A) into Equation 5 yields:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R \cdot K^2 \tag{6}$$

This is similar in form to Equation 3, where R_{OUT} is used to represent the characteristic impedance of the SAC. However, in this case a real R on the input side of the SAC is effectively scaled by K² with respect to the output.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 28mΩ, with K = 1/6.

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 17.

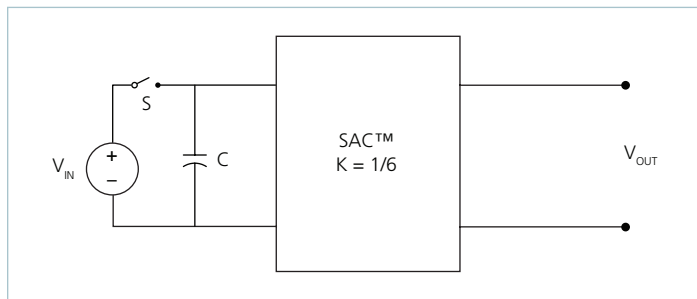


Figure 17 — Sine Amplitude Converter™ with input capacitor

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{IN} , the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \cdot K \quad (8)$$

substituting Equations 1 and 8 into Equation 7 reveals:

$$I_{OUT} = \frac{C}{K^2} \cdot \frac{dV_{OUT}}{dt} \quad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C , specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a $K = 1/6$ as shown in Figure 17, $C = 1\mu\text{F}$ would appear as $C = 36\mu\text{F}$ when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point-of-load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low-loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No-load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (P_{ROUT}): refers to the power loss across the BCM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{ROUT} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{ROUT} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\begin{aligned} \eta &= \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{ROUT}}{P_{IN}} \quad (12) \\ &= \frac{V_{IN} \cdot I_{IN} - P_{NL} - (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}} \\ &= 1 - \frac{(P_{NL} + (I_{OUT})^2 \cdot R_{OUT})}{V_{IN} \cdot I_{IN}} \end{aligned}$$

Input and Output Filter Design

A major advantage of SACTM systems versus conventional PWM converters is that the transformers do not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- **Guarantee low source impedance:**

To take full advantage of the BCM's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1μF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- **Further reduce input and/or output voltage ripple without sacrificing dynamic response:**

Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor. This is illustrated in Figures 13 and 14.

- **Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:**

The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Total load capacitance at the output of the BCM shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500kHz the module appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Equation 13.

$$C_{OUT} = \frac{C_{IN}}{K^2} \quad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the BCM48Bx080y240A00 case to less than 100°C will keep all junctions within the VI Chip module below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- Apply same input / output filters (if present) to each unit.

For further details see [AN:016 Using BCM Bus Converters in High Power Arrays](#).

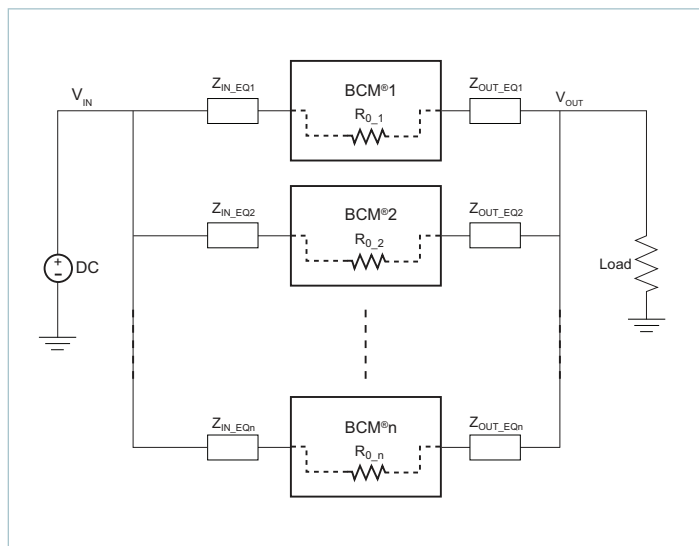


Figure 18 — BCM module array

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum current of BCM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: $\leq 10A$ Littlefuse Nano² Fuse.

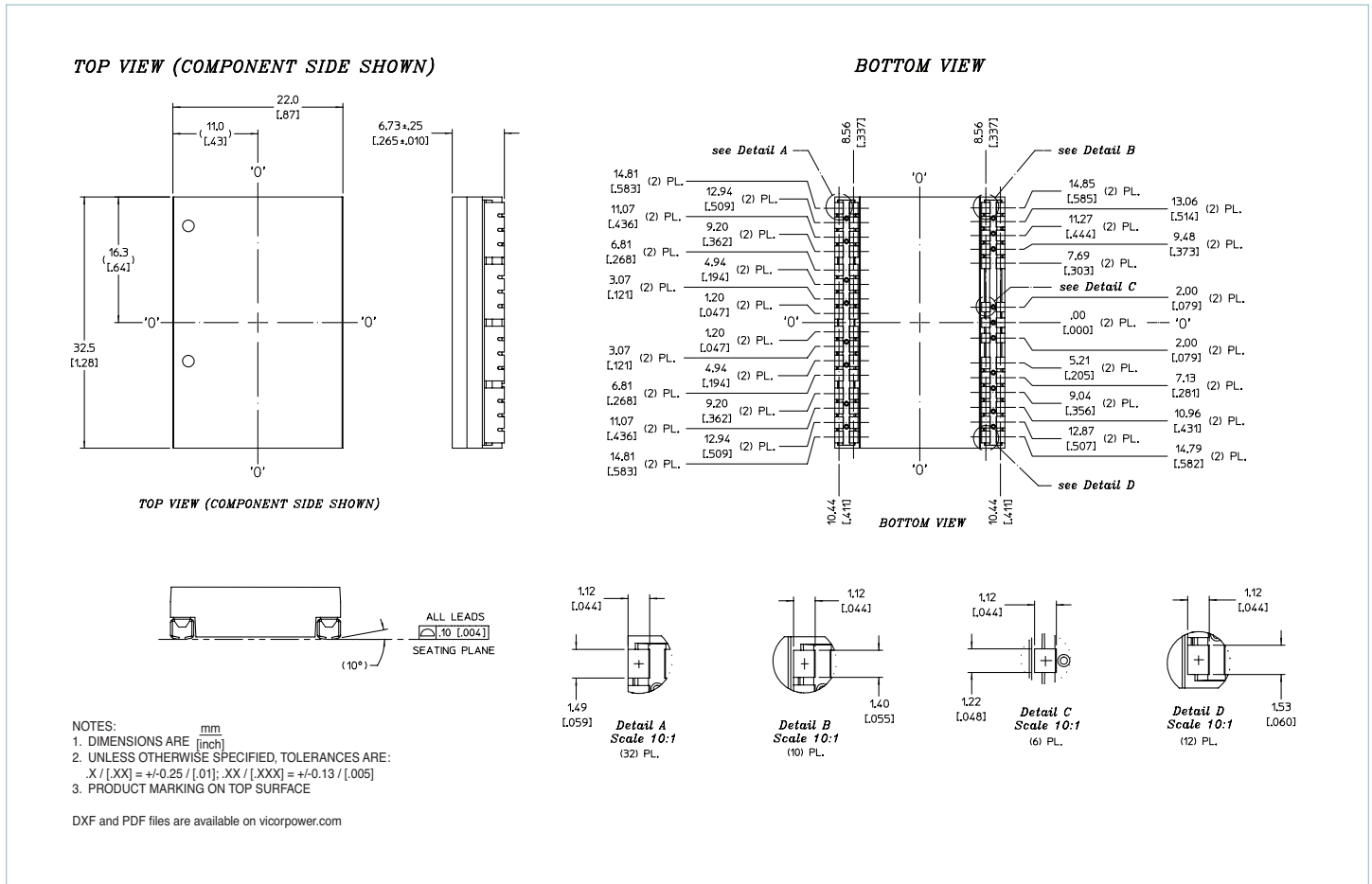
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{IN} \cdot K$. The module will continue operation in this fashion for as long as no faults occur.

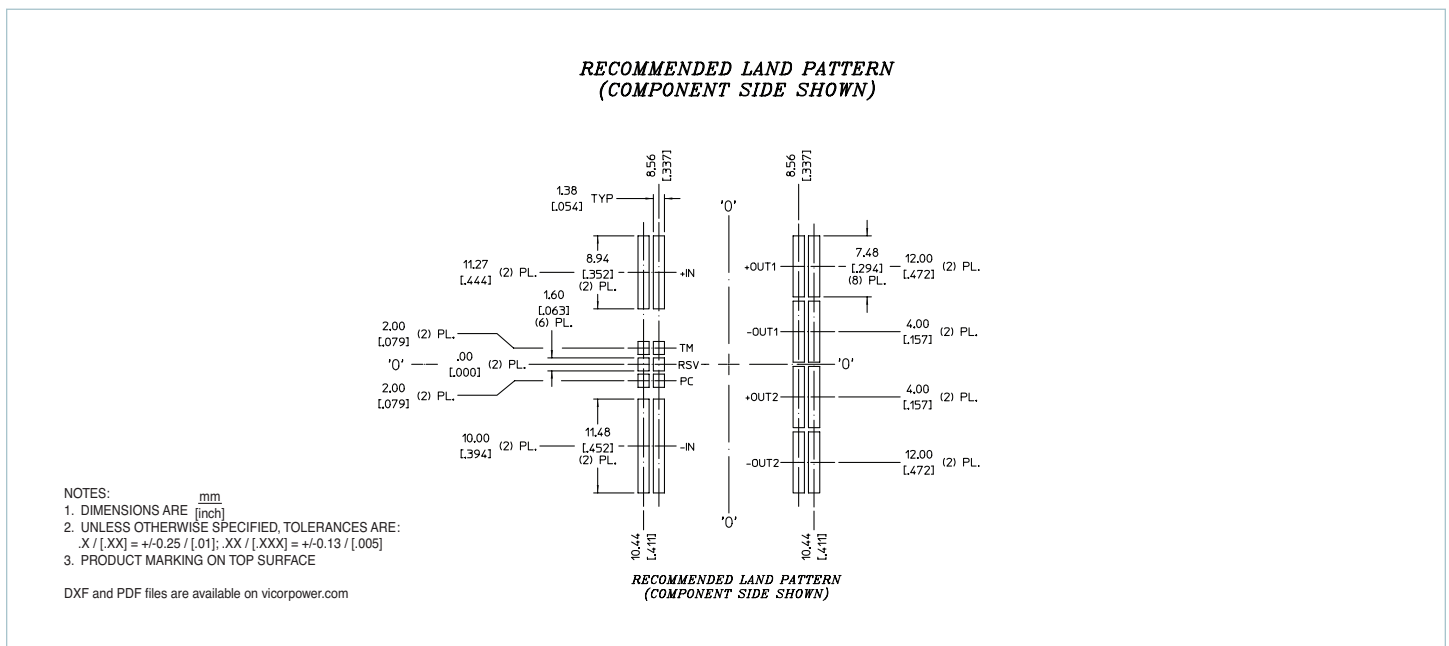
The BCM48Bx080y240A00 has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10ms, 10% duty cycle is permitted and has been qualified to cover these cases.

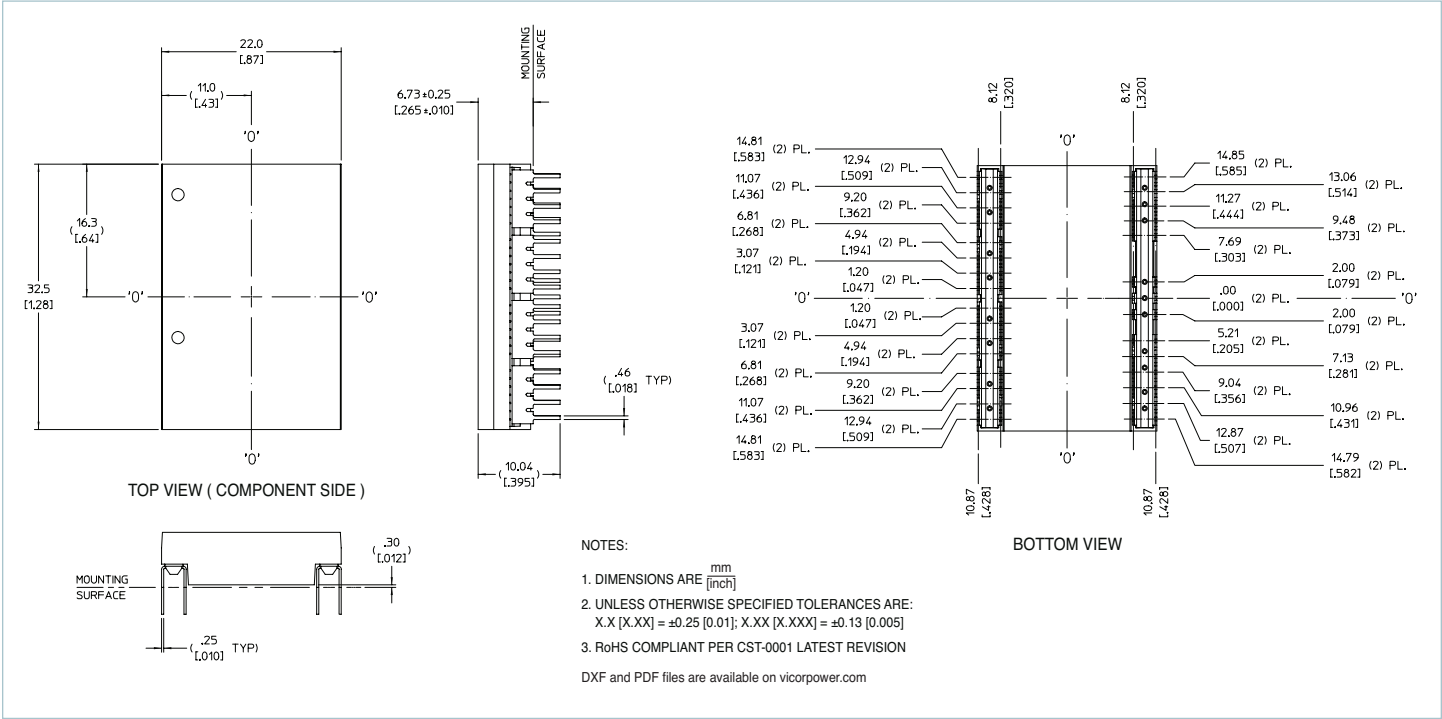
J-Lead Package Mechanical Drawing



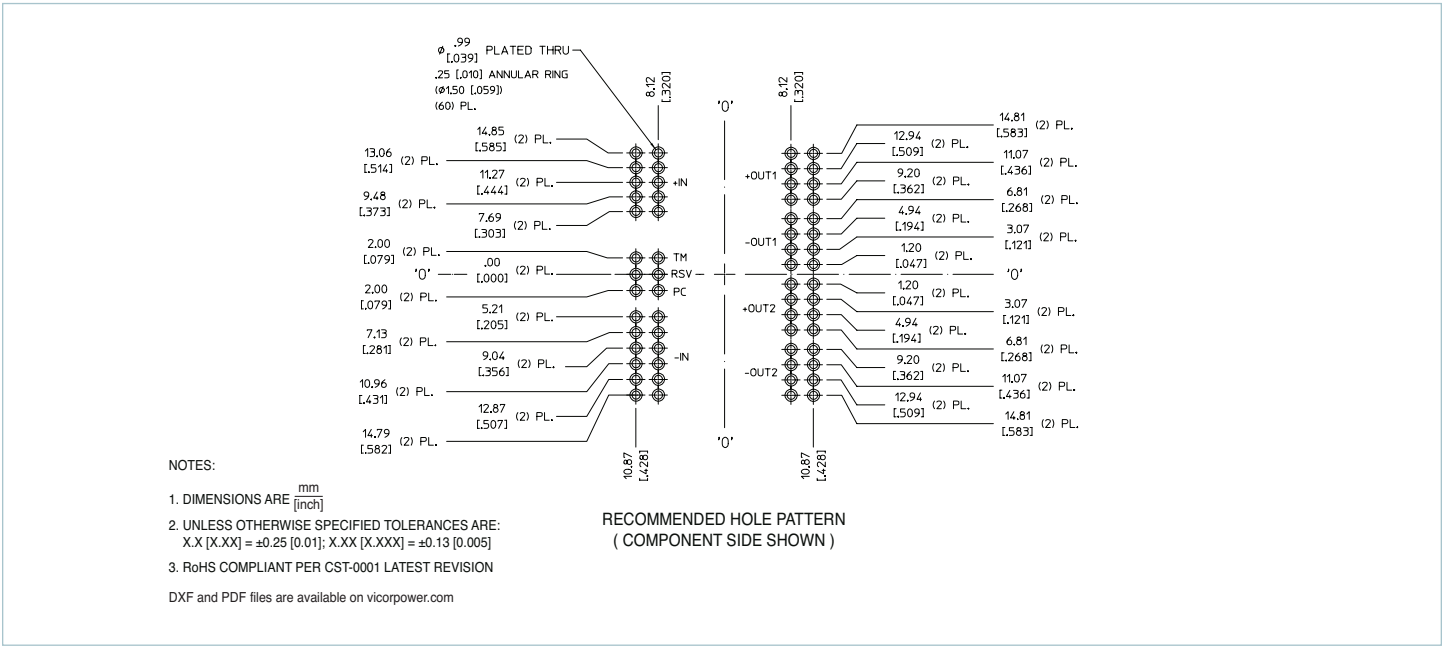
J-Lead Package Recommended Land Pattern



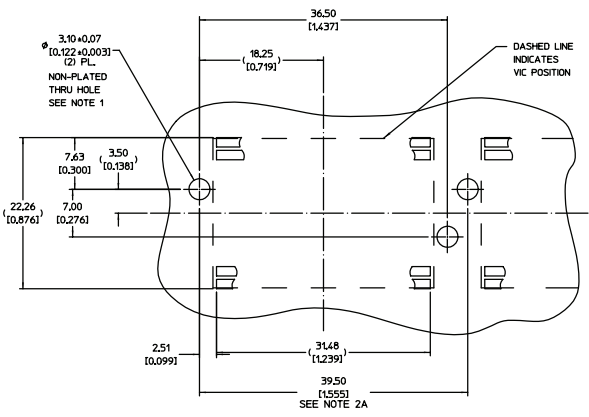
Through Hole Package Mechanical Drawing



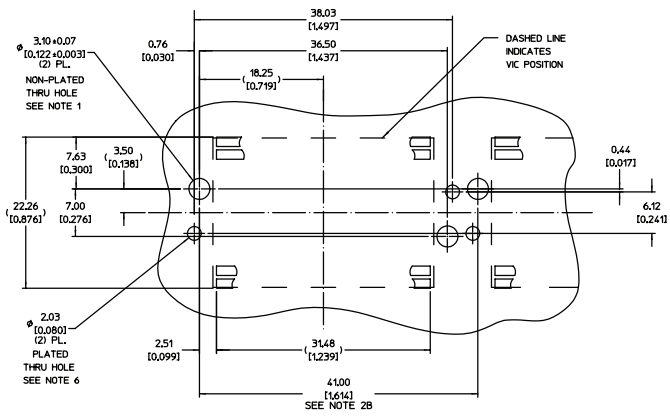
Through Hole Package Recommended Land Pattern



Recommended Heat Sink Push Pin Location



(NO GROUNDING CLIPS)



(WITH GROUNDING CLIPS)

Notes:

1. Maintain 3.50 [0.138] Dia. keep-out zone free of copper, all PCB layers.
2. (A) Minimum recommended pitch is 39.50 [1.555]. This provides 7.00 [0.275] component edge-to-edge spacing, and 0.50 [0.020] clearance between Vicor heat sinks.
(B) Minimum recommended pitch is 41.00 [1.614]. This provides 8.50 [0.334] component edge-to-edge spacing, and 2.00 [0.079] clearance between Vicor heat sinks.
3. VI Chip® module land pattern shown for reference only; actual land pattern may differ. Dimensions from edges of land pattern to push-pin holes will be the same for all full-size VI Chip® products.
4. RoHS compliant per CST-0001 latest revision.
5. Unless otherwise specified: Dimensions are mm [inches] tolerances are:
x.x (x.xx) = ±0.3 [0.01]
x.xx (x.xxx) = ±0.13 [0.005]
6. Plated through holes for grounding clips (33855) shown for reference, heat sink orientation and device pitch will dictate final grounding solution.

Revision History

Revision	Date	Description	Page Number(s)
1.5	01/04/21	Provided additional information to soldering guidelines	11
1.6	02/21/23	Revised t _{AUTO_RESTART} and t _{ON1} specifications	4, 5, 10, 13, 14, 16,

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