

Customer Part:

Description

- A disciplined OCXO incorporating sync to a 1PPS input and provides 1PPS output with up to 1.5µs holdover stability achieved by using an adaptive algorithm. Current internal parameters of the algorithm are available to the user via Tx and Rx commands.
- Model IQCM-200
- Model Issue number 3



Frequency Parameters

- Frequency 10.0MHz
- Operating Temperature Range -10.00 to 70.00°C
- Rise and Fall time: 8ns max
- Duty Cycle: 45/55% max
- Accuracy (24-hour averaging when locked to 1PPS): ±1E-12 max
- Short Term Stability (ADEV, tested after powered for 1 hour reference to T=25°C, τ=1s): 2E-11 max
- Frequency Stability (Temperature varied across the operating temperature range, measurement referenced to frequency observed with $f_{ref} = (\Delta f_{max} + f_{min})/2$): ±0.2 ppb typical
- Ageing (Vs and temperature constant, reference to T=25°C, Vs = 5.0V, in free run mode and after 30 days operation): ±0.2ppb per day
±10ppb per year
- Holdover Capability:
Reference 7 days powered on, 3 days GPS lock
Temperature varied <±1°C/min within operating temperature range

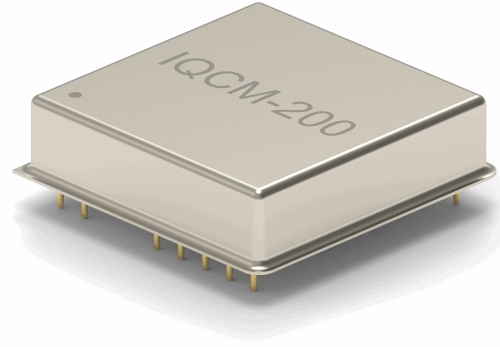
Specification example:
0 to 60°C ±1.5µs/24 hours (LTE compatible)

Temperature range option:
0 - 60°C
ΔT ≤ ±5°C
ΔT ≤ ±2°C

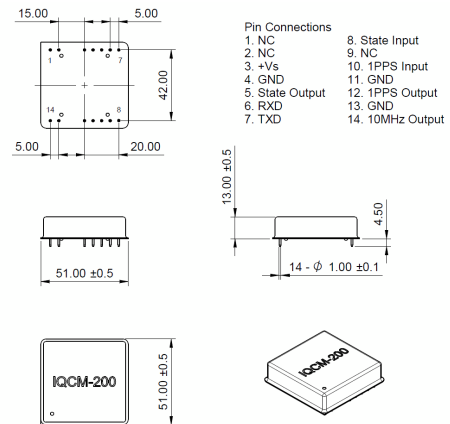
Holdover time range options:
8 hrs
24 hrs

Phase deviation range options:
±1.5µs
±8.0µs

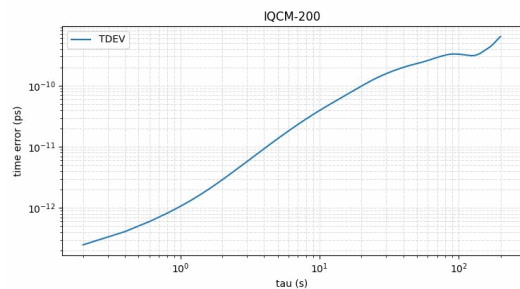
Note: Other options available on request



Outline (mm)



Typical TDEV Plot



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Customer Part:**Electrical Parameters**

- Supply Voltage 5.0V ±5%
- Current Consumption (@25°C):
 - 1.4A during warm up
 - 600mA steady state
- AC Ripple (10Hz to 1MHz): 50mV pk-pk max
- 1PPS Reference Input (15pF test condition):
 - Waveform: HCMOS
 - ViH: 2.7V min
 - ViL: 0.4V max
 - Pulse Width: 10us min
- State Input (5mA load max):
 - Lock: 2.7V min
 - Unlock: 0.4V max
- Note 4: Pins 4 to 13 should not be subjected to a voltage greater than 3.6V. If subjected to a higher voltages the processor will be damaged and the unit will not function correctly.

Output Details

- Output Compatibility HCMOS
- 1PPS Reference Output (50Ω test condition):
 - Waveform: HCMOS
 - VoH: 2.7V min
 - VoL: 0.4V max
 - Pulse Width: 10μs min
- State Output:
 - Module Locked: 2.7V min
 - Module Holdover: 0.4V max
 - Module Locked means Working State is = Run2
- Serial UART:
 - VoL and ViL: 0.4V max
 - VoH and ViH: 2.7V min
 - Baud: 9600 8-N-1
- 10MHz RF Output Details:
 - HCMOS Compatible, 15pF load (Sinewave 50Ω option available)
 - VoH: 2.7V min
 - VoL: 0.4V max

Noise Parameters

- Phase Noise on 10MHz RF output signal (dBc/Hz):

Offset	Typical	Max
10Hz	-118	-113
100Hz	-138	-133
1kHz	-148	-143
10kHz	-150	-145
100kHz	-150	-145
1MHz	-150	-150

Environmental Parameters

- Storage Conditions:
 - Temperature: -55 to 105°C
 - Humidity: 30 to 80%
- Shock: IEC68-2-27 Test Ea, severity 50A, 50G 11ms half sinewave, 3 times in three mutually perpendicular axis
- Vibration: IEC 68-2-06 Test Fc, 10G, 0.75mm acceleration, 10Hz to 500Hz, 3 times in three mutually perpendicular axis

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Customer Part:**Manufacturing Details**

- Application Information (Reference Drawing):
Connect the 1PPS output of your GPS system, for example, to the IQCM-200. A MCU can be used to monitor the working state of the IQCM-200.
- Working States (Reference Drawing):
Run1: Fast track. Adjust the OCXO 10MHz output frequency quickly to track the 1PPS to 10MHz with 1PPS reference.

Run2: Slow track. Adjust the OCXO 10MHz output frequency slowly when phase error is in the defined range.

Holdover: No 1PPS input present; an algorithm enables adaptive modelling of the frequency stability of an OCXO with reference to the 1PPS timing signal.

Free Run: Clock module powered up with no 1PPS input.

- Note 1: The IQCM-200 should be left powered and running for 7 days minimum before operation to allow for the OCXO's internal drift to stabilise.

Note 2: The adaptive module algorithm can be built after two days operation with good 1PPS signal, however this data will be lost at power down.

Note 3: When State input (Pin 8) is set low the IQCM-200 will operate in Holdover mode regardless of the 1PPS signal condition.

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- Output Data Word Example:
\$PDP,00,0,F,Q,-3095,32768.0000,32768.0000,000,000,000000
.0000,00000.0000,00000.0000,00000.0000,3-23,+000.0000,-0
000,www.iqdfp.com,1.1,2011-05-16*55

(See table for full description)

- Frequency: 10.0MHz
- ESD Level:
ANSI/ESDA/JEDEC JS-001-2010; HBM Class 2; 2kV to 4kV
ANSI/ESDA/JEDEC JS-001-2010; Machine Model Class B
200V to 400V

Compliance

- RoHS Status (2015/863/EU) Compliant
- REACH Status Compliant
- MSL Rating (JDEC-STD-033): Not Applicable

Packaging Details

- Pack Style: Bulk Loose in bulk pack
Pack Size: 1
- *Alternative packing option available*

Technical Notes

- *Holdover stability 1.5µs in 24hrs ref ±2°C*

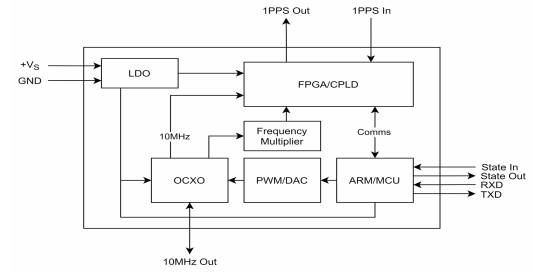
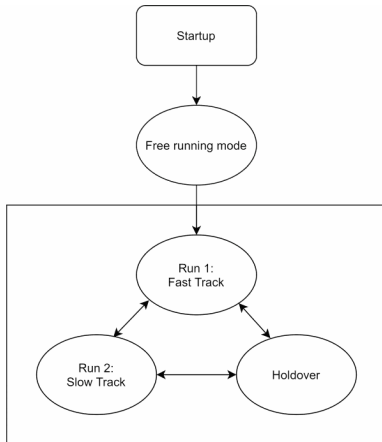
Workflow Diagram**Functional Block Diagram****Sales Office Contact Details:**

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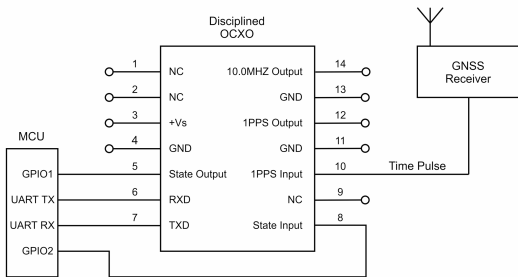
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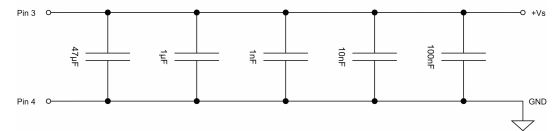
Customer Part:



Application Information



Recommended Supply Filtering



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Customer Part:
Output Data Word (Format Key: c=Character, d=Numerical Digit, s=Sign)

Field No.	Name	Format	Description	Length
0	\$PDP	\$ccc	Message ID, Protocol Header	4
1	No	dd	Message No	2
2	TxRxFlag	d	Transmit and Receive Flag (0=upper computer transmit, 1=upper computer receive)	1
3	CStatus	c	Current Status (F=warm up, L=lock, H=holdover)	1
4	TrackStatus	d	Track status (Q= fast track, S = slow track)	1
5	cPHDiff	sdddd	Current phase difference, 1 unit = 6.25ns	5
6	cPWM1	dddd.dddd	Current PWM1 (Voltage control value1)	10
7	cPWM2	dddd.dddd	Current PWM2 (Voltage Controlled Value 2), not used, default value =32769.000000	10
8	SYNCNT	ddd	The synchronous times	3
9	HCNT	ddd	Power on hours count	3
10	HPAVG	dddd.dddd	The average of the PWM in the last half hour	10
11	VCH1	dddd.dddd	Voltage Controlled compensation value every half hour	10
12	HPMOD	dddd.dddd	The Module PWM Value	10
13	VCM10	dddd.dddd	Voltage controlled compensation value every 10mins	10
14	POS	d-dd	The position of the product. (Layer-No), just for the inner test.	4
15	TEMP	sdddd.ddd	The temperature monitor inside the module	9
16	TcPHDiff	sdddd	The product current phase difference	5
17	Website		www.IQDFP.com	13
18	Version	d.d	version	3
19	Date	dddd-dd-dd	Date	10
20		dd	55	2
21	END		<CR><LF>	2

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