Description

The TSE2004GB2C0 digital temperature sensor comes with several user-programmable registers to provide maximum flexibility for temperature-sensing applications. The user-programmable registers specify critical, upper and lower temperature limits, as well as hysteresis settings. Both the limits and hysteresis values are used for communicating temperature events from the chip to the system. This communication is done using the EVENT_n pin, which has an open-drain configuration. The user has the option of setting the EVENT_n pin polarity as either an active-low or active-high comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems.

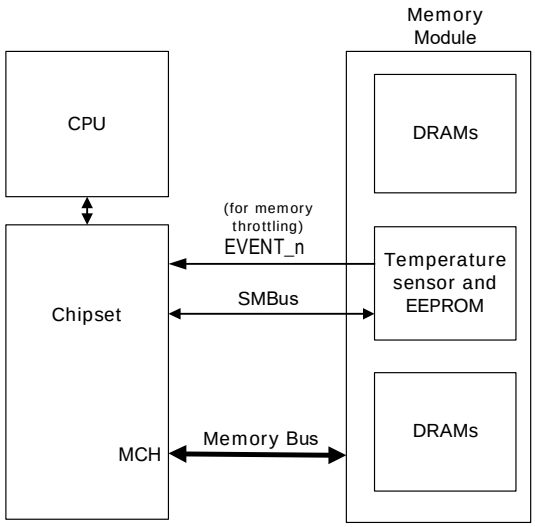
The sensor uses an industry standard 2-wire, I^2C/SMBus serial interface, and allows up to eight devices to be controlled on the bus.

The 4Kbit (512 bytes) Serial EEPROM memory in the part is organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128 byte blocks. The device can selectively lock the data in any or all of the four 128-byte blocks.

Typical Applications

- DIMM modules (DDR3, DDR4)
- Servers, laptops, ultra-portables, PCs, etc.
- Industrial temperature monitors
- Hard disk drives and other PC peripherals

Figure 1. Memory Module Temperature Sensor Application



Features

- Compliant to JEDEC TSE2004av Device Specification (JEDEC Standard No. 21-C, Section 4.1.6)
- Temperature Sensor plus a 512-byte Serial EEPROM
- A 512-byte Serial EEPROM for SPD
- Single supply: 2.2V to 3.6V
- Accurate timeout support that meets strict SMBus specifications for: 25ms (minimum), 35ms (maximum)
- Timeout supported for Temperature Sensor and EEPROM
- Timeout supported in all modes:
  - Active mode for Temperature Sensor and EEPROM
  - EEPROM in standby or Temperature Sensor in shutdown
  - EEPROM in standby and Temperature Sensor in shutdown
- Schmitt trigger and noise filtering on bus inputs
- A 2-wire serial interface: 10kHz to 1MHz (maximum) I^2C™/ SMBus™
- Available package: 8-DFN, 2.0 × 3.0 × 0.75 mm

Temperature Sensor Features

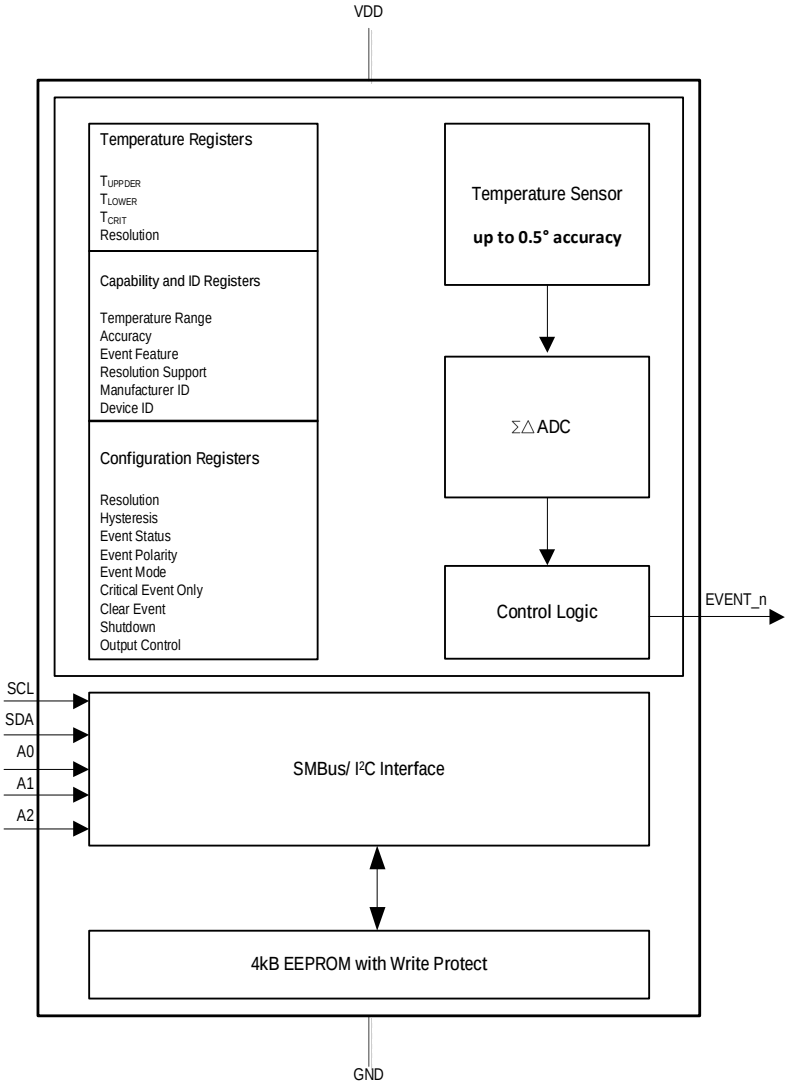
- Temperature converted to digital data
- Sampling rate of 125ms (maximum)
- Selectable 0, 1.5°C, 3°C, 6°C Hysteresis
- Programmable resolution from 0.0625°C to 0.5°C
- Accuracy:
  - 0.5°C / ±1.0°C (typ./max.) from +75°C to +95°C
  - ±1.0°C / ±2.0°C (typ./max.) from +40°C to +125°C
  - ±2.0°C / ±3.0°C (typ./max.) from -40°C to +125°C

Serial EEPROM Features

- Individual Reversible Software Data Protection for all 128-byte blocks
- Byte and page (up to 16 bytes) Write operation
- Self-time Write cycle
- Automatic address incrementing
- Random and sequential Read modes

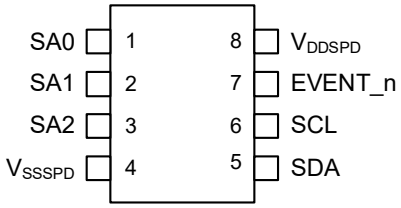
Contents

Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2 x 3 mm 8-DFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions[a]

Number	Pin Name	Definition
1	SA0	Select Address 0
2	SA1	Select Address 1
3	SA2	Select Address 2
4	V_{SSSPD}	Ground
5	SDA	Serial Data In
6	SCL	Serial Clock In
7	EVENT_n	Temperature Event Out
8	V_{DDSPD}	Supply Voltage

[a] The thermal sensing heat paddle is located at the bottom of the package. JEDEC suggests connecting the heat paddle to ground for better thermal connection between the DIMM PCB plane and the temperature sensor.

Functional Description

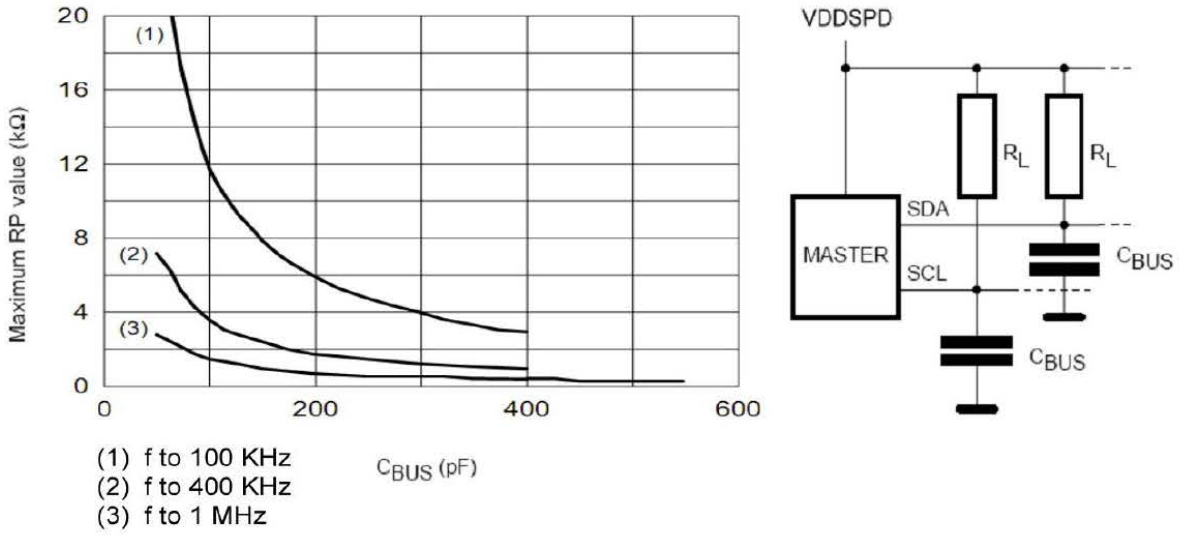
Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD} (to calculate the value of the pull-up resistor, see Figure 3). In most applications, this method of synchronization is not employed and the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open-drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from the Serial Data (SDA) to the most positive V_{DDSPD} in the i^2C Bus chain (to calculate the value of the pull-up resistor, see Figure 3).

Figure 3. Maximum R_L Value vs. Bus Capacitance (C_{BUS}) for an I^2C Bus



Select Address (SA0, SA1, SA2)

These input signals are used to create the Logical Serial Address (LSA) that is compared to the least significant bits (b3, b2, b1) of the 7-bit Slave Address (Table 9). The SA0 input is used to detect the V_{HV} voltage when decoding an SWPn or CWP instruction. For decoding details (see Table 9).

EVENT_n

The TSE2004GB2C0 EVENT_n pin is an open drain output that requires a pull-up to V_{DDSPD} on the system motherboard, or integrated into the master controller. The TSE2004GB2C0 EVENT_n pin has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are *Interrupt, Comparator, or TCRIT Only*.

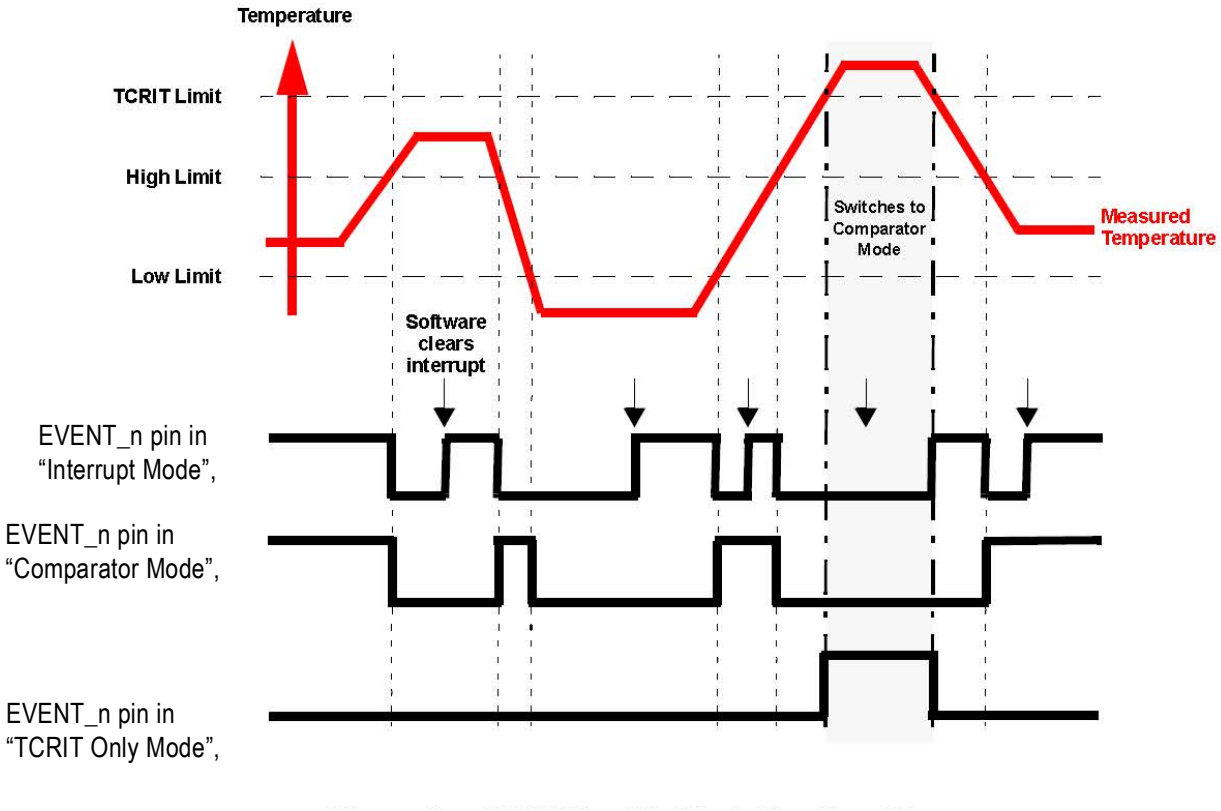
In Interrupt Mode, the EVENT_n pin will remain asserted until it is released by writing a 1 to the *Clear Event* bit in the Status Register. The value to Write is independent of the EVENT_n polarity bit.

In Comparator Mode, the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Lastly, in the TCRIT Only Mode, the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT limit minus the TCRIT hysteresis. The operation of the different modes over time and temperature are illustrated (Figure 4).

Systems that use the *active high* mode for EVENT_n must be wired point-to-point between the TSE2004GB2C0 and the sensing controller. Wire-OR configurations should not be used with an active high EVENT_n since any device pulling the EVENT_n signal low, will mask the other devices on the bus. Also note, the normal state of EVENT_n in *active high* mode is a 0, which will continually draw power through the pull-up resistor.

Figure 4. EVENT_n Pin Mode Functionality



Serial Communications

The TSE2004GB2C0 includes a 4 Kbit serial EEPROM organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in one or more of the blocks of memory.

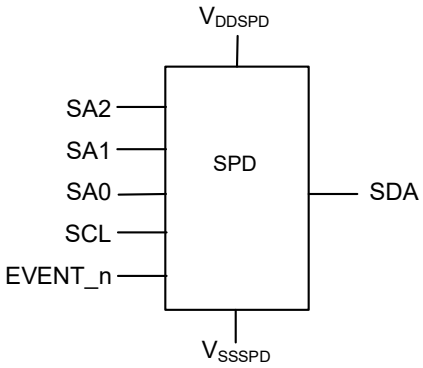
The TSE2004GB2C0 is protocol compatible with previous generation 2Kbit devices such as the TSE2002. The page selection method allows commands used with legacy devices such as TSE2002 to be applied to the lower or upper pages of the TSE2004GB2C0. In this way, the TSE2004GB2C0 may be used in legacy applications without software changes. Minor exceptions to this compatibility, such as elimination of the Permanent Write Protect feature are documented.

Individually locking a 128-byte block of the SPD may be accomplished using a software write protection mechanism in conjunction with a high input voltage VHV on input SA0. By sending the device a specific SMBus sequence, each block may be protected from writes until Write protection is electrically reversed using a separate SMBus sequence, which also requires VHV on input SA0. Write protection for all four blocks is cleared simultaneously, and Write protection may be reasserted after being cleared.

The Thermal Sensor (TS) section of the TSE2004GB2C0 continuously monitors the temperature, and updates the temperature data a minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device EVENT_n pin can be configured as *active high* or *active low,* and can be configured to operate as an interrupt or as a comparator output.

Figure 5. Device Diagram



Absolute Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
T_{STG}	Storage Temperature	-65	150	°C
V_{IO}	Input or Output Range, SA0	-0.50	10	V
	Input or Output Range, Other Pins	-0.50	4.3	V
V_{DDSPD}	Supply Voltage	-0.5	4.3	V

DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the *Measurement Conditions* summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 3. Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{DDSPD}	Supply Voltage	2.2	3.6	V
T_A	Ambient Operating Temperature	-40	+125	°C

Table 4. AC Measurement Conditions

Symbol	Parameter	Minimum	Maximum	Units
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V \times V_{DDSPD}$ to $0.8V \times V_{DDSPD}$		V
	Input and Output Timing Reference Levels	$0.3V \times V_{DDSPD}$ to $0.7V \times V_{DDSPD}$		V

Figure 6. AC Measurement I/O Waveform

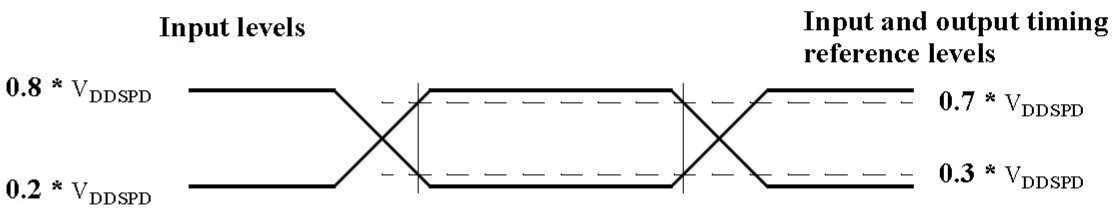


Table 5. Input Parameters

Symbol	Parameter[a] [b]		Test Condition	Minimum	Maximum	Units
C_{IN}	Input Capacitance	SDA			8	pF
C_{IN}	Input Rise and Fall Times				6	ns
Z_{EIL}	Ei Input Impedance	SA0,SA1,SA2	$V_{IN} < 0.3V \times V_{DDSPD}$	30		kΩ
Z_{EIH}	Ei input impedance	SA0,SA1,SA2	$V_{IN} > 0.7V \times V_{DDSPD}$	800		kΩ
t_{SP}	Pulse Width ignored (input filter on SCL and SDA)		Single glitch, f ≤100kHz			ns
			Single glitch, f >100kHz		50	ns

[a] T_A = 25°C, f = 400kHz.

[b] Verified by design and characterization, not necessarily tested on all devices.

DC Characteristics

Table 6. DC Characteristics

Symbol	Parameter		Conditions	f ≤400kHz		f >400kHz		Units
				Minimum	Maximum	Minimum	Maximum	
I_{LI}	Input Leakage Current	SCL, SDA	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}	—	±5	—	±5	µA
I_{LO}	Output Leakage Current		$V_{OUT} = V_{SSSPD}$ or V_{DDSPD}, SDA in Hi-Z	—	±5	—	±5	µA
I_{DD}	Supply Current		V_{DDSPD} = 3.3V, f_C = 100kHz (rise/fall time	—	2	—	2	mA
I_{DD1}	Standby Supply Current		$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 3.6V	—	100	—	100	µA
			$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 2.2V	—	100	—	100	µA
V_{IL}	Input Low Voltage	SCL, SDA	—	-0.5	0.3 × V_{DDSPD}	-0.5	0.3 × V_{DDSPD}	V
V_{IH}	Input High Voltage	SCL, SDA	—	0.7V × V_{DDSPD}	V_{DDSPD} +0.5	0.7V × V_{DDSPD}	V_{DDSPD} +0.5V	V
V_{HV}	SA0 High Voltage		VHV – V_{DDSPD} ≥4.8V	7	10	7	10	V
V_{OL1}	Output Low Voltage Open-drain or Open-collector		3mA sink current, V_{DDSPD} >2V	—	0.4	—	0.4	V
I_{OL}	LOW-level Output Current[a]		V_{OL} = 0.4V	3	—	20	—	mA
			V_{OL} = 0.6V	6		—	—	mA
V_{HYST}	Input Hysteresis		V_{DDSPD} ≥2V	0.05V × V_{DDSPD}	—	0.05V × V_{DDSPD}	—	V
V_{PON}	Power-on Reset Threshold		Monotonic rise between V_{PON} and V_{DDSPD}	1.6	—	1.6	—	V
V_{POFF}	Power Off Threshold for warm power-on cycle		No ring-back above V_{POFF}	—	0.9	—	0.9	V

[a] In order to drive a full bus load at 400kHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts not meeting this specification can still function but not at 400kHz and 400pF.

AC Characteristics

Table 7. AC Characteristics[a]

Symbol	Parameter	$V_{DDSPD} \geq 2.2V$				Units
		400kHz[b]		1000kHz		
		Minimum	Maximum	Minimum	Maximum	
f_{SCL}	Clock Frequency	10	400	10	1000	kHz
t_{HIGH}	Clock Pulse Width High Time	600	—	260	—	ns
t_{LOW}[c]	Clock Pulse Width Low Time	1300	—	500	—	ns
$t_{TIME-OUT}$[d] [e]	Detect Clock Low Timeout	25	35	25	35	ms
t_R[f] [g]	SDA Rise Time	20	300	—	120	ns
t_F[f] [g]	SDA Fall Time	20	300	—	120	ns
$t_{SU:DAT}$	Data In Setup Time	100	—	50	—	ns
$t_{HD:DI}$	Data In Hold Time	0	—	0	—	ns
$t_{HD:DAT}$	Data Out Hold Time	200	900	0	350	ns
$t_{HD:STA}$[h]	Start Condition Setup Time	600	—	260	—	ns
$t_{HD:STA}$	Start Condition Hold Time	600	—	260	—	ns
$t_{SU:STO}$	Stop Condition Setup Time	600	—	260	—	ns
t_{BUF}	Time between Stop Condition and next Start Condition	1300	—	500	—	ns
t_W	Write Time	—	5	—	5	ms
t_{POFF}	Warm Power Cycle Off Time	1	—	1	—	ms
t_{INIT}	Time from Power on to First Command	10	—	10	—	ms

[a] TSE devices are not required to support the I^2C Bus ALERT function.

[b] 400kHz timing defined for compatibility with TSE2002av applications.

[c] The TSE2004GB2C0 does not initiate clock stretching, which is an optional SMBus feature.

[d] The TSE2004GB2C0 supports bus time-out on EE access.

[e] Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, an embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically can reset its communications port after a start or a stop condition. A timeout condition can only be ensured if, the device that is forcing the timeout holds SCL low for $t_{IMEOUT,MAX}$ or longer.

[f] Guaranteed by design and characterization at 50°C, 3.6V. Not tested on all devices.

[g] To avoid spurious START and STOP conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.

[h] For a re-START condition, or following a write cycle.

Temperature-to-Digital Conversion Performance

Table 8. Temperature-to-Digital Conversion Performance

Parameter	Test Conditions[a]	Typical	Maximum	Unit
Temperature Sensor Accuracy (JEDEC B-grade)	75°C ≤ T_A ≤ 95°C, Active Range	±0.5	±1.0	°C
	40°C ≤ T_A ≤ 125°C, Monitor Range	±1.0	±2.0	°C
	-40°C ≤ T_A ≤ 125°C	±2.0	±3.0	°C
Resolution	—	0.0625	—	°C
Conversion Time[b]	Worse case conversion time	—	125	ms

[a] $V_{DDSPDMIN} \leq V_{DDSPD} \leq V_{DDSPDMAX}$

[b] Assuming 10-bit resolution.

Figure 7. AC Waveforms

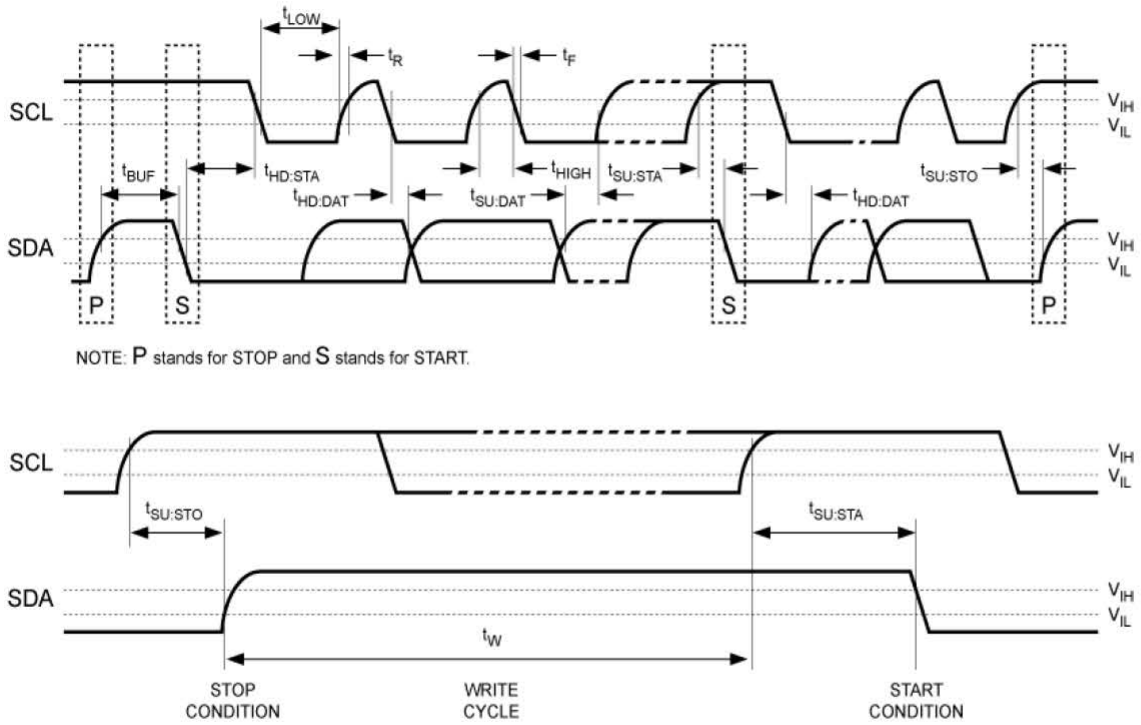
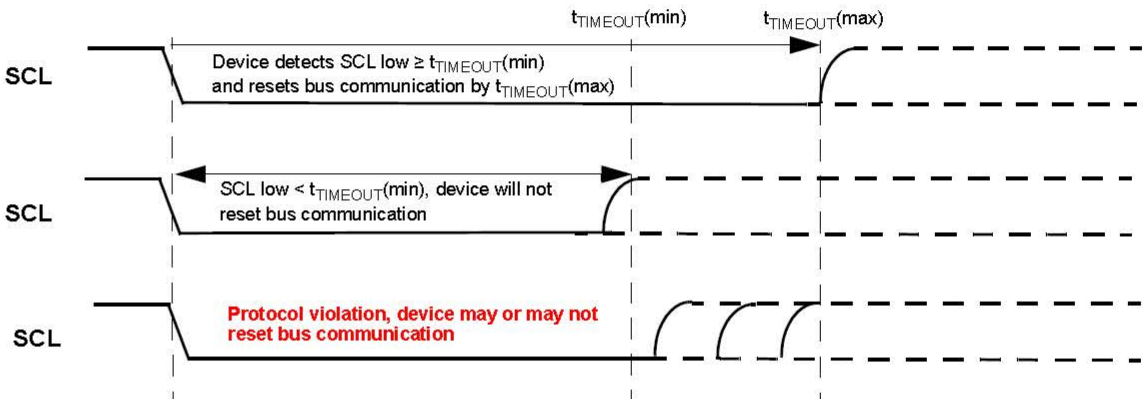


Figure 8. EE/TSE Bus Timeout Waveforms



Device Interface

The TSE2004GB2C0 functions as a slave device in the I^2C Bus protocol with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition generated by the bus master. The START condition is followed by a Device Select Code and R/W# bit (Table 9), and terminated by an acknowledge bit. The TSE2004GB2C0 does not initiate clock stretching, which is an optional I^2C Bus feature.

In accordance with the I^2C Bus definition, the device uses three built-in 4-bit Device Type Identifier Codes (DTIC), and the state of SA0, SA1, and SA2 to generate an I^2C Bus Slave Address. The SPD memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CSWP operations, a DTIC of (0110) is required. The TS registers are accessed using a DTIC of (0011).

Serial Address Selection

SA0, SA1, and SA2 inputs are directly combined with the DTIC and the EE page address bit to qualify SMBus addresses. Each of the SAx pins are tied to V_{DDSPD} or V_{SSSPD}, and the Logical Serial Address (LSA) is equal to the code on the Serial Address pins.

Table 9. I^2C Bus Addressing Modes[a]

Logical Serial Address (LSA)	SA2	SA1	SA0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1

[a] 0 = V_{SSSPD}, 1 = V_{DDSPD}.

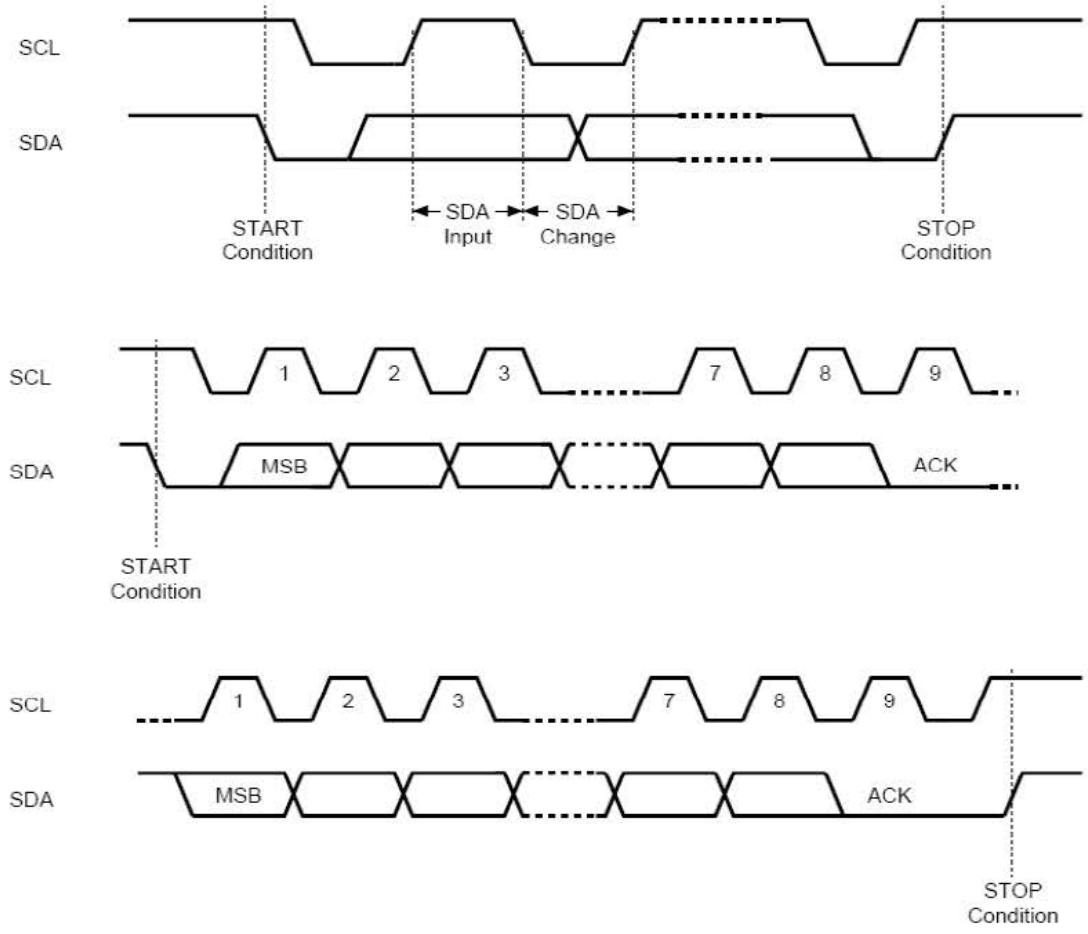
Interface Protocol

When writing data to the memory, the SPD inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ.

Violations of the command protocol result in an unpredictable operation.

The TS section of the device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/ write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received, starting first with the Most Significant Bit.

Figure 9. I²C Bus Protocol



Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA), while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the SPD into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the SPD. Neither of these conditions changes the operation of the TS section.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be the bus master or the slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

No Acknowledge Bit (NACK)

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following, the bus master sends the Device Select Code (Table 10) on Serial Data (SDA) most significant bit first).

Table 10. Device Select Code[a][b]

Function	Abbr[c]	Device Type Identifier[d]				Select Address[e][f]			R/W_n	SA0 Pin[g]
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Temperature Registers	RTR	0	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Temperature Registers	WTR								0	
Read EE Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, Block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, Block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, Block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, Block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, Block 0	RPS0					0	0	1	1	0, 1 or V_{HV}
Read Protection Status, Block 1	RPS1					1	0	0	1	0, 1 or V_{HV}
Read Protection Status, Block 2	RPS2					1	0	1	1	0, 1 or V_{HV}
Read Protection Status, Block 3	RPS3					0	0	0	1	0, 1 or V_{HV}
Set SPD Page Address to 0[h]	SPA0					1	1	0	0	0, 1 or V_{HV}
Set SPD Page Address to 1[h]	SPA1					1	1	1	0	0, 1 or V_{HV}
Read SPD Page Address[i]	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	—					All Other Encodings				

[a] Permanent Write Protect features for the TSE2002av has been eliminated from the TSE2004GB2C0.

[b] Don't Care values for word address and data fields following commands may result in Ack or No_Ack responses.

[c] For commands, SWPn, CWP, RPSn, SPAn, RPA (Figure 9).

[d] The most significant bit, b7, is sent first.

[e] Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins (Table 9).

[f] For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number.

[g] SA0 pin is driven to 0 = V_{SSSPD}, 1 = V_{DDSPD}, or VHV.

[h] Setting the EE page address to 0, selects the lower 256 bytes of EEPROM. Setting the EE page address to 1, selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.

[i] Reading the EE page address results in Ack, when the current page is 0, and NoAck, when the current page is 1.

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address. To address the EE memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings or EE page address, it is 0110b; and to access the Temperature Sensor settings is 0011b. Additionally, writing or clearing the reversible EE write protect requires SA0 be raised to the VHV voltage level.

Up to eight memory devices can be connected on a single I^2C Bus. Each one is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the SA pins SA0, SA1, and SA2 (Table 10). When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address.

Write Protection commands SWPn, CWP, and RPSn, and the EE Page Address commands SPAn and RPA, do not use the Select Address or Logical Serial Address, therefore, all devices on the I^2C Bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in-system applications.

The eighth bit is the Read/Write bit (R/W_n). This bit is set to 1 for Read, and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the ninth bit time. If the device does not match the EE Device Select code, the EE section deselects itself from the bus, and switches into Standby mode. The I^2C Bus operating modes are shown in Table 11.

I^2C Bus Operating Modes

Table 11. I^2C Bus Operating Modes

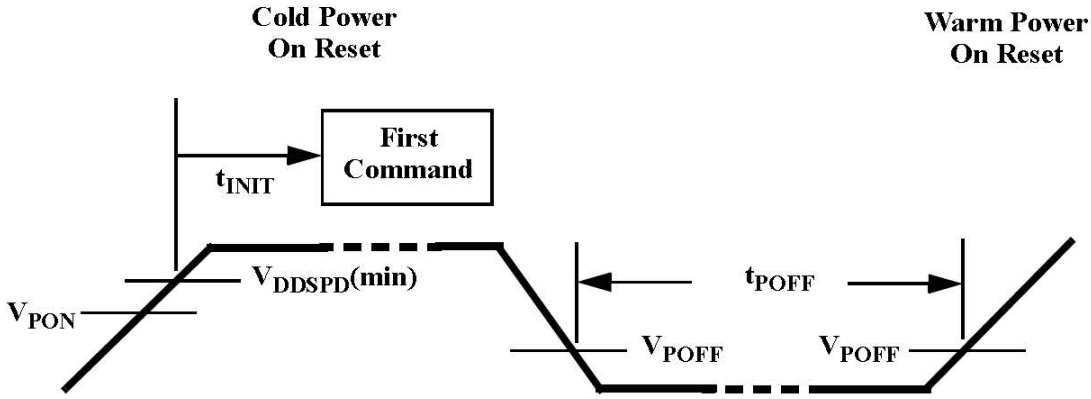
Mode	R/W_n Bit	Bytes	Initial Sequence
EE Current Address Read	1	1	START, Device Select, R/W_n = 1
EE Random Address Read	0	1	START, Device Select, R/W_n = 0, Address
	1		reSTART, Device Select, R/W_n = 1
EE Sequential Read	1	≥ 1	Similar to Current or Random Address Read
EE Byte Write	0	1	START, Device Select, R/W_n = 0, data, STOP
EE Page Write	0	≤ 16	START, Device Select, R/W_n = 0, data, STOP
TS Write	0	2	START, Device Select, R/W_n = 0, pointer, data, STOP
TS Read	1	2	START, Device Select, R/W_n = 1, pointer, data, STOP

Device Reset and Initialization

In order to prevent inadvertent Write operations during power-up, a Power-On Reset (POR) circuit is included. To ensure proper startup with cold power-on, V_{DDSPD} must rise monotonically between V_{PON} and $V_{DDSPD(min)}$. Once V_{DDSPD} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DDSPD} voltage must be applied, and no command may be issued to the device for t_{INIT}. This supply voltage must remain stable and valid until the end of the transmission of the instruction, and for a Write instruction, until the completion of the internal Write cycle (t_W).

Figure 10. Device Reset and Initialization



At power-down (phase during which V_{DDSPD} decreases continuously), when V_{DDSPD} drops immediately below the minimum operating voltage, the device stops responding to commands. On warm power cycling for t_{POFF}, V_{DDSPD} must remain below V_{POFF}, and must meet cold power-on reset timing when restoring power.

The device is delivered with all bits in the EEPROM memory array when set to 1 (each byte contains 0xFF).

Software Write Protect

The TSE2004GB2C0 has three software commands for setting, clearing, or interrogating the Write-protection status.

Software write-protection is handled by three instructions:

1. SWPn: Set Write Protection for Block n
2. CWP: Clear Write Protection for all Blocks
3. RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block can be independently protected. The memory blocks are:

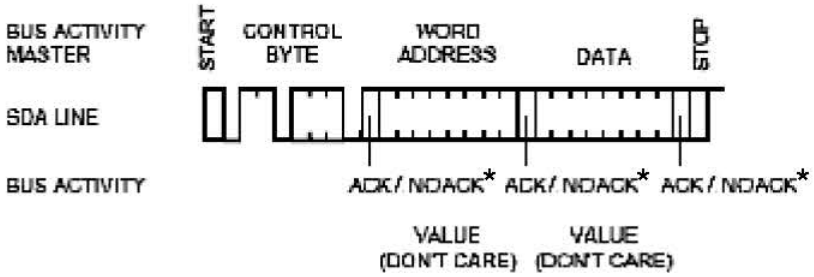
- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of Write-protection (set or cleared) which has been defined using these instructions, will remain defined even after a power cycle.

SWPn and CWP: Set and Clear Write Protection

If the software Write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.

Figure 11. Protocol for Write Protection Commands SWPn, CWP, RPSn



RPSn: Read Protection Status

The controller issues a RPSn command specifying which block to report upon. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If the Software Write Protection has been set, the device replies to the data byte with a NoAck.

SPAn: Set SPD Page Address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the SPD Page Address is always 0, selecting the lower 256 bytes

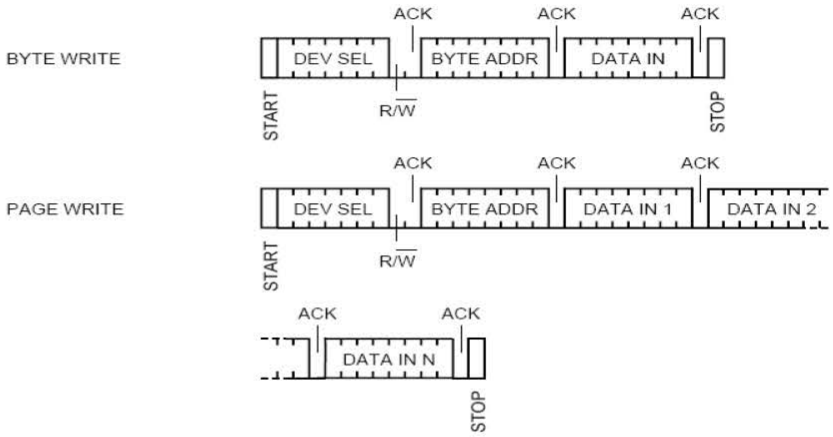
RPA: Read SPD Page Address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

Write Operations

Following a Start condition, the bus master sends a Device Select Code with the R/W_n bit reset to 0. The device acknowledges this (Figure 12), and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

Figure 12. Write Mode Sequences in a Non-Write Protected Area



When the bus master generates a Stop condition immediately after the Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored by the EE, and the EE device does not respond to any requests. Access to the TS portion of the TSE2004GB2C0 is permitted during this period.

The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. After the byte is transferred, the internal byte address counter is incremented unless the block is write protected. The bus master terminates the transfer by generating a Stop condition (Figure 12).

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

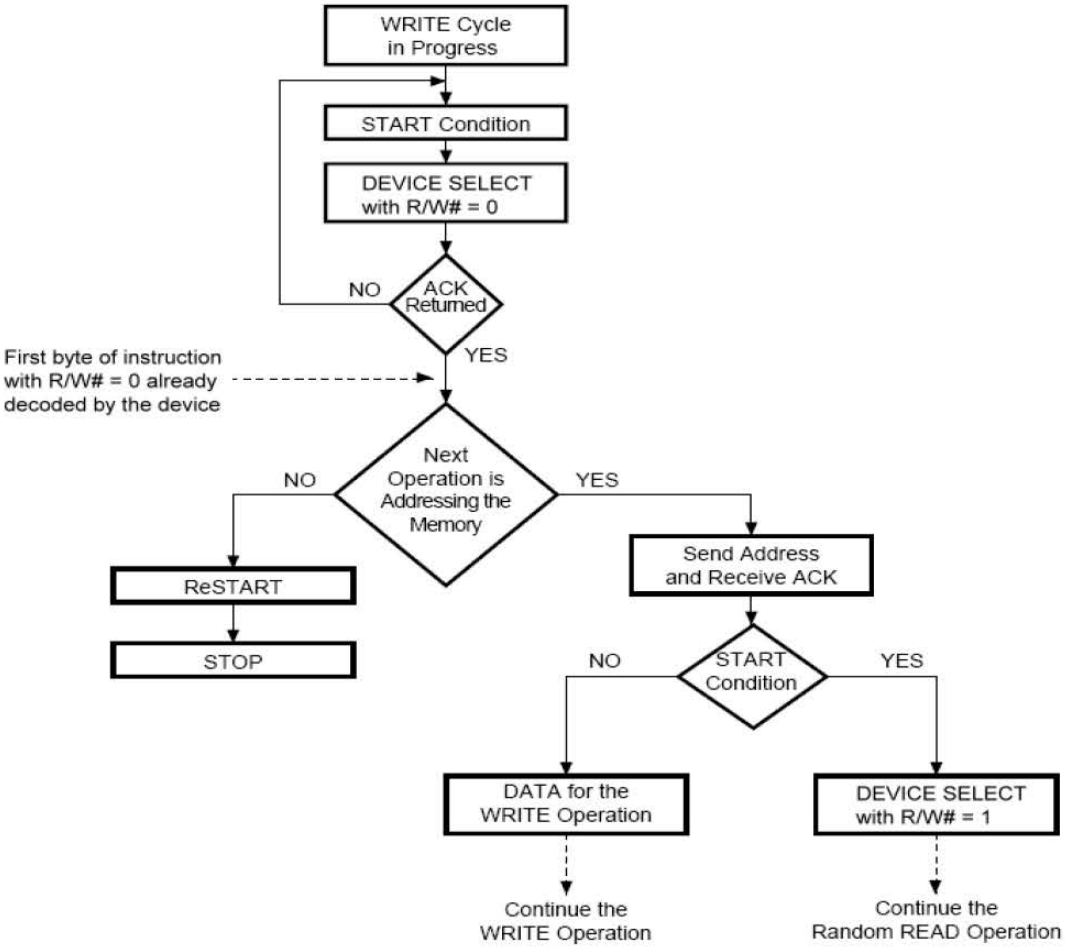
Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in theTSE2004GB2C0 AC Characteristic table, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The polling sequence is shown in Figure 13:

- Initial condition: a Write cycle is in progress.
  - Step 1: The bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
  - Step 2: If the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

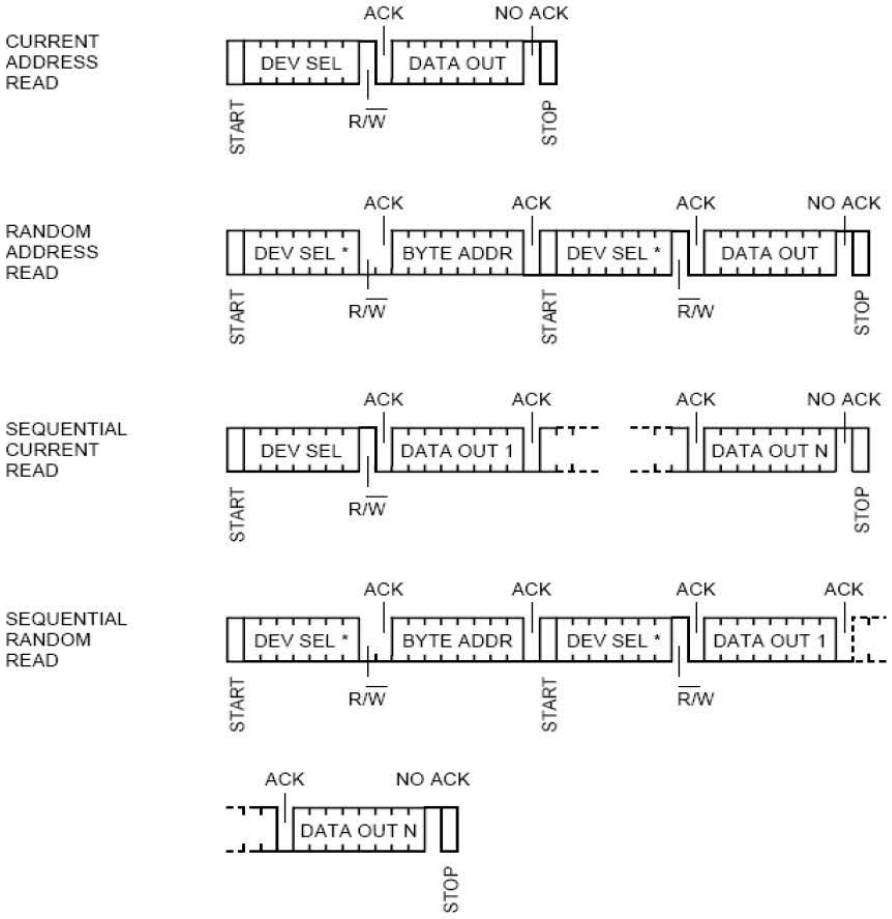
Figure 13. Write Cycle Polling Flowchart Using ACK



Read Operations

Read operations are performed independent of the software protection state. The device has an internal address counter which is incremented each time a byte is read.

Figure 14. Read Mode Sequences



Random Address Read

A dummy Write is first performed to load the address into this address counter (Figure 14), but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/W_n bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/W_n bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition (Figure 14), without acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition (Figure 14). The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

Acknowledge in Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status.

Table 12. Acknowledge when Writing Data or Defining Write Protection (R/W_n Bit = 0)

Status	Instruction	ACK	Address	ACK	Data Byte	ACK	Write Cycle (t_W)
Protected with SWP	SWPn	NoACK	Not Significant	NoACK	Not Significant	NoACK	No
	CWP	ACK	Not Significant	ACK	Not Significant	ACK	Yes
	Page or byte write in protected block	ACK	Address	ACK	Data	NoACK	No
Not Protected	SWPn, or CWP	ACK	Not Significant	ACK	Not Significant	ACK	Yes
	Page or byte write	ACK	Address	ACK	Data	ACK	Yes

Table 13. Acknowledge When Reading the Protection Status (R/W_n Bit = 1)

SWPn Status	Instruction	ACK	Address	ACK	Data Byte	ACK
Set	RPSn	NoACK	Not Significant	NoACK	Not Significant	NoACK
Not Set	RPSn	ACK	Not Significant	NoACK	Not Significant	NoACK

Temperature Sensor (TS) Device Operation

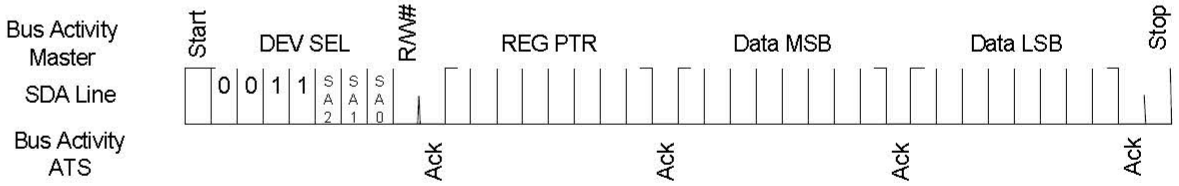
The TSE2004GB2C0 Temperature Register Set is accessed through the I^2C Bus address 0011_bbb_R/W_n. The “bbb” denotes the Logical Serial Address code (LSA). In the event SA0 is in the high voltage state, the device does not recognize the LSA. The Temperature Register Set stores the temperature data, limits, and configuration values. All registers in the address space from 0x00 through 0x08 are 16-bit registers accessed through block read and write commands (Write Operations).

Behavior on accesses to invalid register locations is vendor-specific, and may return an Ack or a NoAck.

Write Operations

Writing to the TSE2004GB2C0 Temperature Register Set is accomplished through a modified block write operation for two data bytes. To maintain I^2C Bus compatibility, the 16 bit register is accessed through a pointer register, requiring the write sequence to include an address pointer in addition to the Slave address. This indicates the storage location for the next two bytes received. Figure 15 shows an entire write transaction on the bus.

Figure 15. TS Register Write Operation



Read Operations

Reading data from the TS may be accomplished in one of two ways:

1. If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a Slave Address from the bus master followed by two bytes of data from the device; or
2. The pointer register is loaded with the correct register address, and the data is read. The sequence to preset the pointer register is shown in Figure 16, and the preset pointer read is shown in Figure 17. If it is desired to read random address each cycle, the complete Pointer Write, Word Read sequence is shown in Figure 18.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (No Ack) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

Figure 16. I^2C Write to Pointer Register

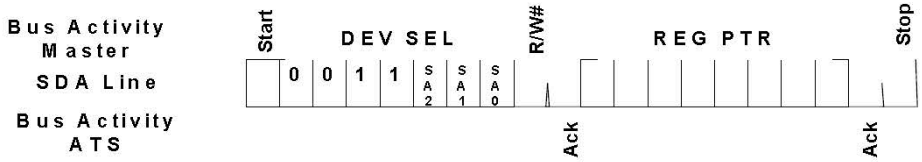


Figure 17. I^2C Preset Pointer Register Word Read

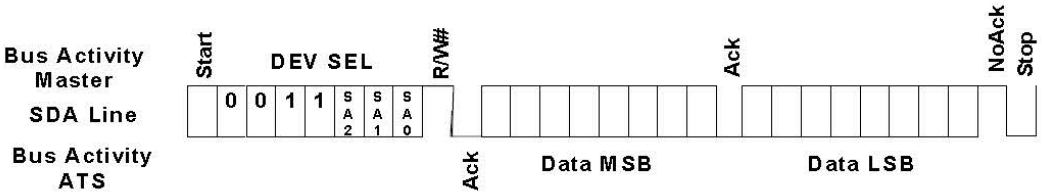
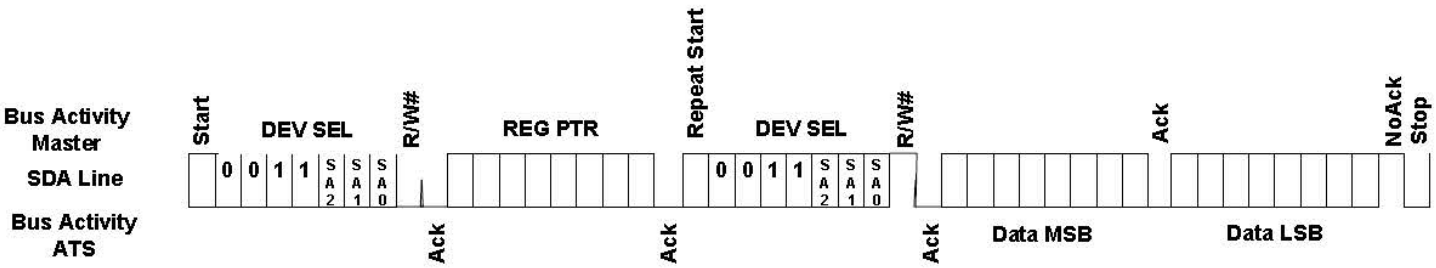


Figure 18. I^2C Pointer Write Register Word Read



Device Registers

The register set address is shown in Table 12. These values also used in the I^2C Bus operations as the “REG_PTR”.

Table 14. Device Registers

ADDR	R/W	Name	Function	Default
N/A	W	Address Pointer	Address storage for subsequent operations	N/A
00	R	Capabilities	Indicates the functions and capabilities of the temperature sensor	00ff
01	R/W	Configuration	Controls the operation of the temperature monitor	0000
02	R/W	High Limit	Temperature High Limit	0000
03	R/W	Low Limit	Temperature Low Limit	0000
04	R/W	TCRIT Limit	Critical Temperature	0000
05	R	Ambient Temperature	Current Ambient temperature	N/A
06	R	Manufacturer ID	manufacturer ID	00b3
07	R	Device/Revision	Device ID and Revision number	2215
08	R/W	Vendor Defined	Change resolution of temperature sensor	0018
09–0F	R/W	ADDR	Vendor specific information	N/A

Capabilities Register

The Capabilities Register indicates the supported features of the temperature sensor.

Table 15. Capabilities Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	00ff
		EVSD	TMOUT	VHV	TRES[1:0]		RANGE	ACC	EVENT	

- Bits 15 through Bit 8: RFU – Reserved for future use. These bits will always read 0 and writing to them will have no affect.
- Bit 7: EVSD – EVENT_n with shutdown action. Must be 1.
  - 0: Not used.
  - 1: The EVENT_n output is deasserted (not driven) when entering shutdown and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode. In interrupt mode, EVENT_n may or may not be asserted when exiting shutdown if a pending interrupt has not been cleared.
- Bit 6: TMOUT is a bus timeout period for thermal sensor access during normal operation.
  - 0: Not used.
  - 1 (default): Parameter $t_{TIMEOUT}$ is supported within the range of 25ms to 35ms (SMBus compatible).
- Bit 5: VHV
  - 0: Not used
  - 1: Defined for compatibility with TS3000 devices. Since all TSE2004av devices are required to support VHV, this bit is not used.
- Bits 4 through 3: TRES[1:0] – Indicates the resolution of the temperature monitor (default = 11), (Table 16).

Table 16. TRES Bit Decode

TRES[1:0][a]		Temperature Resolution
1	0	
0	0	0.5°C (9-bit)
0	1	0.25°C (10-bit)
1	0	0.125°C (11-bit)
1	1	0.0625°C (12-bit) (default)

[a] See Table 26.

- Bit 2: RANGE – Indicates the supported temperature range.
- 0: The temperature monitor clamp values lower than 0°C.
- 1 (default): The temperature monitor can read temperatures below 0°C, and sets the sign bit appropriately.
- Bit 1: ACC indicates the supported temperature accuracy.
  - 0: Not used
  - 1 (default): Bgrade. The temperature monitor has ±1°C accuracy over the active range (75°C to 95°C) and 2°C accuracy over the monitoring range (40°C to 125°C).
- Bit 0: EVENT – Indicates whether the temperature monitor supports interrupt capabilities.
  - 0: Not used.
  - 1 (default): The device supports interrupt capabilities.

Configuration Register

Table 17. Configuration Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
01	R/W	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	0000
		TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE	

The Configuration Register holds the control and status bits of the EVENT_n "T" pin, as well as general hysteresis on all limits. To avoid glitches on the EVENT_n output, disable the EVENT or TCRIT functions prior to programming or changing other device configuration settings.

- Bits 15 through 11: RFU – Reserved for future use. These bits will always read 0 and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as 0.
- Bits 10 through 9: HYST[1:0] – Controls the hysteresis that is applied to all limits (Table 18). This hysteresis applies to all limits when the temperature is dropping below the threshold. Once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to the EVENT_n pin functionality. When either of the lock bits are set, these bits cannot be altered.

Table 18. HYST Bit Decode

HYST[1:0]		Hysteresis
1	0	
0	0	Disable hysteresis (default)
0	1	1.5°C
1	0	3°C
1	1	6°C

- Bit 8: SHDN (Shutdown) – The thermal sensing device and A/D converters are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the TSE2004GB2C0 still responds to commands normally, however bus timeout may or may not be supported in this mode.
  - 0 (default): The temperature monitor is active and converting
  - 1: The temperature monitor is disabled and will not generate interrupts or update the temperature data.
- Bit 7: TCRIT_LOCK. Locks the TCRIT Limit Register from being updated.
  - 0 (default): The TCRIT Limit Register can be updated normally.
  - 1: The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.
- Bit 6: EVENT_LOCK – Locks the High and Low Limit Registers from being updated.
  - 0: (default – The High and Low Limit Registers can be updated normally.
  - 1: The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.
- Bit 5: CLEAR – Clears the EVENT_n pin when it has been asserted. This bit is write only and will always read 0.
  - 0: does nothing
  - 1: The EVENT_n pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

- Bit 4: EVENT_STS – Indicates if the EVENT_n pin is asserted. This bit is read only.
  - 0 (default): The EVENT_n pin is not asserted.
  - 1: The EVENT_n pin is being asserted by the device.
- Bit 3: EVENT_CTRL – Masks the EVENT_n pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.
  - 0 (default): The EVENT_n pin is disabled and will not generate interrupts.
  - 1: The EVENT_n pin is enabled.
- Bit 2: TCRIT_ONLY – Controls whether the EVENT_n pin will be asserted from a high or low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.
  - 0 (default): The EVENT_n pin will be asserted if the measured temperature is above the High Limit or below the Low Limit, in addition to, if the temperature is above the TCRIT Limit.
  - 1: The EVENT_n pin will only be asserted if the measured temperature is above the TCRIT Limit.
- Bit 1: EVENT_POL – Controls the *active* state of the EVENT_n pin. The EVENT_n pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.
  - 0 (default): The EVENT_n pin is active low. The “active” state of the pin will be logical 0.
  - 1: The EVENT_n pin is active high. The *active* state of the pin will be logical 1.
- Bit 0: EVENT_MODE – Controls the behavior of the EVENT_n pin. The EVENT_n pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.
  - 0: The EVENT_n pin will function in comparator mode.
  - 1: The EVENT_n pin will function in interrupt mode.

Temperature Register Value Definitions

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B12 through B2 for each of these registers, are defined for all device resolutions as defined in the TRES field of the Capabilities Register, a 0.25°C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits:

Table 19. Temperature Register Coding Examples

Temperature Register Coding Examples		
B15~B0 (binary)	**Value**	**Units**
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	-0.25	°C
xxx1 1111 1111 00xx	-1.00	°C
xxx1 1111 1101 01xx	-2.75	°C

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or EVENT_n pin changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1:0] = 10) or all 12 bits (TRES[1:0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1:0] = 00), the finest resolution supported is 0.5°C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

High Limit Register

The temperature limit registers (High, Low, and TCRIT) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits '-' must be programmed as 0.

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set (Table 17), then this register becomes read-only.

Table 20. High Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
02	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

Low Limit Register

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set as shown in Table 17 then this register becomes read-only.

Table 21. Low Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
03	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

TCRIT Limit Register

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the EVENT_n pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set as shown in Table 17 then this register becomes read-only.

Table 22. TCRIT Limit Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
04	R/W	–	–	–	Sign	128	64	32	16	0000
		8	4	2	1	0.5	0.25	–	–	

Temperature Data Register

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement, as well as the status bits indicating which error conditions, if any, are active. The encoding of bits B12 through B0 is the same as for the temperature limit registers.

Table 23. Temperature Data Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	N/A (0000)
		8	4	2	1	0.5	0.25[a]	0.125[a]	0.0625[a]	

[a] Resolution defined based on value of TRES field of the Capabilities Register. Unused/unsupported bits will read as 0.

Bit 15: TCRIT – When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT, and will automatically clear once the temperature has dropped below the limit minus the hysteresis.

Bit 14: HIGH – When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the High Limit minus the hysteresis.

Bit 13: LOW – When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.

Manufacturer ID Register

The Manufacturer ID Register holds the PCI SIG number assigned to the specific manufacturer.

Table 24. Manufacturer ID Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
06	R/W	0	0	0	0	0	0	0	0	00B3
		1	0	1	1	0	0	1	1	

Device ID/Revision Register

The upper byte of the Device ID / Revision Register stores a unique number indicating the TSE2004GB2C0 from other devices. The lower byte holds the revision value.

Table 25. Device ID/Revision Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
07	R/W	0	0	1	0	0	0	1	0	2215
		0	0	0	1	0	1	0	1	

Resolution Register

This register allows the user to change the resolution of the temperature sensor. The POR default resolution is 0.0625°C. The resolution implemented via this register is also reflected in the capability register.

Table 26. Resolution Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
08h	R/W	0	0	0	0	0	0	0	0	0018
		0	0	0	TRES[1]	TRES[0]	0	0	0	

Legend

Resolution bits 4:3, TRES[4:3]:

- 00 = LSB = 0.5°C (register value = 0007)
- 01 = LSB = 0.25°C (register value = 000F)
- 10 = LSB = 0.125°C (register value = 0017)
- 11 = LSB = 0.0625°C (register value = 001F)

Use in a Memory Module

In the Dual Inline Memory Module (DIMM) application, the TSE2004GB2C0 is soldered directly onto the printed circuit module. The three select address inputs (SA0, SA1, SA2) must be connected to V_{SSSPD} or V_{DDSPD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (Table 27). Pull-up resistors are required for normal behavior, and are connected to the I^2C Bus signals on the motherboard.

Table 27. Unique Addressing of SPDs in DIMM Applications[a]

DIMM Position	SA2	SA1	SA0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

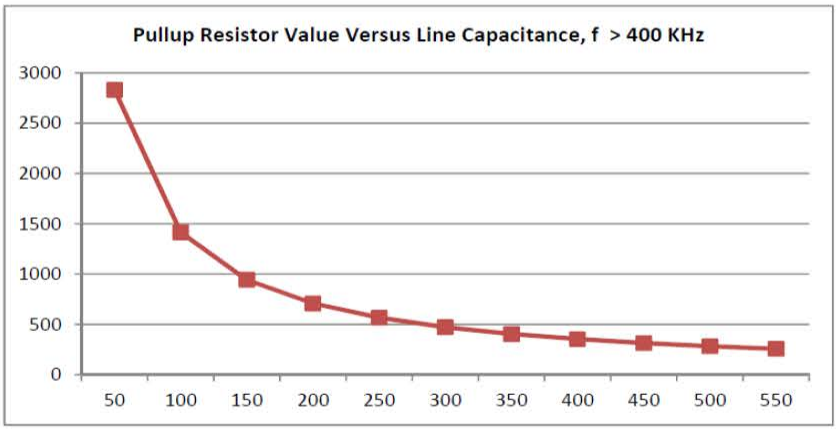
[a] 0 = V_{SSSPD}, 1 = V_{DDSPD}.

The Event_n pin is expected to be used in a wire-OR configuration with a pull-up resistor to V_{DDSPD} on the motherboard. In this configuration, EVENT_n should be programmed for the active low mode. Also note, the comparator mode or TCRIT-only mode for EVENT_n on a wire-OR bus, will show the combined results of all devices wired to the EVENT_n signal.

In DIMM applications, maximum external pull-up resistors on signals are specified based on Figure 3, “Maximum RL Value Versus Bus Capacitance (CBUS) for an I^2C Bus”. Line capacitance limitations should be calculated using this assumption.

Figure 19. Pull-up Resistor Value

Cap	Res
50 pF	2833 Ω
100 pF	1416 Ω
150 pF	944 Ω
200 pF	708 Ω
250 pF	567 Ω
300 pF	472 Ω
350 pF	405 Ω
400 pF	354 Ω
450 pF	315 Ω
500 pF	283 Ω
550 pF	258 Ω



Programming the TSE2004GB2C0

The situations in which the TSE2004GB2C0 is programmed, can be considered under two headings:

1. When the DIMM is isolated (not inserted on the PCB motherboard)
2. When the DIMM is inserted on the PCB motherboard

DIMM Isolated

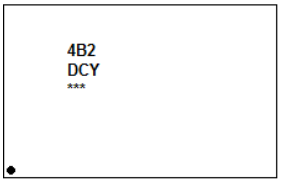
With specific programming equipment, it is possible to define the TSE2004GB2C0 content, using Byte and Page Write instructions, and its write-protection using the SWPn and CWP instructions. To issue the SWPn and CWP instructions, the DIMM must be inserted in the application-specific slot where the SA0 signal can be driven to VHV during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the protected bytes, and finally to set the write-protection with the SWPn instruction.

In DIMM Isolation usage, the Read Protection Status (RPSn), Set EE Page Address (SPAn), and Read EE Page Address (RPA) commands are fully supported.

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



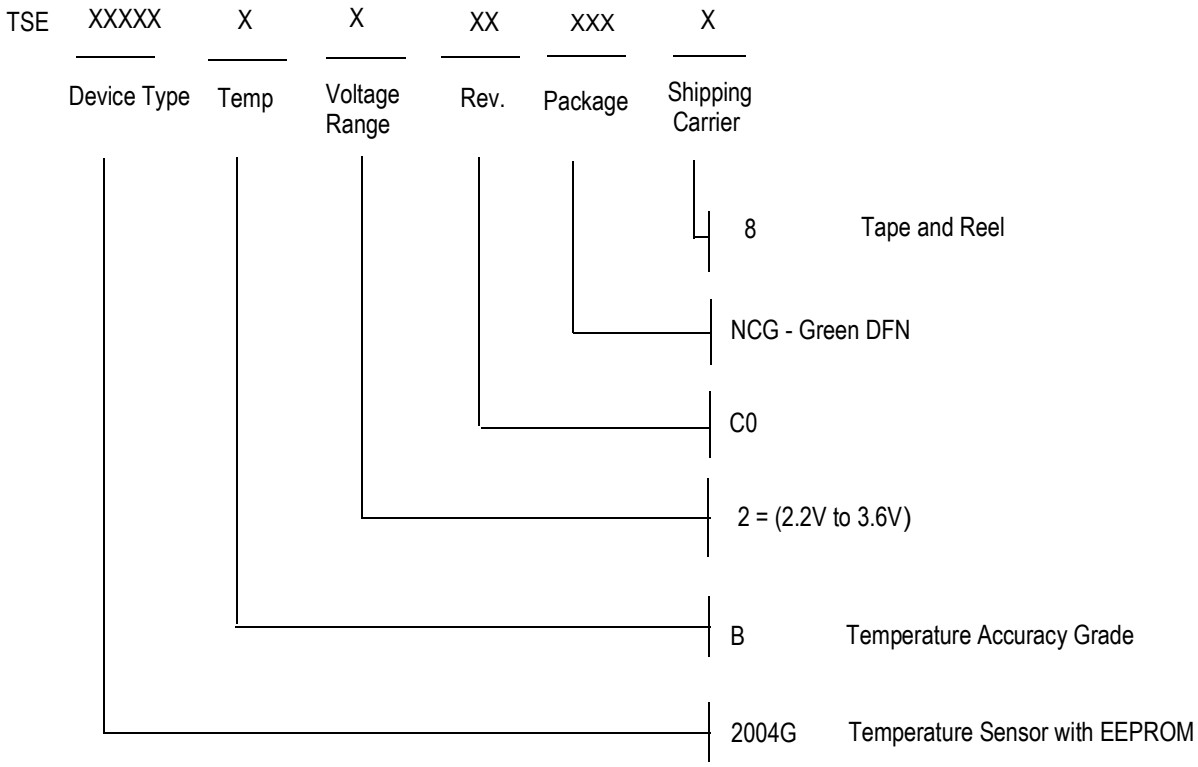
Line 1. Line 1 is the truncated part number/ Product Description.

Line 2. DCY denotes Produce Description + Y, where Y = last digit of year assembled.

Line 3. "***" denotes sequential lot number characters from AAA to ZZZ.

Ordering Information

Part Number	Package	Carrier Type	Temperature Range
TSE2004GB2C0NCG	8-DFN, 2.0 × 3.0 × 0.75 mm	Tray	-40° to +125°C
TSE2004GB2C0NCG8		Tape and Reel	-40° to +125°C



Reference

JEDEC Standard No. 21-C, Release 26, modified February 3, 2016;

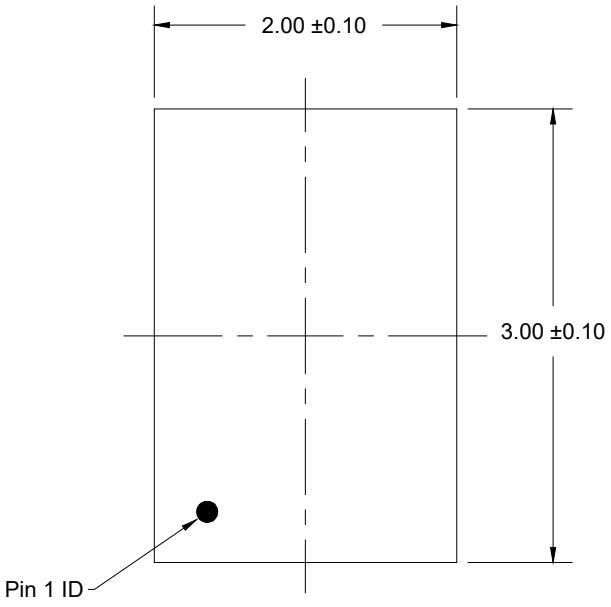
Section 4.1.6 Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 KBit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications.

Revision History

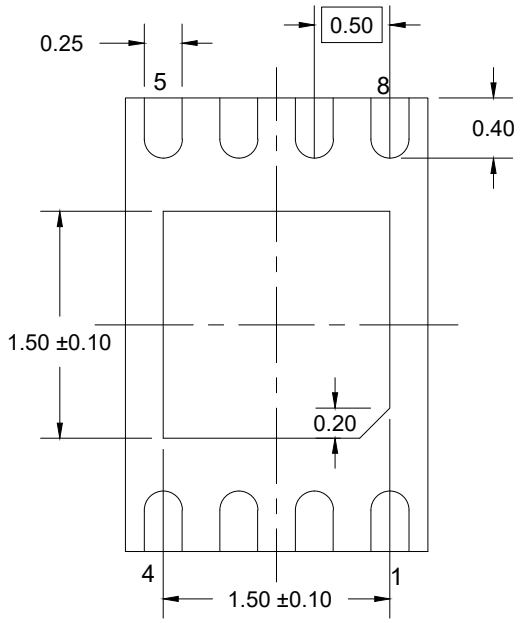
Revision Date	Description of Change
December 14, 2022	▪ Corrected the package link in Ordering Information; no technical changes
May 10, 2018	▪ Updated t_{SP} symbol in Table 5 ▪ Removed several functions from Table 10 ▪ Updated the Package Outline Drawings; however, no technical changes ▪ Completed other minor changes
October 23, 2017	Updated the operating temperature values in Ordering Information
September 14, 2017	▪ Added reference to JEDEC com pliancy in Features ▪ Updated the package outline drawings; however, no mechanical changes ▪ Completed numerous minor changes
May 15, 2017	Table 25 - corrected units for I_{LI}, I_{LO}, I_{DD1} rows.
May 2, 2017	Initial release.

Package Outline Drawing

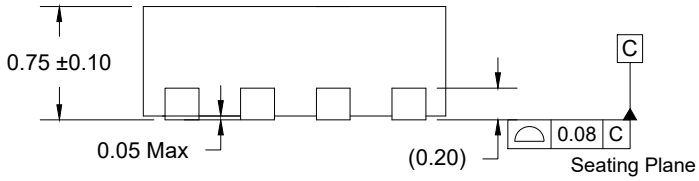
Package Code: NCG8P1
8-DFN 2.0 x 3.0 x 0.75 mm Body, 0.5mm Pitch
PSC-4244-01, Revision: 05, Date Created: Jul 29, 2022



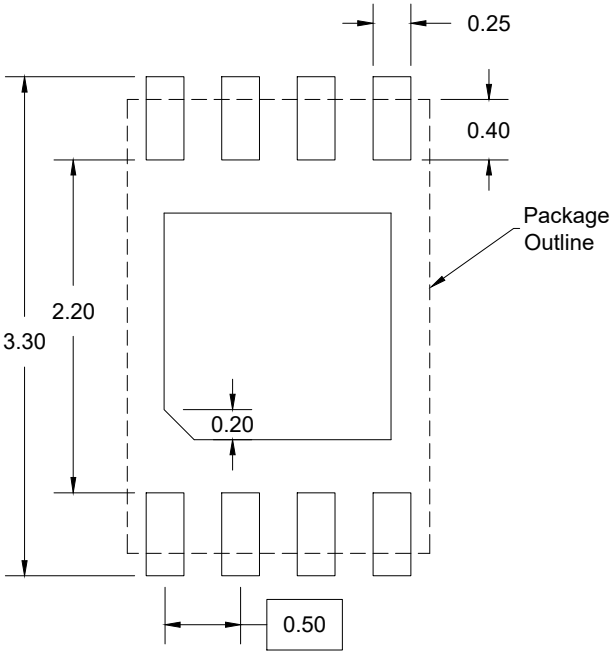
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for reference only.

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