USB-C Controller + Power Switch with HV Protection

General Description

The RT9752 is a USB Type-C Downstream Facing Port (DFP) controller with back to back power switch which offers 28V tolerance on VOUT pin at off state and 3A rated supply current for VBUS for USB Type-C applications. The RT9752 have Configuration Channel (CC) function to determine when USB device is attached. If the Upstream Facing Port (UFP) is attached using an E-marked cable, the RT9752 also applies power to VBUS and VCONN power to the cable CC pin. The RT9752 also identifies when Type-C audio or debug accessories are attached. Reverse voltage protection is provided to prevent reverse current flowing back to input power supply in a power source swap application.

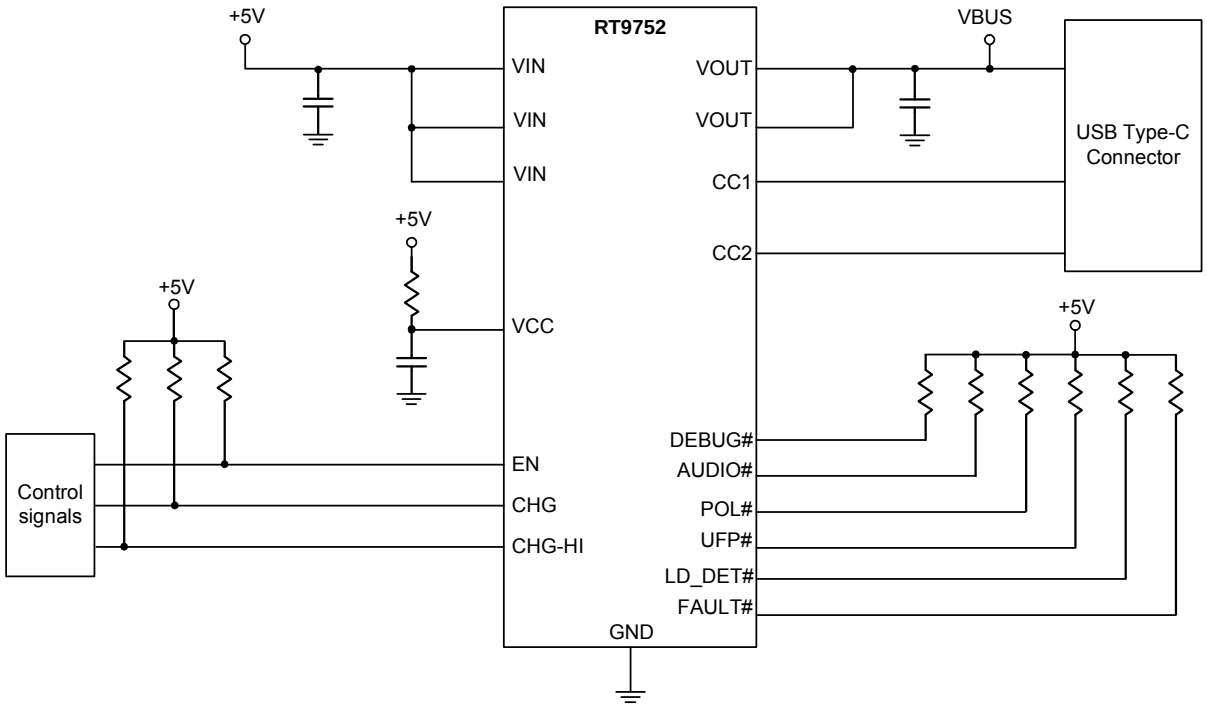
Features

- **USB Type-C Compliant DFP Controller**
- **Standard USB/1.5A/3A Capability Advertisement on CC**
- **VBUS Application and Discharge**
- **VCONN Application to Electronically Marked Cable**
- **VIN Supply Voltage Range from 4.5V to 5.5V**
- **Reverse Voltage Protection with Ultra Fast RVP Recovery**
- **Low On-Resistance of the Power FETs**
- **Programmable Current Limit Level**
- **High Reliability of High Voltage Power Switch**
- **UL Approved-E219878**
- **Nemko Approved-NO110026**

Applications

- Type-C USB Chargers
- PC Products Base on Type-C Host Port

Simplified Application Circuit



Ordering Information

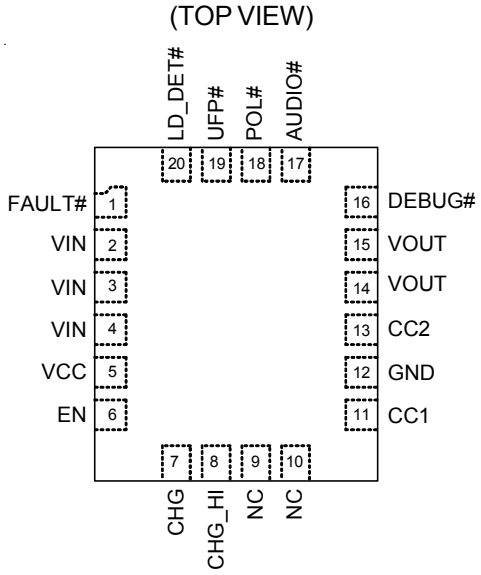
Version	Discharge Function	EN Function		Marking Information	Package Type
		Active High	Active Low		
RT9752AGQWF	Yes	V		0B=	WQFN-20TL 3x4 (FC)
RT9752BGQWF	Yes		V	0A=	
RT9752ANGQWF	No	V		0D=	
RT9752BNGQWF	No		V	0C=	

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

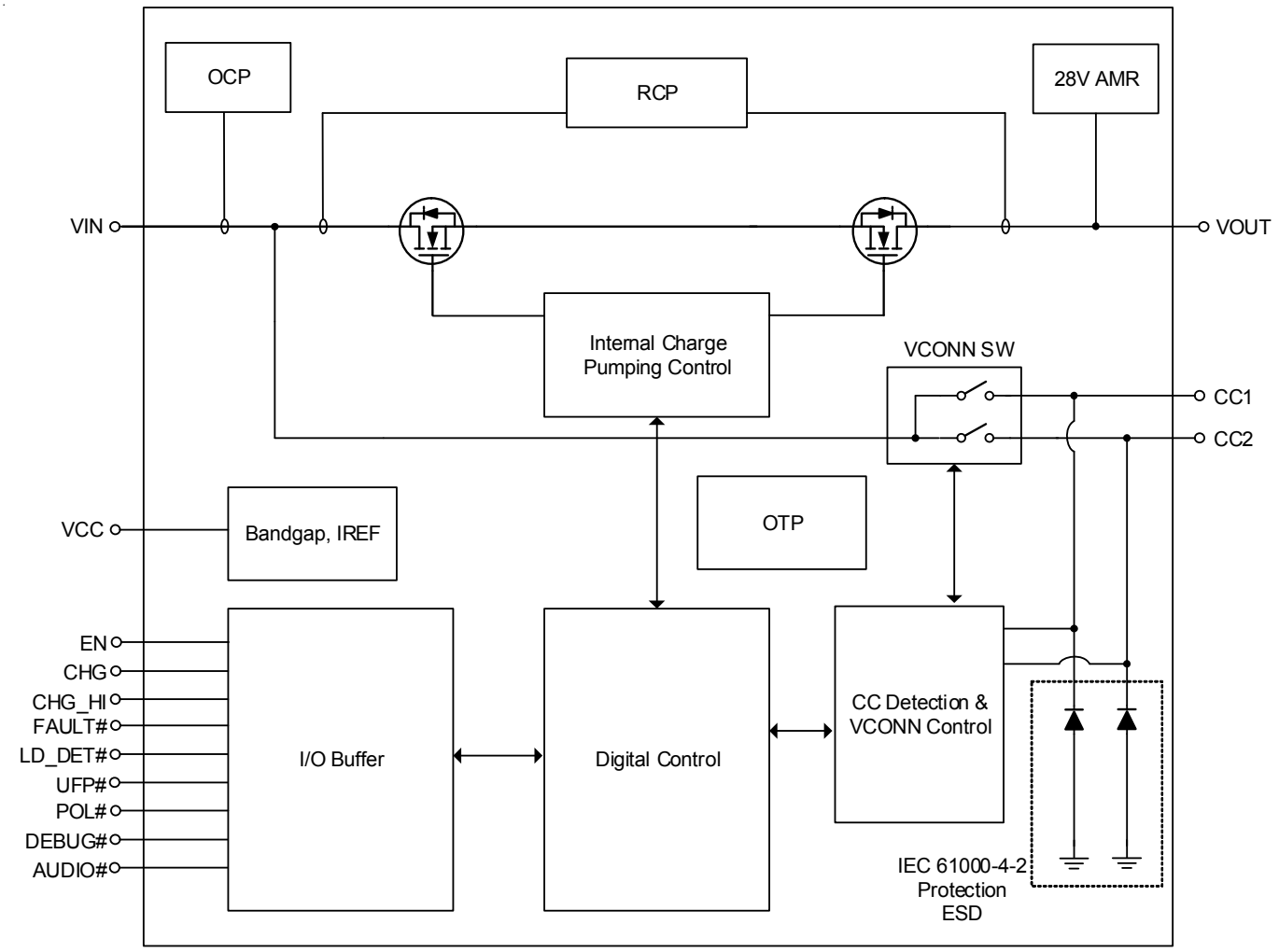


WQFN-20TL 3x4 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FAULT#	Fault event indicator. Open-drain logic output that asserts low to indicate current limit or thermal shutdown event due to over temperature, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
2, 3, 4	VIN	Input power for VBUS and VCONN.
5	VCC	Bias voltage for control logic. The bias voltage of VCC should be tied to same voltage source of VIN pin (5V). For avoiding noise disturbance, the supplied bias voltage must be stable, Beside, a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to VCC pin is necessary which should be placed as close as physically possible to VCC pin.
6	EN	Enable control input pin (Active High). If the voltage of EN pin is risen higher than 1.15V, the RT9752 is ready to work. If the voltage of EN pin falls below its falling 0.65V, the RT9752 is shut down.
7	CHG	Charge logic input for standard USB (2.0/3.0) or Type-C selection.
8	CHG_HI	High-charge logic input for current sourcing capability selection (1.5A/3A) of Type-C.
9	NC	No internal connection.
10	NC	No internal connection.
11	CC1	Connect to Type-C receptacle CC pin. Suggest to place a equal-value output capacitor 22μF (25V/1206/X5R) as close to the CC1 and GND pins as possible.
12	GND	Ground pin. Directly solder to the large PGND plane and use thermal vias to connect PGND of other layers for thermal resistor reduction.
13	CC2	Connect to Type-C receptacle CC pin. Suggest to place a equal-value output capacitor 22μF (25V/1206/X5R) as close to the CC2 and GND pins as possible.
14, 15	OUT	Power switch output VBUS.
16	DEBUG#	Open-drain logic output. It asserts when entry Type-C Debug accessory mode, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
17	AUDIO#	Open-drain logic output. It asserts when entry Type-C Audio accessory mode, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
18	POL#	Polarity open-drain logic output that signals which Type-C CC pin is connected to the CC line, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
19	UFP#	Open-drain logic output. It asserts when entry Type-C UFP mode, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
20	LD_DET#	Load-detect open-drain logic output. It asserts when set to source Type-C 3A current, and VBUS is sourcing over 1.8 A nominal, In which the pull-up resistor is recommended from 10kΩ to 100kΩ.

Functional Block Diagram



Operation

Supply Power

The RT9752 has two input power pins; VIN and VCC. VIN is the power source connection to the VOUT, CC1 and CC2 through the power FETs inside chip for VBUS, VCONN with the Type-C charging current. VCC supply provides power to internal circuits in the chip.

Enable and Disable

The RT9752 includes an EN pin for sequence control (independent control). If the voltage of EN pin rises above rising threshold, the device is turned on or enabled. On the contrary, the RT9752 is shut down when the voltage of EN pin falls below its falling threshold.

Under-Voltage Lockout

A voltage-sense circuit monitors the input voltage. When the input voltage VIN is above 4V, UVLO turns on the MOSFET switch if CC pins configured the UFP device attached.

USB Type-C DFP Output Control

The RT9752 is a DFP Type-C port controller with integrated power switch for VCONN and VBUS. The RT9752 output for VBUS or VCONN supply decided by CC1 and CC2 pin configuration defined by USB Type-C standard. Table 1 lists the RT9752 output response to various port attachments.

Table 1. RT9752 Output with Port Configuration

RT9752 Type-C Port Configuration	CC1	CC2	RT9752 Output	
			VOUT	VCONN Supply
Nothing Attached	OPEN	OPEN	OPEN	NO
UFP Connected	Rd	OPEN	VIN	NO
	OPEN	Rd	VIN	NO
Powered Cable without UFP Connected	OPEN	Ra	OPEN	NO
	Ra	OPEN	OPEN	NO
Powered Cable with UFP Connected	Rd	Ra	VIN	CC2
	Ra	Rd	VIN	CC1
Debug Accessory Connected	Rd	Rd	VIN	NO
Audio Accessory Connected	Ra	Ra	OPEN	NO

The Rd and Ra impedance can refer to Universal Serial Bus Type-C Cable and Connector Specification.

Table 2. CC Termination (Rd) Requirements

Rd Implementation	Nominal Value	Max Voltage On Pin
+-20% resistor to GND	5.1kΩ	2.18V

Table 3. CC Termination (Ra) Requirements

Ra Implementation	Minimum Impedance	Maximum Impedance
Ra	800Ω	1.2kΩ

Current Capability and Over-Current Protection

The RT9752 supports current rating defined by USB Type-C standard with corresponding over-current protection which is configured by the CHG and CHG_HI pins setting. The RT9752 has an internal current limit circuit that protects the device during overload condition or shorting events. After output voltage is successfully powered up and closed to input voltage, the output could draw the current until trip current threshold(I_{TRIP}). When the loading is higher than I_{TRIP}, output voltage will drop and approach to GND. The current limit will change to I_{LIM} level to protect the system. Besides, the current limit is set at I_{LIM} level when output voltage is not established.

The RT9752 further protects device by sequentially switching off and on hiccup cycles if large output voltage drop under current limit condition or the thermal protection engages. The current capability is shown in Table 4.

Table 4. USB Type-C Current Advertisement and Current Limit Threshold

CHG	CHG_HI	Current Advertisement	Current Limit Threshold
Low	Low /High	Standard USB2.0/3.0	1.7A
High	Low	1.5A	1.7A
High	High	3A	3.4A

Reverse-Voltage Protection (RVP) and High Voltage Tolerance

The RVP circuit is integrated to prevent leakage current from output voltage to input voltage. If there is any high voltage plugging in output voltage, the output voltage exceeds the input voltage around 100mV instantly, the reverse voltage protection circuitry will turn internal power FET off immediately to protect the input power supply. The power FET will turn on again when output voltage returns to the same level with input voltage. In addition, to avoid the existing voltage of VBUS higher than 5.25V, the RT9752 provides dynamic gate driver control loop to implement the reverse-voltage protection. Device will always try to regulate the output voltage, lower than intput voltage. If output voltage is higher than input voltage when enabling the device, the power FET will never turn on. The device will always do pre-check before switching on the power MOSFETs. The RT9752 offers 28 V tolerance on VOUT pin and 24V tolerance on CC pins to ensure the device is able to work on a USB PD port.

Over-Voltage Protection (OVP)

The RT9752A also provides the over-voltage protection. When the output voltage exceeds over-voltage threshold (6V, Typ.), the over-voltage protection circuitry will turn off internal power FET immediately to protect the input power supply. The power FET will turn on again when output voltage is lower than voltage threshold (6V, Typ.). Besides, when OVP is triggered, the output voltage is almost the same as input voltage (VOUT – VIN < 100mV). However, OVP behavior is different from RVP (VOUT – VIN > 100mV).

Thermal Shutdown

The RT9752 continuously monitors the operating temperature of the power switch for over-temperature protection. The RT9752 turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 150°C due to over-current or short circuit conditions. The pass element turns on again after the junction temperature cools down to 130°C.

Indicator LD_DET# Response

The load detect function enabled when port configures 3A rated VBUS charging (CHG = CHG_HI = High). LD_DET# pin asserts (active low) when the device monitored that current draw by UFP device exceeds 1.9A (Typ.). Connect LD_DET# pin with a pull-high resistor with 100kΩ to VCC. LD_DET# can be left open or tied to GND when not used.

Indicator FAULT# Response

The FAULT# pin is an open drain output that asserts (active low) when device VOUT current exceeds its programmed value with large output voltage drop after VOUT power

ready or under over-temperature protection. The FAULT# signal remains asserted until the fault condition is removed and the device resumes normal operation. Connect FAULT# with a pull-high resistor with 100kΩ to VCC. FAULT# can be left open or tied to GND when not used.

Indicator AUDIO# / DEBUG# / UFP# / POL# Response

The AUDIO#, DEBUG#, POL# and UFP# pins are all open drain output that asserts (active low) respectively with different CC1 and CC2 pin configured settings. The AUDIO# pin asserts when port configured audio accessory mode (both CC1 and CC2 pin = Ra). Similarly, the DEBUG# pin asserts when port configured debug accessory mode (both CC1 and CC2 pin = Rd). The UFP# pin drives low when port recognizes an UFP device inserted, and the POL# pin asserts if reverse plug orientation UFP# is detected. All of these pins are connected to pull-high resistors with 100kΩ to VCC respectively when used. Tie to GND or leave open when not used.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, VCC ---------- –0.3V to 7V
- Output Voltage, VOUT ---------- –0.3V to 28V
- Output Voltage, CC1, CC2 ---------- –0.3V to 24V
- Other I/O Voltages ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20TL 3x4 (FC) ---------- 1.54W
- Package Thermal Resistance (Note 2)
  WQFN-20TL 3x4 (FC), θ_{JA} ---------- 64.6°C/W
  WQFN-20TL 3x4 (FC), θ_{JC} ---------- 8.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 500V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage VIN ---------- 4.5V to 5.5V
- Supply Input Voltage VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –10°C to 105°C

Electrical Characteristics

(VIN = VCC = 5V, V_{EN} = V_{CHG} = V_{CHG_HI} = VCC, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J from –10°C to105°C, unless other noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply VIN						
UVLO Threshold	$V_{TH\_UVLO\_VIN}$	Rising threshold voltage for UVLO	--	4	--	V
UVLO Hysteresis	$V_{TH\_UVLO\_HYS}$	Hysteresis	--	100	--	mV
Supply Current	I_{VIN_SHDN}	Disabled supply current, V_{EN} = 0V	--	--	1	μA
	I_{VIN_CCOPEN}	Enabled with CC lines open, V_{EN} = VCC	--	--	2	μA
	I_{VIN_ACC}	Enabled with accessory mode or dangling e-marked cable on CC lines ,V_{EN} = VCC, CC = Ra/Ra	--	--	10	μA
	I_{VIN_UFP1}	Enabled with UFP attached V_{CHG} = 0V, 0V ≤ VCCx ≤ 1.5V	--	200	250	μA
	I_{VIN_UFP2}	Enabled with UFP attached V_{CHG} = VIN and V_{CHG_HI} = 0V, 0V ≤ VCCx ≤ 1.5V	--	200	250	μA
	I_{VIN_UFP3}	Enabled with UFP attached 0V ≤ VCCx ≤ 2.45V	--	200	250	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply VCC						
Supply Current	I_{VCC_SHDN}	Disabled supply current, V_{EN} = 0V	--	--	2	μA
	I_{VCC_CCOPEN}	Enabled with CC lines open, V_{EN} = VCC	--	--	3	μA
	I_{VCC_ACC}	Enabled with accessory mode or dangling e-marked cable on CC lines ,V_{EN} = VCC, CC = Ra/Ra	--	240	288	μA
Supply Current	I_{VCC_UFP1}	Enabled with UFP attached V_{CHG} = 0V, 0V ≤ VCCx ≤ 1.5V	--	330	396	μA
	I_{VCC_UFP2}	Enabled with UFP attached V_{CHG} = V_{IN} and V_{CHG_HI} = 0V, 0V ≤ V_{CCx} ≤1.5V	--	430	516	μA
	I_{VCC_UFP3}	Enabled with UFP attached, 0V ≤ VCCx ≤ 2.45V	--	580	696	μA
Logic Threshold						
EN/CHG/CHG_HI	V_{TH_H}	Rising edge	--	0.93	1.15	V
	V_{TH_L}	Falling edge	0.65	0.88	--	V
	V_{TH_HYS}	Hysteresis	--	70	--	mV
EN	I_{EN}	Input current ,V_{EN} = 0V or 6.5V	–0.5	--	0.5	μA
FAULT#	V_{OL}	Output low voltage, I_{FAULT} = 1mA	--	--	350	mV
	I_{OFF}	Off-state leakage, V_{FAULT} = VCC	--	--	1	μA
LD_DET#	V_{OL}	Output low voltage, I_{FAULT} = 1mA	--	--	350	mV
	I_{OFF}	Off-state leakage, V_{FAULT} = VCC	--	--	1	μA
	I_{TH}	VOUT sourcing, rising threshold current for load detect, T_J = 25°C	1.7	1.9	2.1	A
	I_{TH_HYS}	Hysteresis, T_J = 25°C	--	150	--	mA
UFP#/POL#	V_{OL}	Output low voltage, I_{FAULT} = 1mA	--	--	250	mV
AUDIO#/DEBUG#	I_{OFF}	Off-state leakage, V_{FAULT} = VCC	--	--	1	μA
VOUT – VBUS Power Switch						
On-Resistance	$R_{DS(ON)}$	T_J = 25°C, I_{OUT} = 3A	--	34	37	mΩ
Reverse Leakage Current	I_{REV}	V_{OUT} = 6.5V, VIN = V_{EN} = 0V, –40°C ≤ T_J ≤ 85°C, I_{REV} is current out of VIN pin	--	0	3	μA
Over Current Trip Threshold	I_{TRIP}	V_{CHG} = 0V or V_{CC} and V_{CHG_HI} = 0V T_J = 25°C , SR = 100A/s	2	3	3.4	A
		V_{CHG} = V_{CC} and V_{CHG_HI} = V_{CC} T_J = 25°C , SR = 100A/s	3.6	5	5.8	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit Level	I_{LIM}	V_{CHG} = 0V or VCC and V_{CHG_HI} = 0V T_J = 25°C, V_{OUT} < 1V	1.54	1.7	1.86	A
		V_{CHG} = VCC and V_{CHG_HI} = VCC T_J = 25°C, V_{OUT} < 1V	3.09	3.4	3.71	A
Discharge Resistance	R_{DISCHG}	V_{OUT} = 4V, UFP removed from CC lines, time < tw_DCHG	400	500	600	Ω
Bleed Discharge Resistance	R_{DISCHG_BLEED}	VOUT = 4V, No UFP on CC lines, time > tw_DCHG	100	150	250	kΩ
Rise Time	t_R	VIN1 = 5V, C_L = 1μF, R_L = 100Ω (measured from 10% to 90% of final value)	--	2.5	--	ms
Fall Time	t_F		--	0.55	--	ms
CC1/CC2 – VCONN Power Switch /Current Limit						
On-Resistance	$R_{DS(ON)}$	T_J = 25°C, I_{OUT} = 250mA	--	570	1000	mΩ
Over Current Trip Threshold	I_{TRIP}	T_J = 25°C, SR = 100A/s	330	420	510	mA
Current Limit	I_{LIM}	T_J = 25°C, V_{CCx} < 1V	300	355	410	mA
Rise Time	t_R	VIN1 = 5V, C_L = 1μF, R_L = 100Ω (measured from 10% to 90% of final value)	--	45	--	μs
Fall Time	t_F		--	220	--	μs
CC1/CC2 – Connect Management – Dangling E-Marked Cable Mode						
Sourcing Current	I_{SRC}	Current on the pass through CC Line 0V ≤ VCCx ≤ 1.5V	74	93	112	μA
		Current on the Ra CC line 0V ≤ VCCx ≤ 1.5V	74	93	112	μA
CC1/CC2 – Connect Management – Accessory Mode						
Sourcing Current	I_{SRC}	CCx Sourcing current (CC2- Audio, CC1-Debug), V_{CHG} = V_{CHG_HI} = 0V	--	80	--	μA
		CCx Sourcing current (CC1- Audio, CC2-Debug), V_{CHG} = V_{CHG_HI} = 0V	--	80	--	μA
CC1/CC2 – Connect Management – UFP Mode						
Sourcing Current	I_{SRC}	Current with VIN in UVLO 0V ≤ VCCx ≤ 1.5V VIN1 < $V_{TH\_UVLO\_VIN}$	64	80	96	μA
		V_{CHG} = 0V and V_{CHG_HI} = 0V, 0V ≤ VCCx ≤ 1.5V	70	80	90	μA
		V_{CHG} = VCC and V_{CHG_HI} = 0V, 0V ≤ VCCx ≤ 1.5V	158	180	202	μA
		V_{CHG} = VCC and V_{CHG_HI} = VCC, 0V ≤ VCCx ≤ 2.45V	290	330	370	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Shut Down						
Thermal Shutdown Threshold	T_{SD}	Rising threshold temperature for device shutdown	--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Asserting / De-Asserting Timing						
FAULT#	t_{DEGA}	Asserting deglitch due to over-current and VOUT < 1V (Note 5)	1.6	2.5	3.4	ms
	t_{DEGAD}	De-asserting deglitch	5.5	8.2	10.7	ms
LD_DET#	t_{DEGA}	Asserting deglitch	45	65	85	ms
	t_{DEGAD}	De-asserting deglitch	1.5	2.15	2.9	s
UFP# / POL#	t_{DEGA}	Asserting deglitch	100	150	200	ms
AUDIO#/DEBUG#	t_{DEGAD}	De-asserting deglitch	7.9	12.5	17.7	ms

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

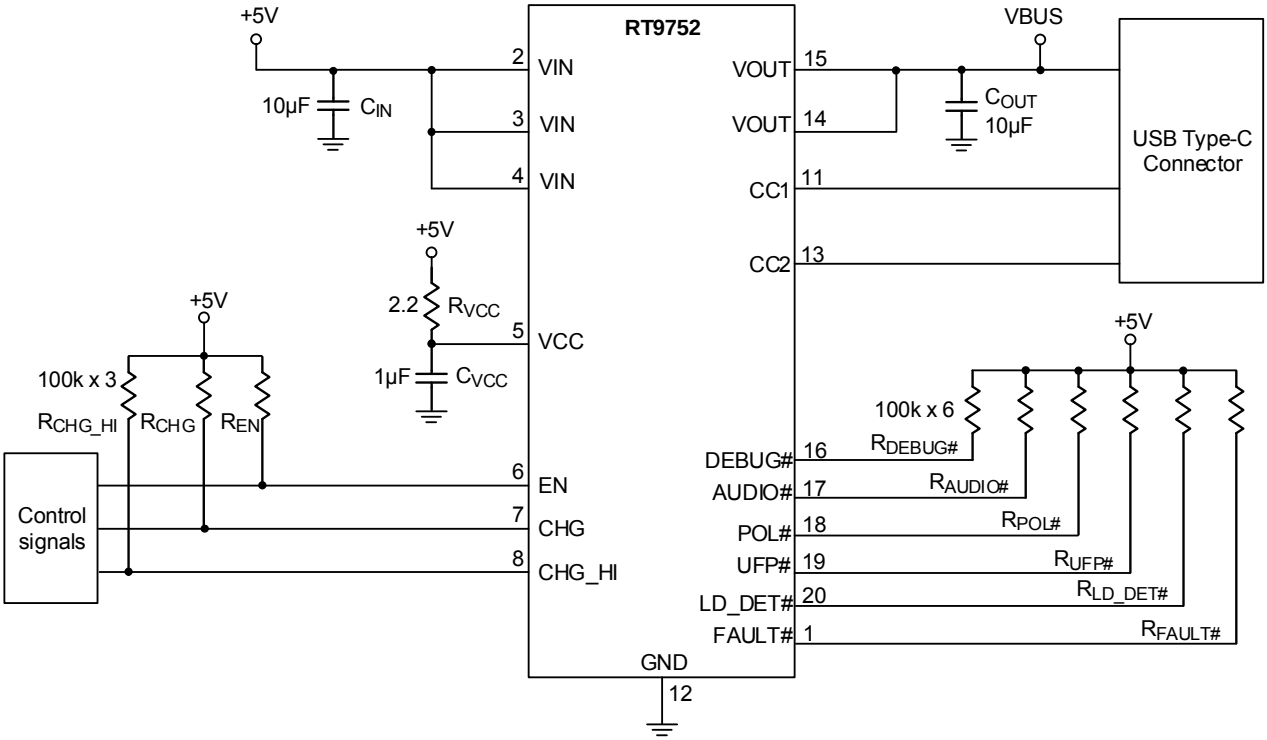
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

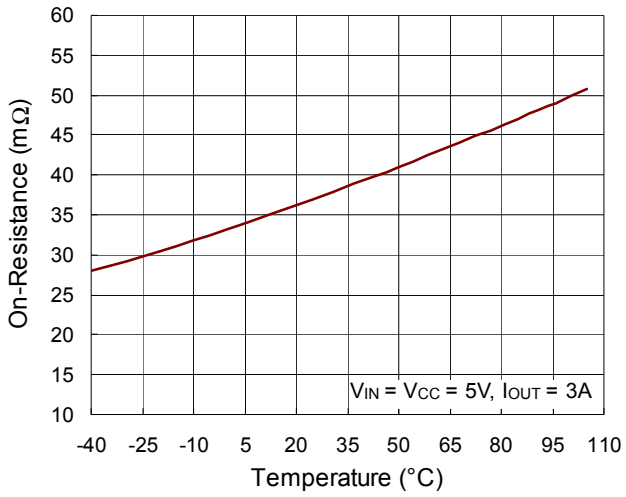
Note 5. Function is enabled after VOUT power is ready.

Typical Application Circuit

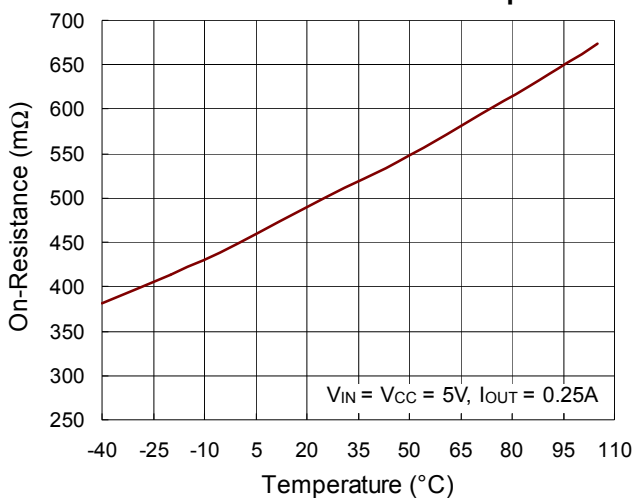


Typical Operating Characteristics

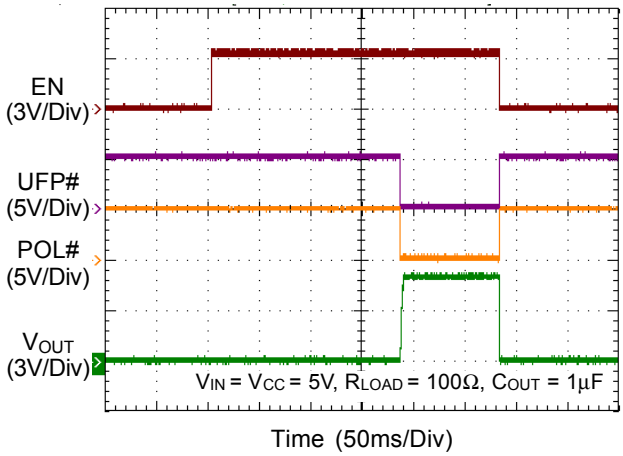
VBUS On-Resistance vs. Temperature



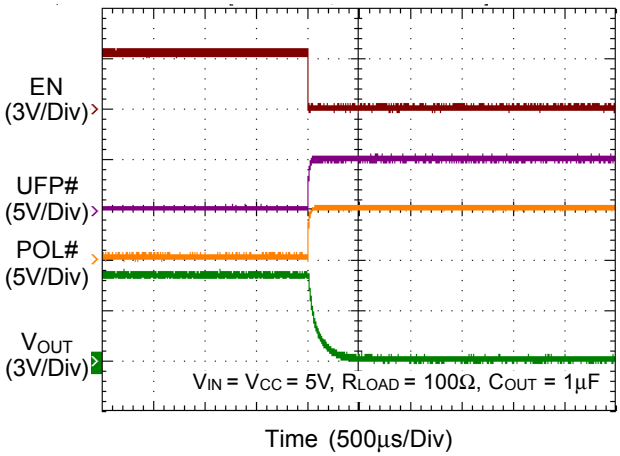
VCONN On-Resistance vs. Temperature



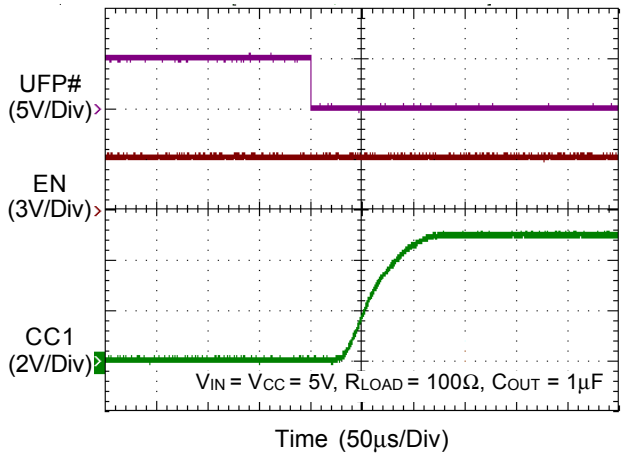
VBUS Power On from EN



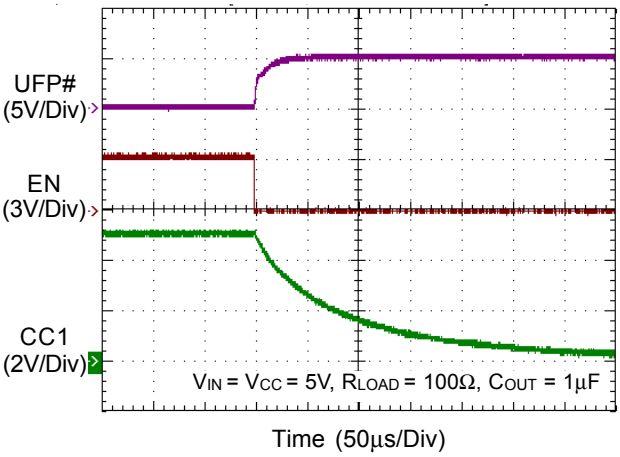
VBUS Power Off from EN



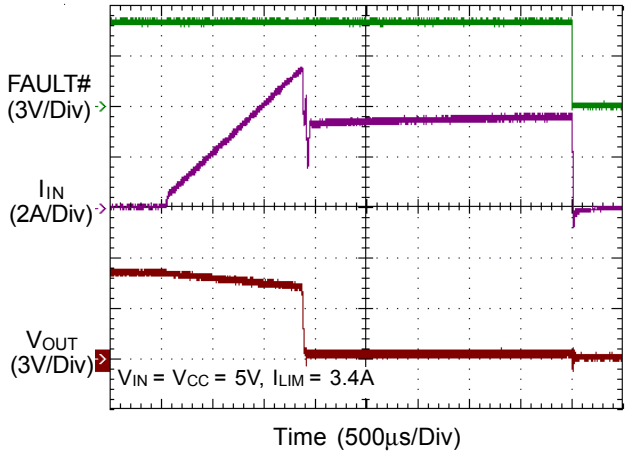
VCONN Power On from EN



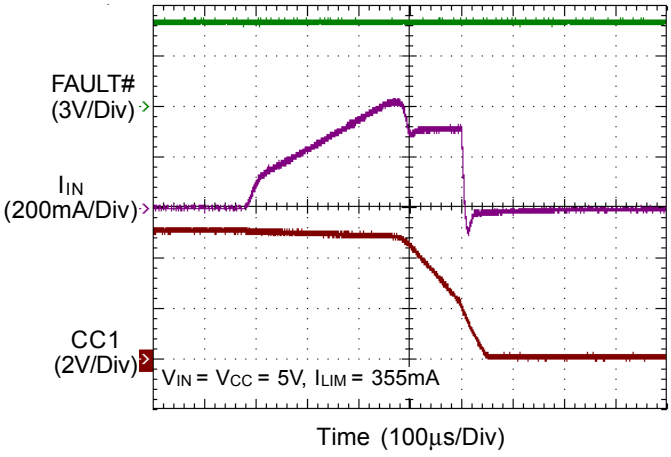
VCONN Power Off from EN



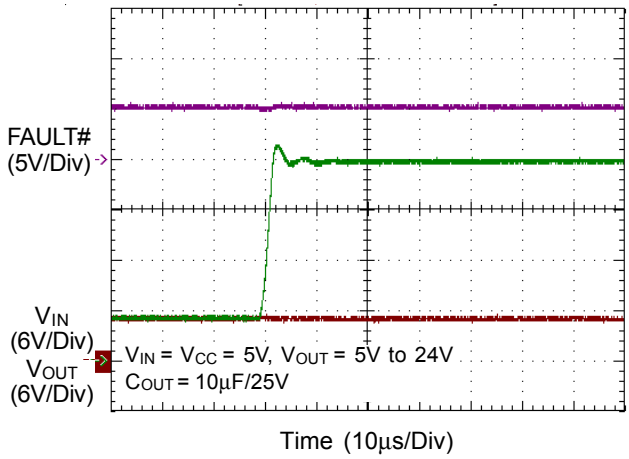
VBUS Current Limit



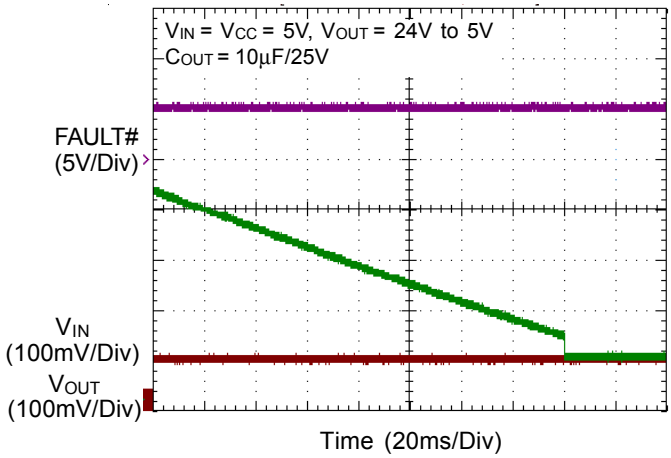
VCONN Current Limit



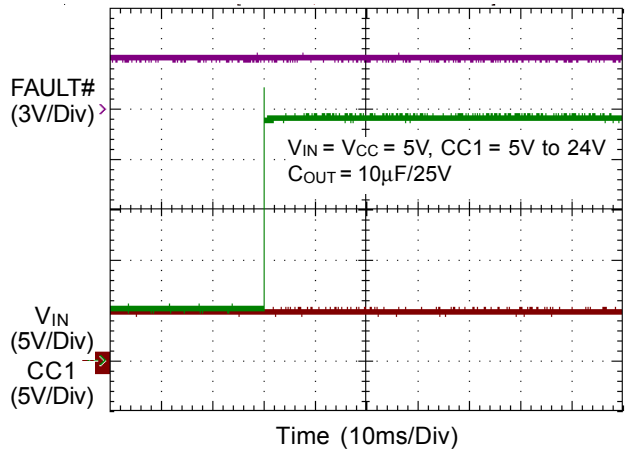
VBUS Reverse Voltage Protection



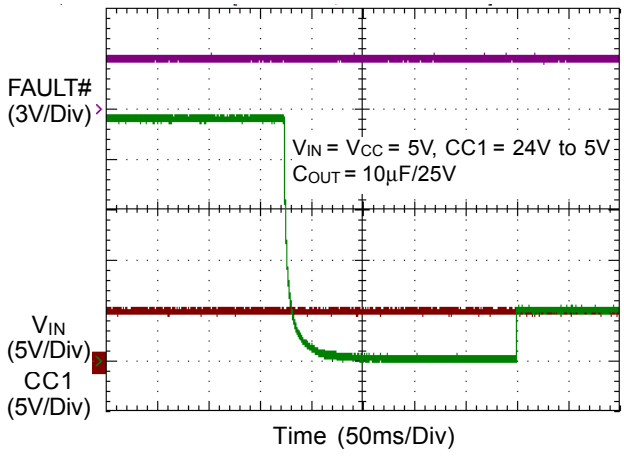
VBUS Reverse Voltage Protection Recovery



CC Pin Reverse Voltage Protection



CC pin Reverse Voltage Protection Recovery



Application Information

The RT9752 is a Type-C DFP load switch and controller that supports all Type-C DFP required functions and further integrated HV protection in internal power switches for VCONN and VBUS. The RT9752 can only be used in a USB2.0 or USB3.0 port implementation, but BC1.2, because of no interacting with USB D+/D-. As UFP is attached detecting by CC pins, RT9752 allows power delivering to VBUS. Conversely, as UFP is detached, power is removed by RT9752. Besides, the RT9752 applies three current advertisements for Type-C through CHG and CHG_HI pin setting, and provides over-current limit protection for device. Apart from delivering power to UFP, the RT9752 also supports Audio and Debug accessory modes.

Input and Output Filter Capacitor

Although the RT9752 provides RVP function to protect any abnormal electrical over-stress happening, there are risks of input voltage overshoot and output undershoot to damage the device.

For the input voltage overshoot, as VBUS is suddenly short circuit while RT9752 is turn-off, the stored energy in input trace inductor is going to release to VIN terminal and cause VIN abnormal oscillation. For avoiding VIN abnormal rising over 7V (absolute maximum rating), a large input capacitor is required to reduce voltage overshoot during output short circuit. Hence, it's strongly suggested to put a 10μF to 22μF low-ESR ceramic capacitor as input filter capacitor. Moreover, for eliminating local noise de-coupling, a 0.1μF or greater ceramic bypass capacitor connected between VIN to GND is recommended and place it as close to the VIN terminal as possible.

The output undershoot is caused by output trace inductance after short circuit happening at VBUS. As output short circuit occurring, the RT9752 is turned off to reduce output current and finally the stored energy in trace inductance of output drives the output voltage down to negative level. That negative voltage on output would cause unexpected circuit behavior or damage. However, for preventing any negative voltage influences, the output capacitor is required, which is sufficient to control voltage undershoot. According to USB standard, 120μF minimum output capacitance is required to meet the minimum drop voltage of VBUS (330mV), but the maximum output capacitance is constrained from the applications. Too much output capacitor induces large inrush current during power on period and large VIN spike as output short circuit happens. Thus, the recommended output capacitance is from 120μF to 220μF.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20TL 3x4 (FC) package, the thermal resistance, θ_{JA}, is 64.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (64.6°C/W) = 1.54W for a WQFN-20TL 3x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

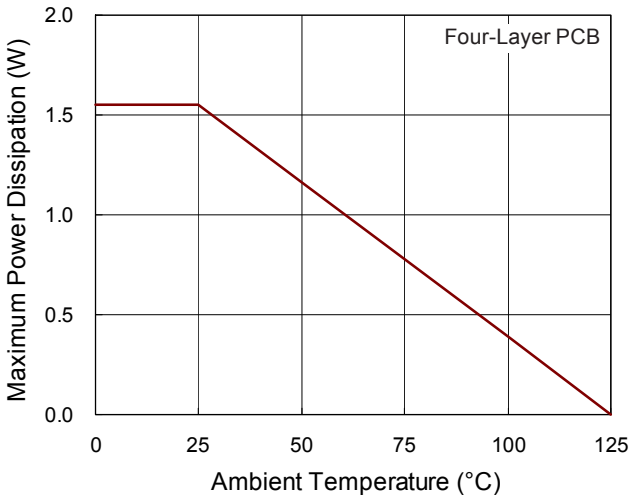


Figure 1. Derating Curve of Maximum Power Dissipation

Layout consideration

In order to meet the voltage drop, droop, and EMI requirements, careful PCB layout is necessary. The following guidelines must be followed :

Locate the ceramic bypass capacitors as close as possible to the VIN pins of the RT9752.

- Place a ground plane under all circuitry to lower both resistance and inductance, and improve DC and transient performance (Use a separate ground and power plans if possible).
- Avoid vias as much as possible. If vias are necessary, make them as large as feasible.
- Place cuts in the ground plane between ports to help reduce the coupling of transients between ports.

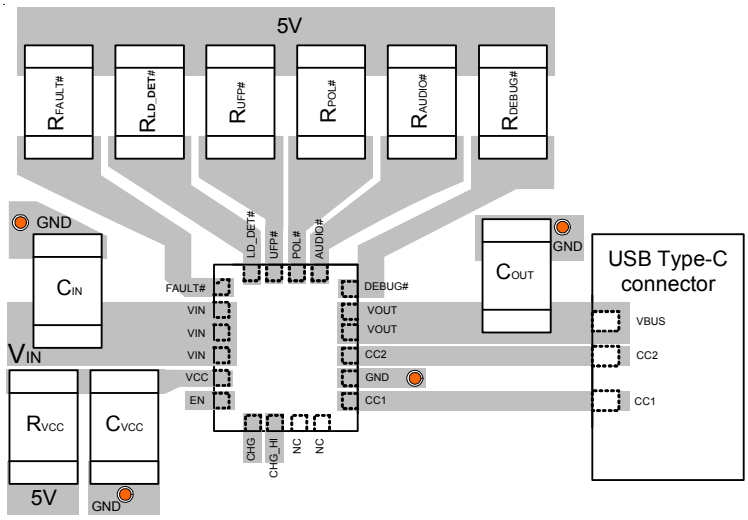
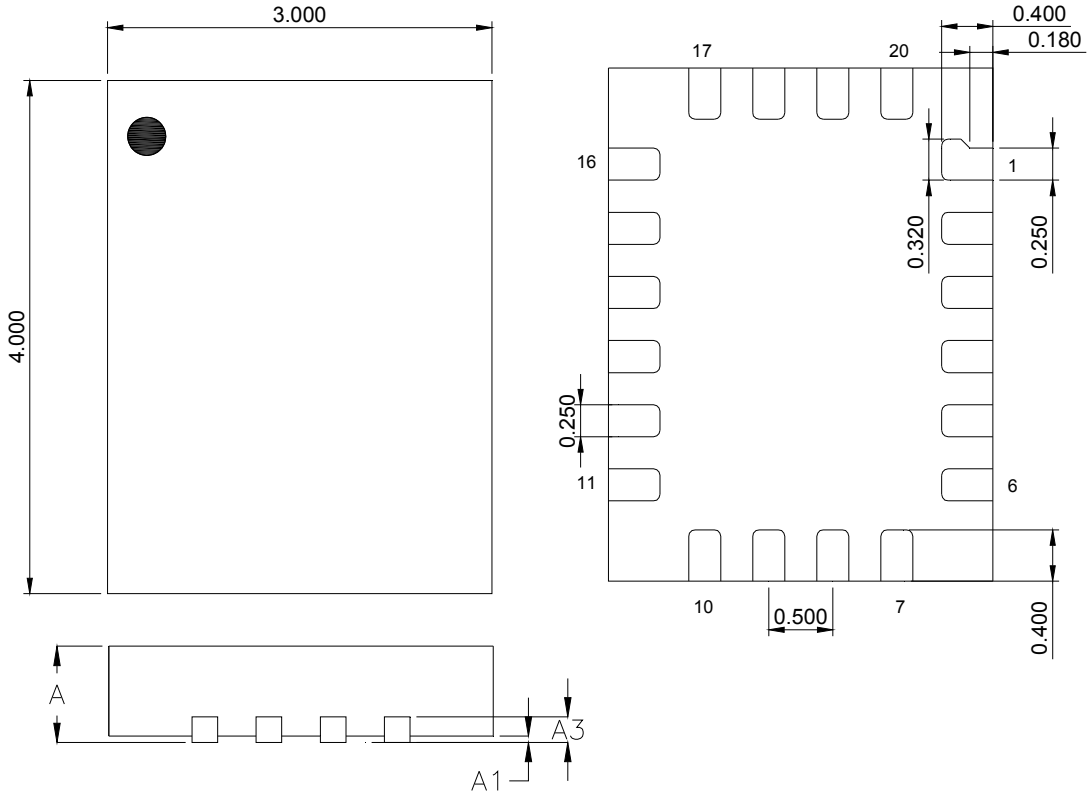


Figure 2. PCB Layout Guide

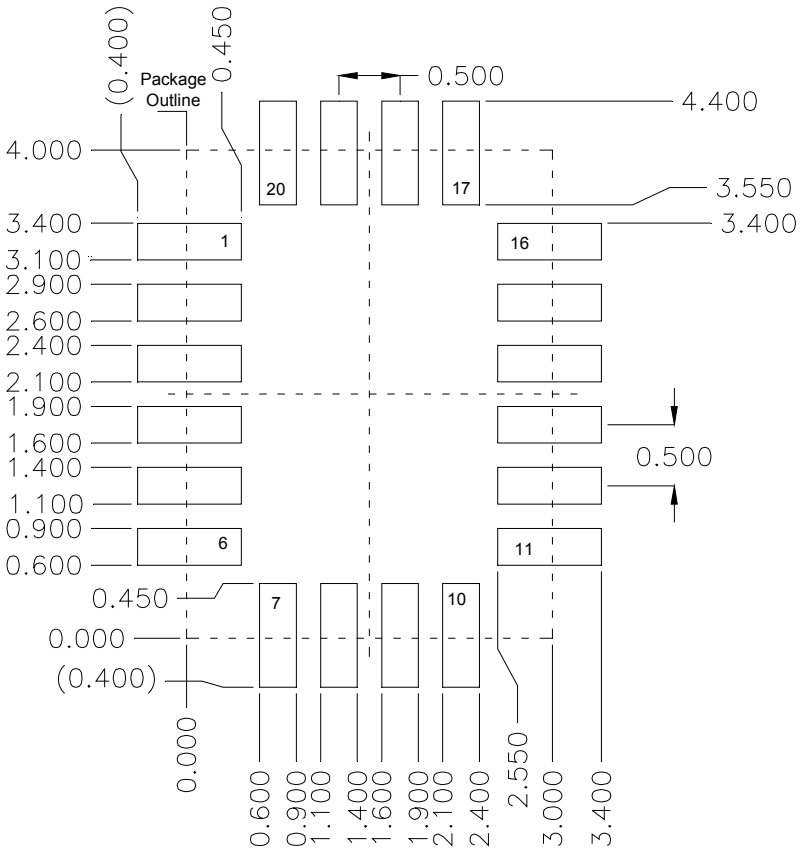
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	Tolerance
A3	0.175	0.250	0.007	0.010	±0.050

W-Type 20TL QFN 3x4 (FC) Package

Footprint Information



Package	Number of Pin	Tolerance
V/W/U/XQFN3x4-20T(FC)	20	±0.05

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